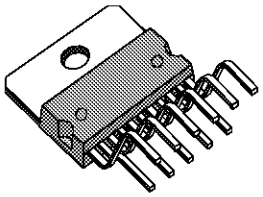
SGS-THOMSON MICROELECTRONICS

L296
L296P

HIGH CURRENT SWITCHING REGULATORS

- 4 A OUTPUT CURRENT
- 5.1 V TO 40 V OUTPUT VOLTAGE RANGE
- 0 TO 100 % DUTY CYCLE RANGE
- PRECISE (±2 %) ON-CHIP REFERENCE
- SWITCHING FREQUENCY UP TO 200 KHz
- VERY HIGH EFFICIENCY (UP TO 90 %)
- VERY FEW EXTERNAL COMPONENTS
- SOFT START
- RESET OUTPUT
- EXTERNAL PROGRAMMABLE LIMITING CURRENT (L296P)
- CONTROL CIRCUIT FOR CROWBAR SCR
- INPUT FOR REMOTE INHIBIT AND SYNCHRONUS PWM
- THERMAL SHUTDOWN



Multiwatt®
(15 lead)

ORDERING NUMBERS :

L296 (Vertical)	L296HT (Horizontal)
L296P (Vertical)	L296PHT (Horizontal)

DESCRIPTION

The L296 and L296P are stepdown power switching regulators delivering 4 A at a voltage variable from 5.1 V to 40 V.

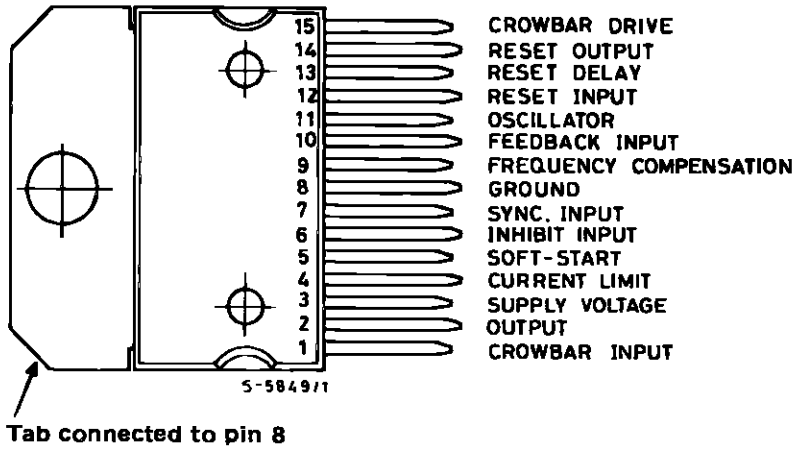
Features of the devices include soft start, remote inhibit, thermal protection, a reset output for microprocessors and a PWM comparator input for synchronization in multichip configurations.

The L296P incudes external programmable limiting current.

The L296 and L296P are mounted in a 15-lead Multiwatt® plastic power package and requires very few external components.

Efficient operation at switching frequencies up to 200 KHz allows a reduction in the size and cost of external filter components. A voltage sense input and SCR drive output are provided for optional crowbar overvoltage protection with an external SCR.

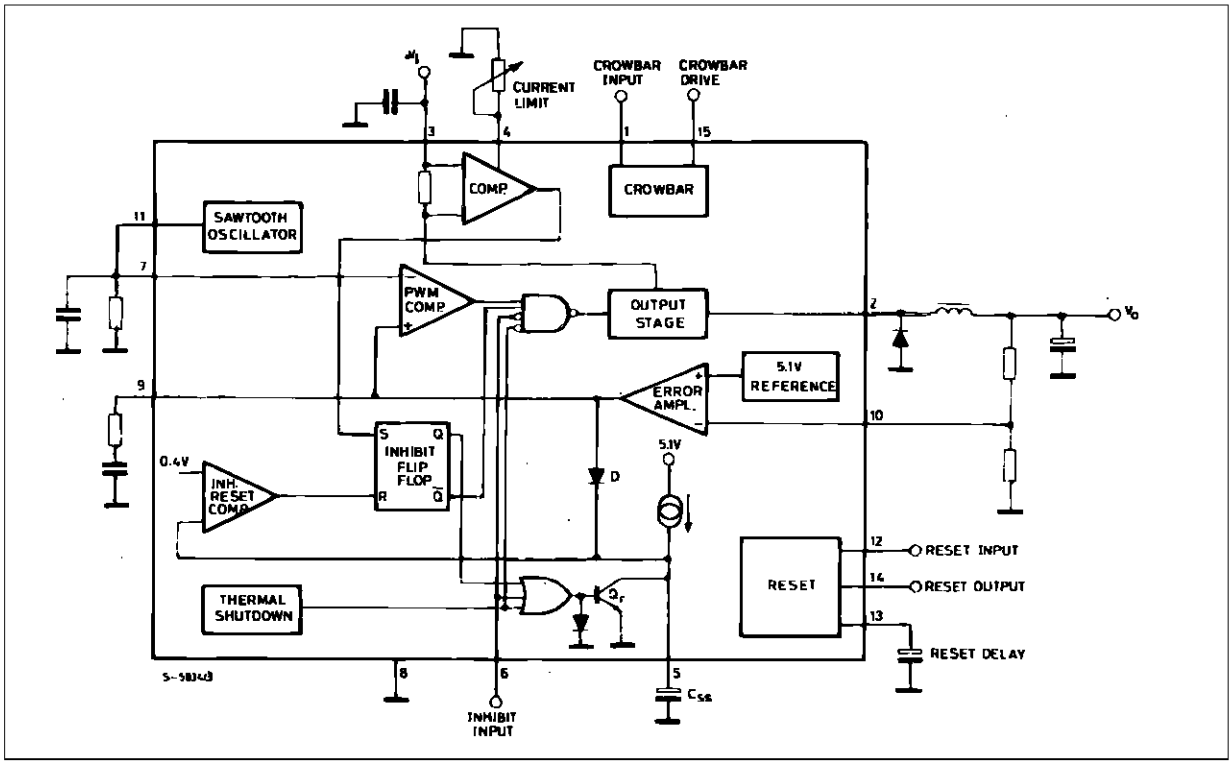
PIN CONNECTION (top view)



PIN FUNCTIONS

N°	Name	Function
1	CROWBAR INPUT	Voltage Sense Input for Crowbar Overvoltage Protection. Normally connected to the feedback input thus triggering the SCR when V_{out} exceeds nominal by 20 %. May also monitor the input and a voltage divider can be added to increase the threshold. Connected to ground when SCR not used.
2	OUTPUT	Regulator Output
3	SUPPLY VOLTAGE	Unrergulated Voltage Input. An internal Regulator Powers the L296s Internal Logic.
4	CURRENT LIMIT	A resistor connected between this terminal and ground sets the current limiter threshold. If this terminal is left unconnected the threshold is internally set (see electrical characteristics).
5	SOFT START	Soft Start Time Constant. A capacitor is connected between this terminal and ground to define the soft start time constant. This capacitor also determines the average short circuit output current.
6	INHIBIT INPUT	TTL – Level Remote Inhibit. A logic high level on this input disables the device.
7	SYNC INPUT	Multiple L296s are synchronized by connecting the pin 7 inputs together and omitting the oscillator RC network on all but one device.
8	GROUND	Common Ground Terminal
9	FREQUENCY COMPENSATION	A series RC network connected between this terminal and ground determines the regulation loop gain characteristics.
10	FEEDBACK INPUT	The Feedback Terminal on the Regulation Loop. The output is connected directly to this terminal for 5.1V operation ; it is connected via a divider for higher voltages.
11	OSCILLATOR	A parallel RC networki connected to this terminal determines the switching frequency. This pin must be connected to pin 7 input when the internal oscillator is used.
12	RESET INPUT	Input of the Reset Circuit. The threshold is roughly 5 V. It may be connected to the feedback point or via a divider to the input.
13	RESET DELAY	A capacitor connected between this terminal and ground determines the reset signal delay time.
14	RESET OUTPUT	Open collector reset signal output. This output is high when the supply is safe.
15	CROWBAR OUTPUT	SCR gate drive output of the crowbar circuit.

BLOCK DIAGRAM



CIRCUIT OPERATION

(refer to the block diagram)

The L296 and L296P are monolithic stepdown switching regulators providing output voltages from 5.1V to 40V and delivering 4A.

The regulation loop consists of a sawtooth oscillator, error amplifier, comparator and the output stage. An error signal is produced by comparing the output voltage with a precise 5.1V on-chip reference (zener zap trimmed to ± 2 %). This error signal is then compared with the sawtooth signal to generate the fixed frequency pulse width modulated pulses which drive the output stage. The gain and frequency stability of the loop can be adjusted by an external RC network connected to pin 9. Closing the loop directly gives an output voltage of 5.1V. Higher voltages are obtained by inserting a voltage divider.

Output overcurrents at switch on are prevented by the soft start function. The error amplifier output is initially clamped by the external capacitor Css and allowed to rise, linearly, as this capacitor is charged by a constant current source.

Output overload protection is provided in the form of a current limiter. The load current is sensed by an internal metal resistor connected to a comparator. When the load current exceeds a preset threshold this comparator sets a flip flop which disables the output stage and discharges the soft start capacitor. A second comparator resets the flip flop when the voltage across the soft start capacitor has fallen to 0.4V. The output stage is thus re-enabled and the output voltage rises under control of the soft start network. If the overload condition is still present the limiter will trigger again when the threshold current is reached. The average short circuit current is limited to a safe value by the dead time introduced by the soft start network.

The reset circuit generates an output signal when the supply voltage exceeds a threshold programmed by an external divider. The reset signal is generated with a delay time programmed by an external capacitor. When the supply falls below the threshold the reset output goes low immediately. The reset output is an open collector.

The scrowbar circuit senses the output voltage and the crowbar output can provide a current of 100mA to switch on an external SCR. This SCR is triggered when the output voltage exceeds the nominal by 20%. There is no internal connection between the output and crowbar sense input therefore the crowbar can monitor either the input or the output.

A TTL - level inhibit input is provided for applications such as remote on/off control. This input is activated by high logic level and disables circuit operation. After an inhibit the L296 restarts under control of the soft start network.

The thermal overload circuit disables circuit operation when the junction temperature reaches about 150 °C and has hysteresis to prevent unstable conditions.

Figure 1 : Reset Output Waveforms

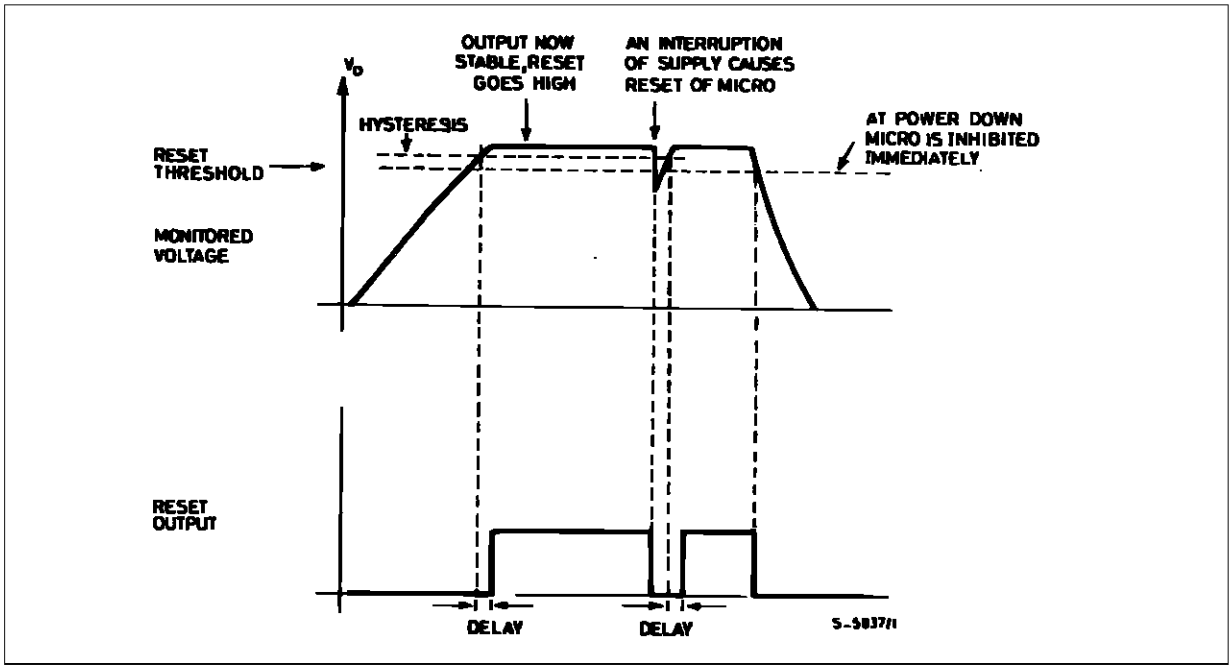


Figure 2 : Soft Start Waveforms

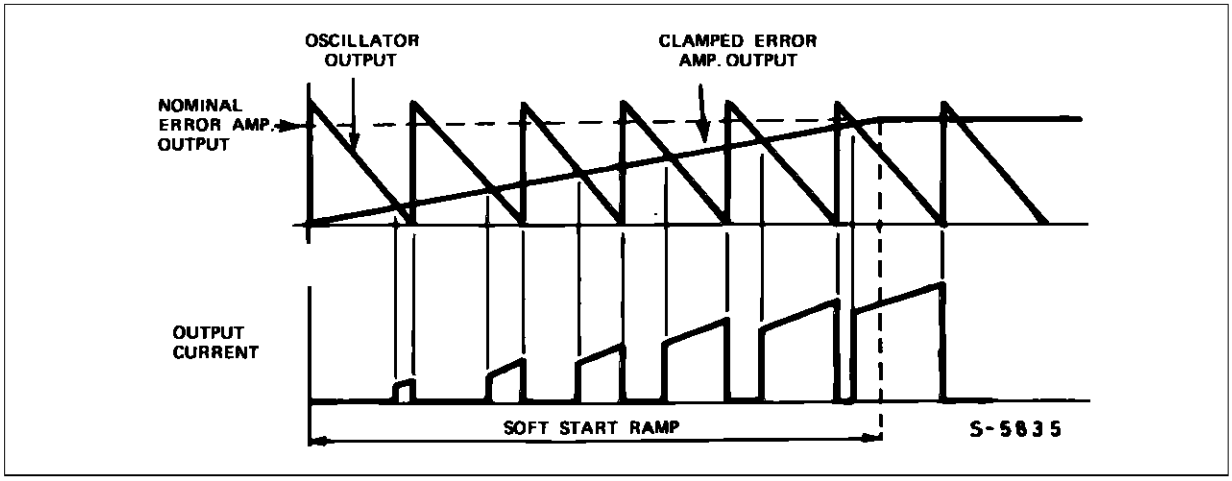
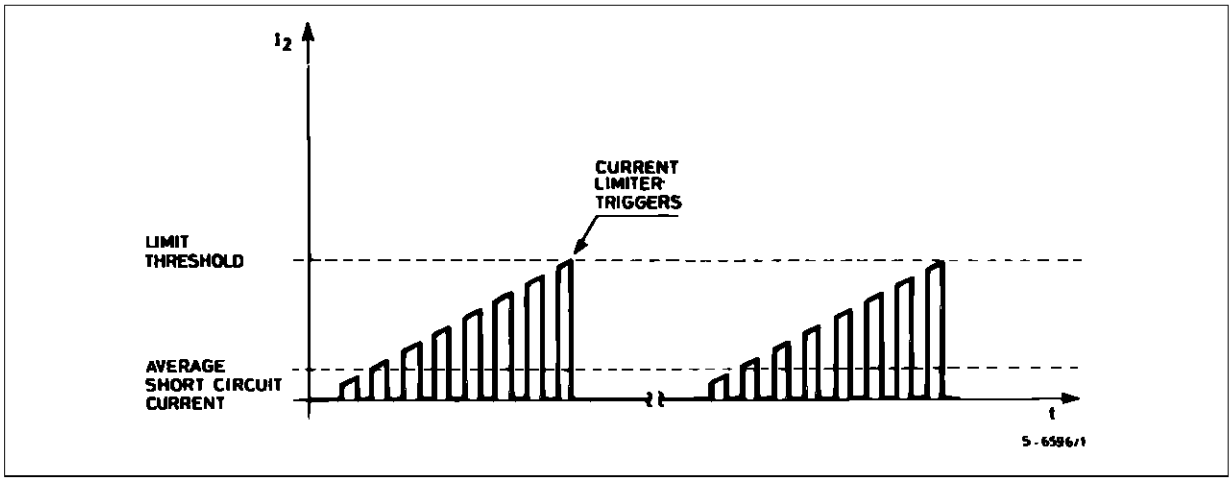


Figure 3 : Current Limiter Waveforms



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_i	Input Voltage (pin 3)	50	V
$V_i - V_2$	Input to Output Voltage Difference	50	V
V_2	Output DC Voltage Output Peak Voltage at t = 0.1 µsec f = 200KHz	– 1 – 7	V V
V_1, V_{12}	Voltage at Pins 1, 12	10	V
V_{15}	Voltage at Pin 15	15	V
V_4, V_5, V_7, V_9, V_{13}	Voltage at Pins 4, 5, 7, 9 and 13	5.5	V
V_{10}, V_6	Voltage at Pins 10 and 6	7	V
V_{14}	Voltage at Pin 14 ($I_{14} \leq 1$ mA)	V_i	
I_9	Pin 9 Sink Current	1	mA
I_{11}	Pin 11 Source Current	20	mA
I_{14}	Pin 14 Sink Current ($V_{14} < 5$ V)	50	mA
P_{tot}	Power Dissipation at $T_{case} \leq 90$ °C	20	W
T_j, T_{stg}	Junction and Storage Temperature	– 40 to 150	°C

THERMAL DATA

Symbol	Parameter		Value	Unit
$R_{th\ j\text{-}case}$	Thermal Resistance Junction-case	Max.	3	°C/W
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient	Max.	35	°C/W

ELECTRICAL CHARACTERISTICS

(refer to the test circuits $T_j = 25^oC$, $V_i = 35V$, unless otherwise specified)

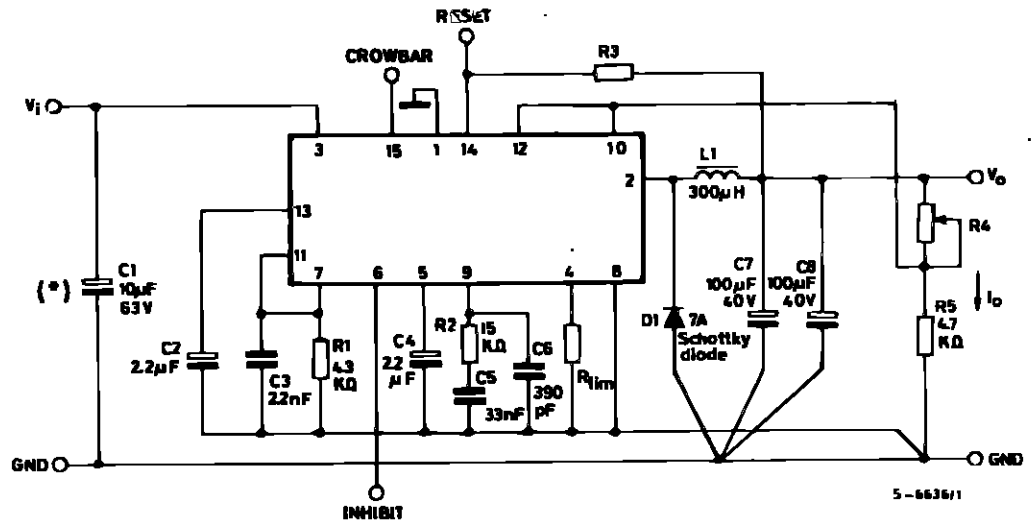
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit	Fig.
DYNAMIC CHARACTERISTICS (pin 6 to GND unless otherwise specified)							
V_o	Output Voltage Range	$V_i = 46V$, $I_o = 1A$	V_{ref}		40	V	4
V_i	Input Voltage Range	$V_o = V_{ref}$ to 36V, $I_o \leq 3A$	9		46	V	4
V_i	Input Voltage Range	Note (1), $V_o = V_{REF}$ to 36V $I_o = 4A$			46	V	4
ΔV_o	Line Regulation	V_i =10V to 40V, $V_o = V_{ref}$, $I_o = 2A$		15	50	mV	4
ΔV_o	Load Regulation	$V_o = V_{ref}$ I_o = 2A to 4A I_o = 0.5A to 4A		 10 15	 30 45	mV	4
V_{ref}	Internal Reference Voltage (pin 10)	V_i = 9V to 46V, I_o = 2A	5	5.1	5.2	V	4
$\frac{\Delta V_{ref}}{\Delta T}$	Average Temperature Coefficient of Reference Voltage	T_j = 0°C to 125°C, I_o = 2A		0.4		mV/°C	
V_d	Dropout Voltage Between Pin 2 and Pin 3	I_o = 4A I_o = 2A		2 1.3	3.2 2.1	V V	4 4
I_{2L}	Current Limiting Threshold (pin 2)	L296 - Pin 4 Open, V_i = 9V to 40V, $V_o = V_{ref}$ to 36V	4.5		7.5	A	4
		L296P - V_i = 9V to 40V, $V_o = V_{ref}$ Pin 4 Open R_{lim} = 22kΩ	 5 2.5		 7 4.5	A	4
I_{SH}	Input Average Current	V_i = 46V, Output Short-circuited		60	100	mA	4
η	Efficiency	I_o = 3 A $V_o = V_{ref}$ V_o = 12V		 75 85		%	4
SVR	Supply Voltage Ripple Rejection	ΔV_i = 2 V_{rms}, f_{ripple} = 100Hz $V_o = V_{ref}$, I_o = 2A	50	56		dB	4
f	Switching Frequency		85	100	115	kHz	4
$\frac{\Delta f}{\Delta V_i}$	Voltage Stability of Switching Frequency	V_i = 9V to 46V		0.5		%	4
$\frac{\Delta f}{\Delta T_j}$	Temperature Stability of Switching Frequency	T_j = 0°C to 125°C		1		%	4
f_{max}	Maximum Operating Switching Frequency	$V_o = V_{ref}$, I_o = 1A	200			kHz	–
T_{sd}	Thermal Shutdown Junction Temperature	Note (2)	135	145		°C	–
DC CHARACTERISTICS							
I_{3Q}	Quiescent Drain Current	V_i = 46V, V_7 = 0V, S1 : B, S2 : B V_6 = 0V V_6 = 3V			 66 30	 85 40	mA
$-I_{2L}$	Output Leakage Current	V_i = 46V, V_6 = 3V, S1 : B, S2 : A, V_7 = 0V				2	mA

Note (1) : Using min. 7 A schottky diode.
(2) : Guaranteed by design, not 100 % tested in production.

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit	Fig.
SOFT START							
$I_{5\,so}$	Source Current	V_6 = 0V, V_5 = 3V	80	130	150	µA	6b
$I_{5\,si}$	Sink Current	V_6 = 3V, V_5 = 3V	50	70	120	µA	6b
INHIBIT							
V_{6L} V_{6H}	Input Voltage Low Level High Level	V_i = 9V to 46V, V_7 = 0V, S1 : B, S2 : B	– 0.3 2		0.8 5.5	V	6a
$-I_{6L}$ $-I_{6H}$	Input Current with Input Voltage Low Level High Level	V_i = 9V to 46V, V_7 = 0V, S1 : B, S2 : B V_6 = 0.8V V_6 = 2V			 10 3	µA	6a
ERROR AMPLIFIER							
V_{9H}	High Level Output Voltage	V_{10} = 4.7V, I_9 = 100µA, S1 : A, S2 : A	3.5			V	6c
V_{9L}	Low Level Output Voltage	V_{10} = 5.3V, I_9 = 100µA, S1 : A, S2 : E			0.5	V	6c
$I_{9\,si}$	Sink Output Current	V_{10} = 5.3V, S1 : A, S2 : B	100	150		µA	6c
$-I_{9\,so}$	Source Output Current	V_{10} = 4.7V, S1 : A, S2 : D	100	150		µA	6c
I_{10}	Input Bias Current	V_{10} = 5.2V, S1 : B V_{10} = 6.4V, S1 : B, L296P		2 2	10 10	µA µA	6c 6c
G_v	DC Open Loop Gain	V_9 = 1V to 3V, S1 : A, S2 : C	46	55		dB	6c
OSCILLATOR AND PWM COMPARATOR							
$-I_7$	Input Bias Current of PWM Comparator	V_7 = 0.5V to 3.5V			5	µA	6a
$-I_{11}$	Oscillator Source Current	V_{11} = 2V, S1 : A, S2 : B	5			mA	
RESET							
$V_{12\,R}$	Rising Threshold Voltage	V_i = 9V to 46V, S1 : B, S2 : B	V_{ref} -150mV	V_{ref} -100mV	V_{ref} -50mV	V	6d
$V_{12\,F}$	Falling Threshold Voltage		4.75	V_{ref} -150mV	V_{ref} -100mV	V	6d
$V_{13\,D}$	Delay Thershold Voltage	V_{12} = 5.3V, S1 : A, S2 : B	4.3	4.5	4.7	V	6d
$V_{13\,H}$	Delay Threshold Voltage Hysteresis			100		mV	6d
$V_{14\,S}$	Output Saturation Voltage	I_{14} = 16mA, V_{12} = 4.7V, S1, S2 : B			0.4	V	6d
I_{12}	Input Bias Current	V_{12} = 0V to V_{ref}, S1 : B, S2 : B		1	3	µA	6d
$-I_{13\,so}$ $I_{13\,si}$	Delay Source Current Delay Sink Current	V_{13} = 3V, S1 : A, S2 : B V_{12} = 5.3V V_{12} = 4.7V	 70 10	 110	 140	 µA mA	6d
I_{14}	Output Leakage Current	V_i = 46V, V_{12} = 5.3V, S1 : B, S2 : A			100	µA	6d
CROWBAR							
V_1	Input Threshold Voltage	S1 : B	5.5	6	6.4	V	6b
V_{15}	Output Saturation Voltage	V_i = 9V to 46V, V_i = 5.4V, I_{15} = 5mA, S1 : A		0.2	0.4	V	6b
I_1	Input Bias Current	V_1 = 6V, S1 : B			10	µA	6b
$-I_{15}$	Output Source Current	V_i = 9V to 46V, V_1 = 6.5V, V_{15} = 2V, S1 : B	70	100		mA	6b

Figure 4 : Dynamic Test Circuit



C7, C8 : EKR (ROE)
L1 : L = 300 µH at 8 A Core type : MAGNETICS 58930 - A2 MPP
N° turns : 43 Wire Gauge : 1 mm (18 AWG) COGEMA 946044
(*) Minimum suggested value (10 µF) to avoid oscillations. Ripple consideration leads to typical value of 1000 µF or higher.

Figure 5 : PC. Board and Component Layout of the Circuit of Figure 4 (1:1 scale)

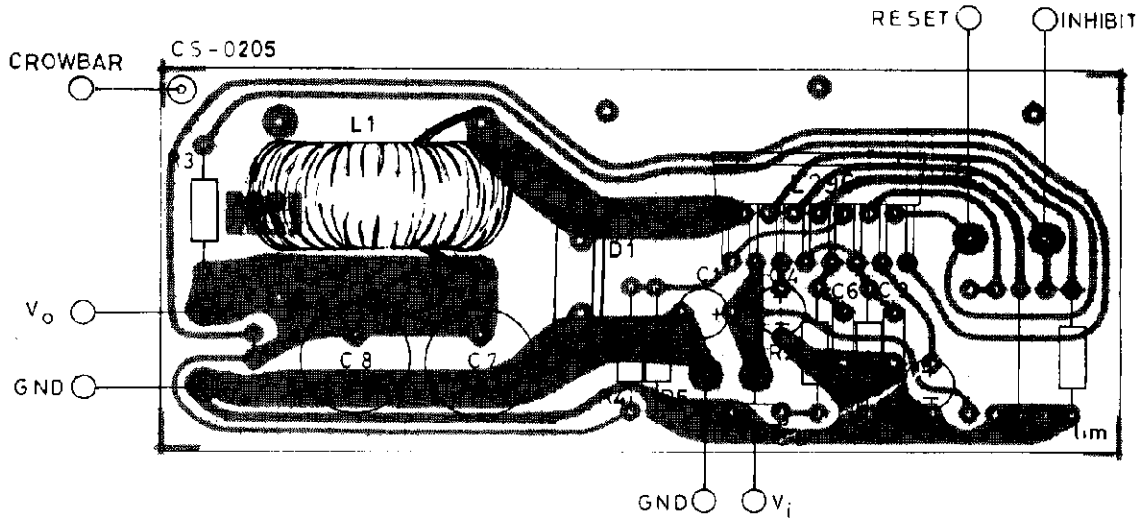


Figure 6 : DC Test Circuits.

Figure 6a.

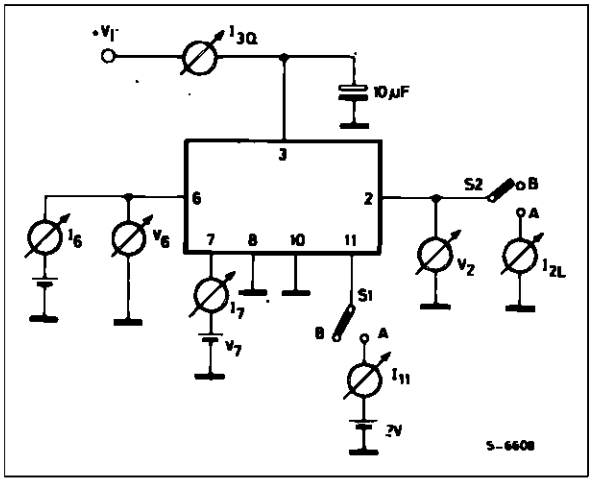


Figure 6b.

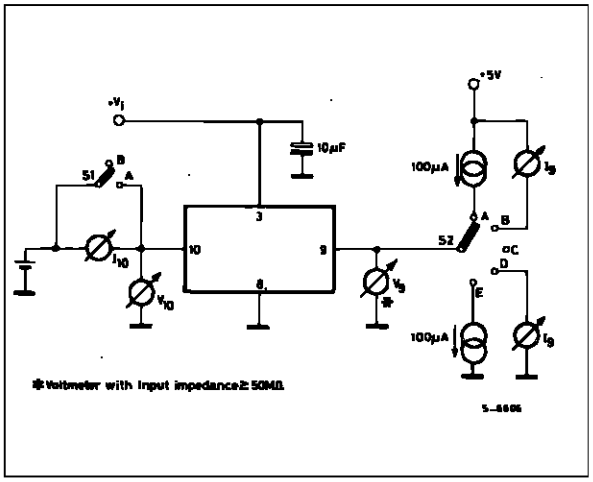


Figure 6c.

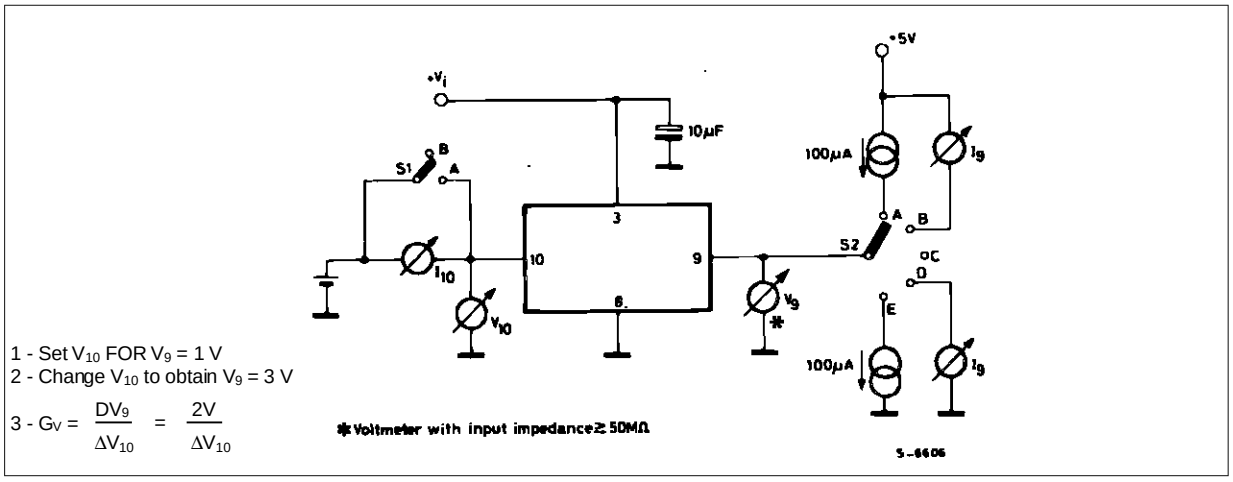


Figure 6d.

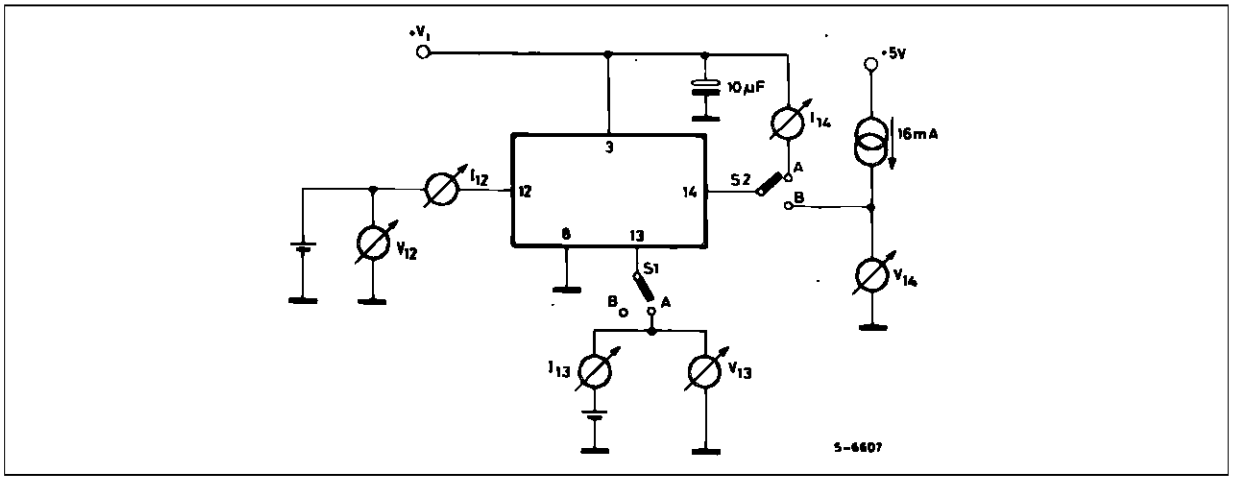


Figure 7 : Quienscent Drain Current vs. Supply Voltage (0 % Duty Cycle - see fig. 6a).

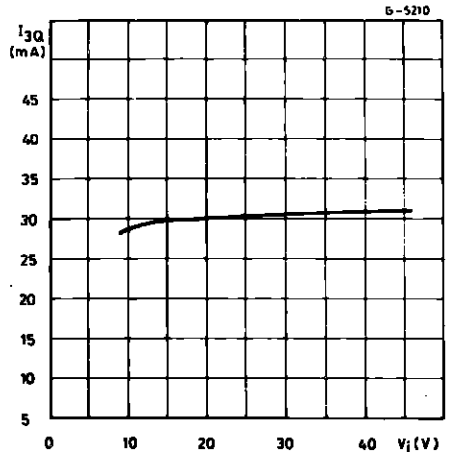


Figure 8 : Quienscent Drain Current vs. Supply Voltage (100 % Duty Cycle see fig. 6a).

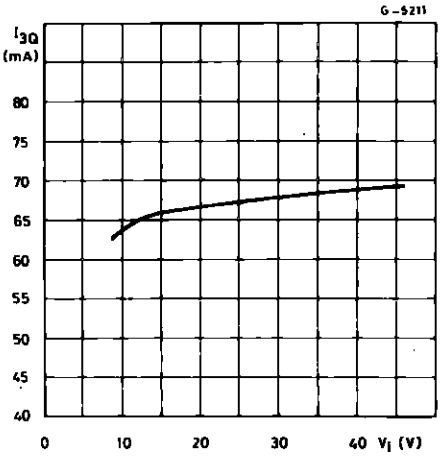


Figure 9 : Quiescent Drain Current vs. Junction Temperature (0 % Duty Cycle - see fig. 6a).

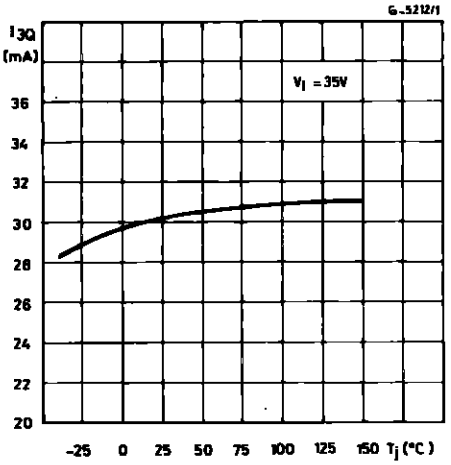


Figure 10 : Quiescent Drain Current vs. Junction Temperature (100 % Duty Cycle - see fig. 6a).

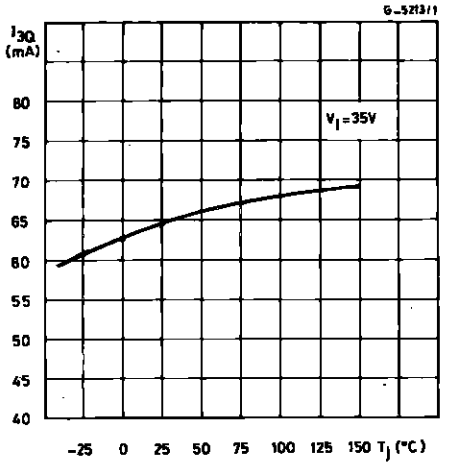


Figure 11 : Reference Voltage (pin 10) vs. V_I (see fig. 4).

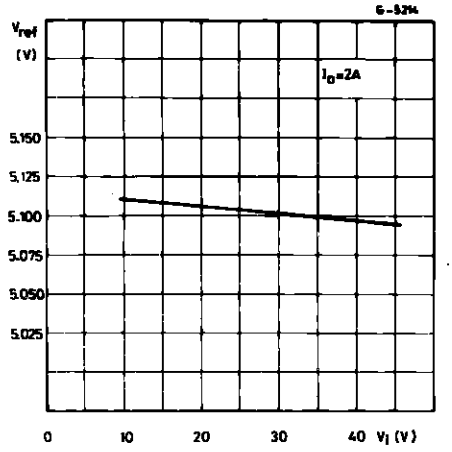


Figure 12 : Reference Voltage (pin 10) vs. Junction Temperature (see fig. 4).

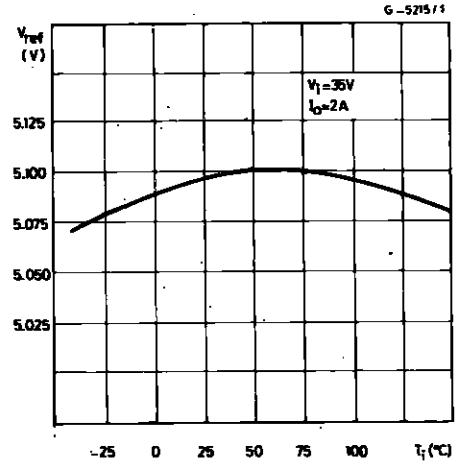


Figure 13 : Open Loop Frequency and Phase Response of Error Amplifier (see fig. 6c).

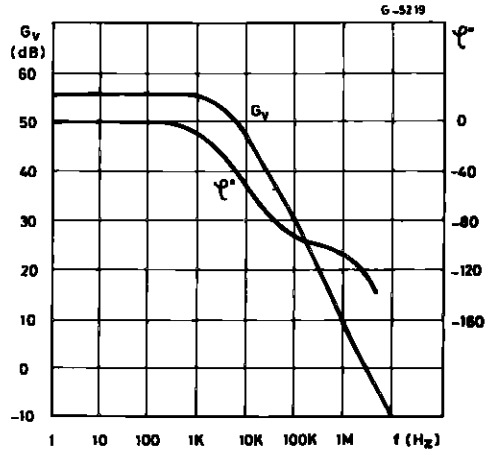


Figure 14 : Switching Frequency vs. Input Voltage (see fig. 4).

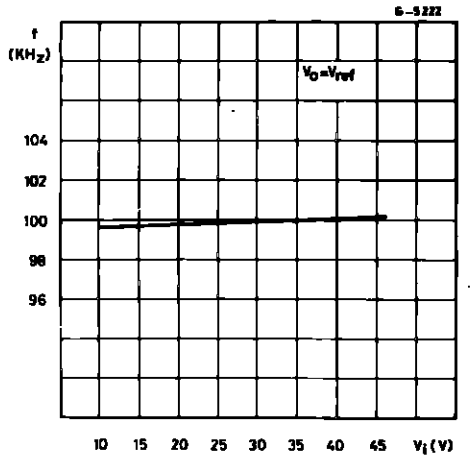


Figure 15 : Switching Frequency vs. Junction Temperature (see fig. 4).

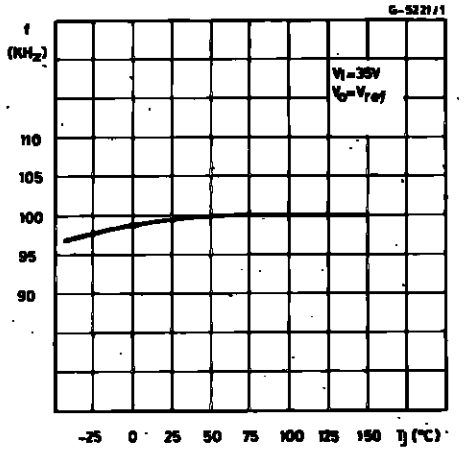


Figure 16 : Switching Frequency vs. R1 (see fig. 4).

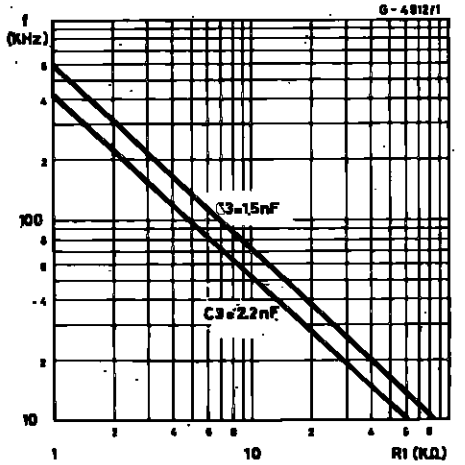


Figure 17 : Line Transient Response (see fig. 4).

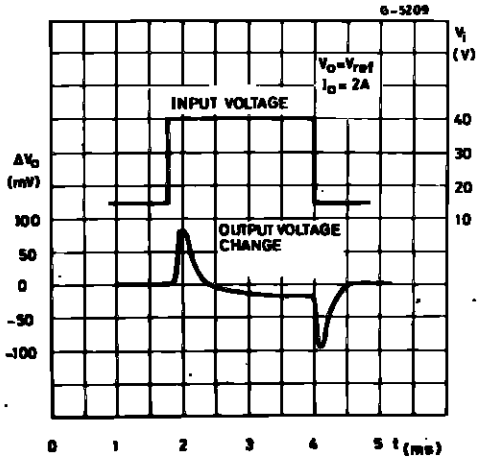


Figure 18 : Load Transient Response (see fig. 4).

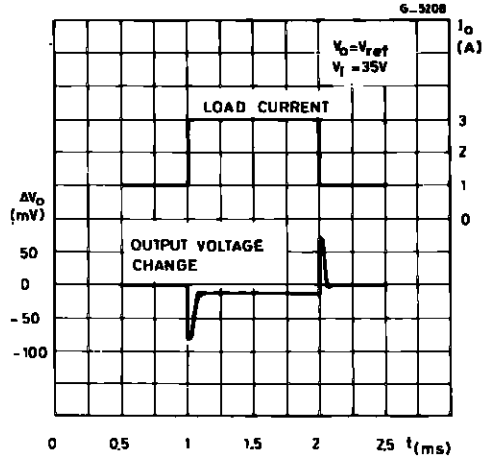


Figure 19 : Supply Voltage Ripple Rejection vs. Frequency (see fig. 4).

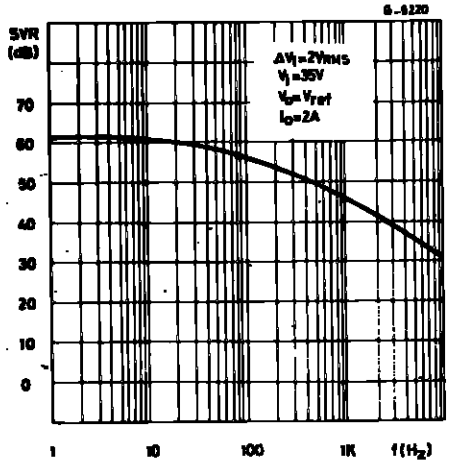


Figure 20 : Dropout Voltage Between Pin 3 and Pin 2 vs. Current at Pin 2.

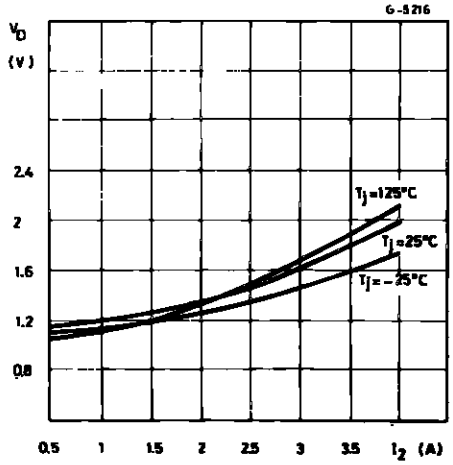


Figure 21 : Dropout Voltage Between Pin 3 and Pin 2 vs. Junction Temperature.

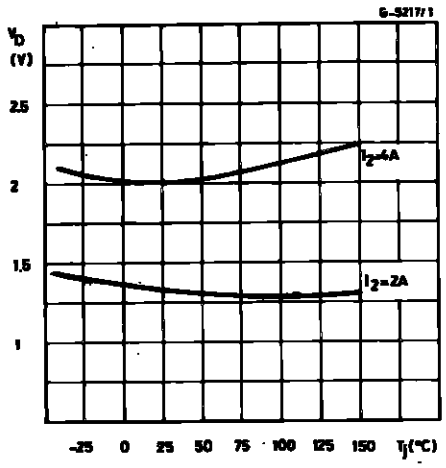


Figure 22 : Power Dissipation Derating Curve.

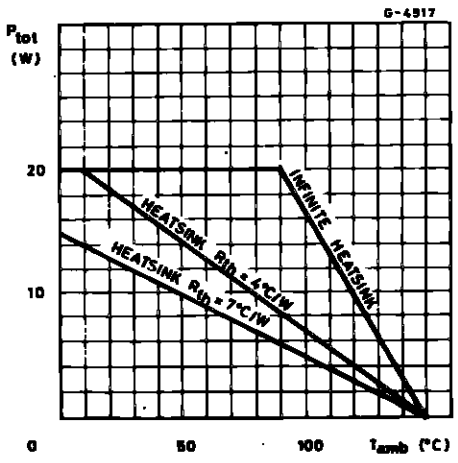


Figure 23 : Power Dissipation (device only) vs. Input Voltage.

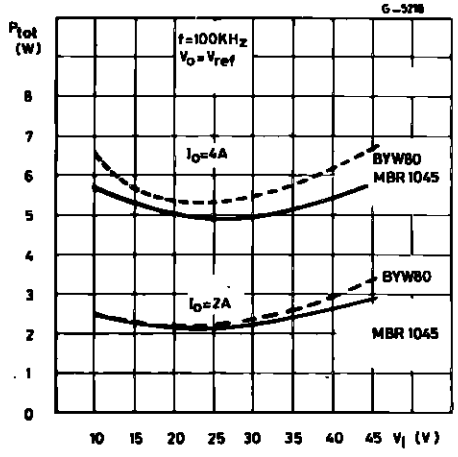


Figure 24 : Power Dissipation (device only) vs. Input voltage.

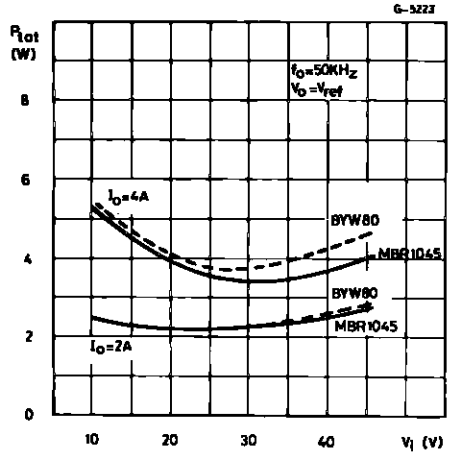


Figure 25 : Power Dissipation (device only) vs. Output Voltage (see fig. 4).

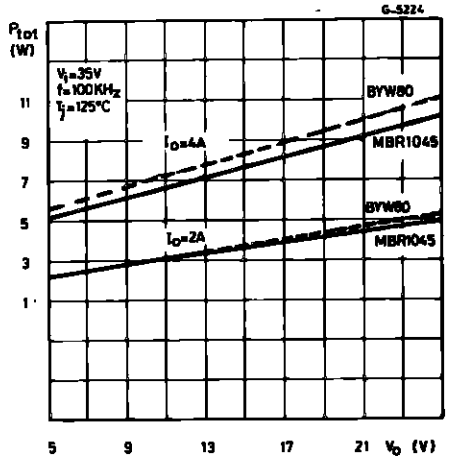


Figure 26 : Power Dissipation (device only) vs. Output Voltage (see fig. 4).

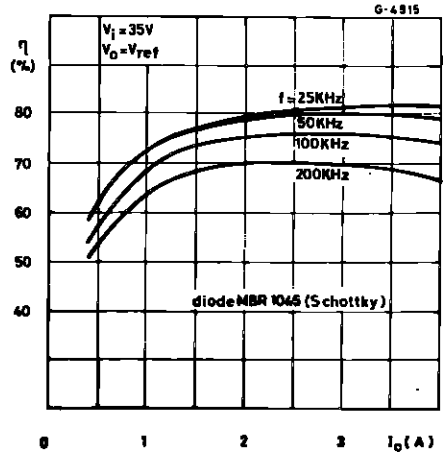


Figure 27 : Voltage and Current Waveforms at Pin 2 (see fig. 4).

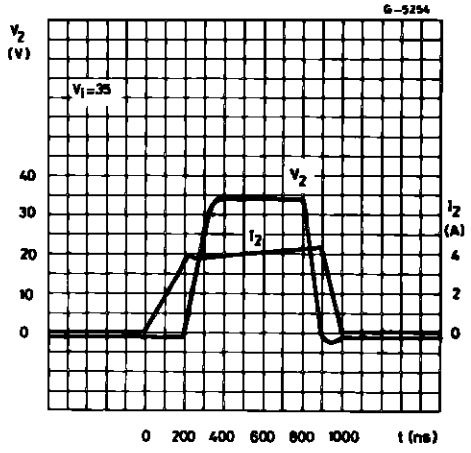


Figure 28 : Efficiency vs. Output Current.

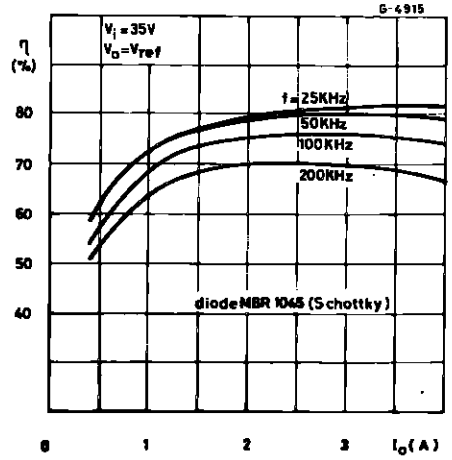


Figure 29 : Efficiency vs. Output Voltage.

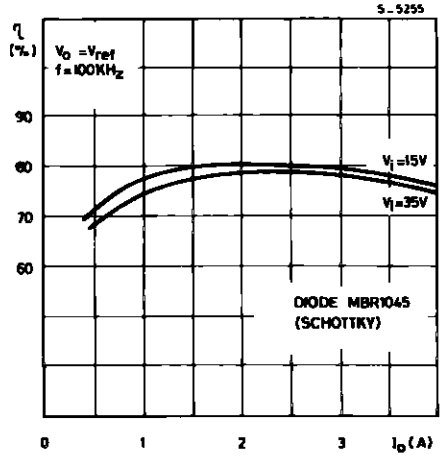


Figure 30 : Efficiency vs. Output Voltage.

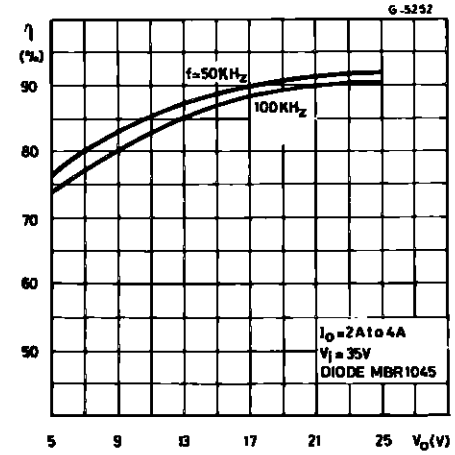


Figure 31 : Current Limiting Threshold vs. $R_{pin\ 4}$ (L296P only).

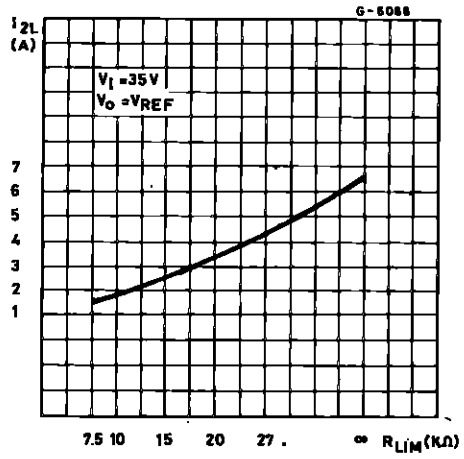


Figure 32 : Current Limiting Threshold vs. Junction Temperature.

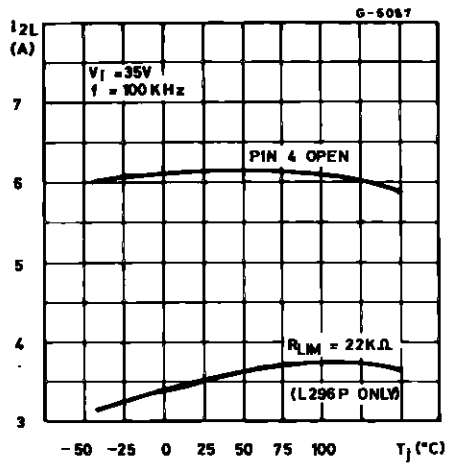
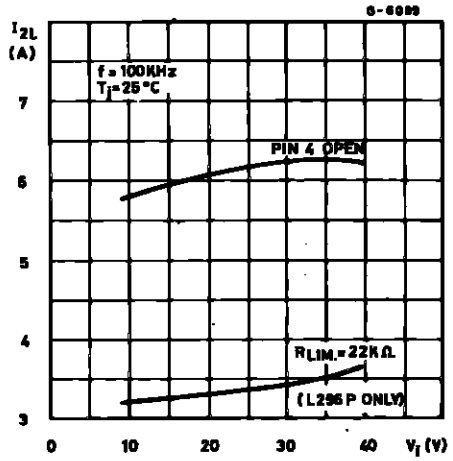
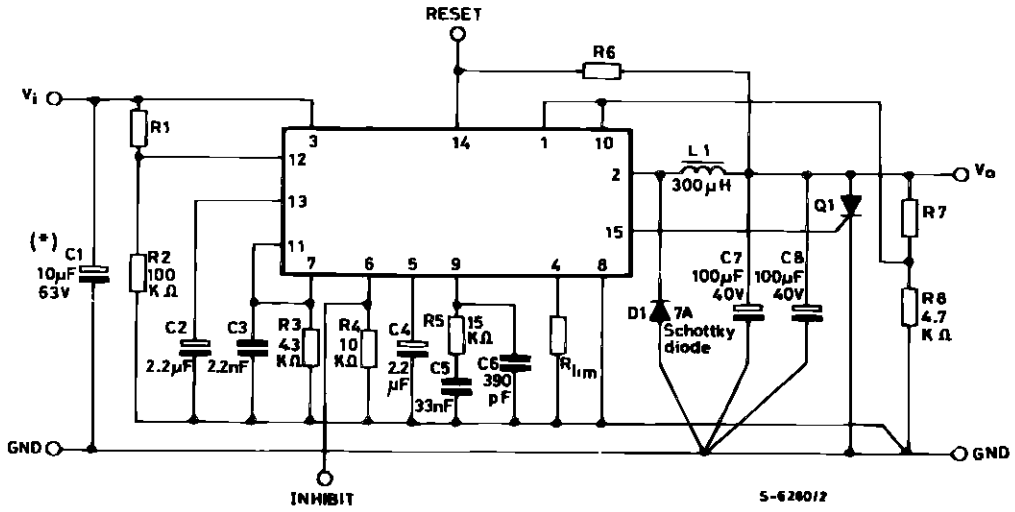


Figure 33 : Current Limiting Threshold vs. Supply Voltage.



APPLICATION INFORMATION

Figure 34 : Typical Application Circuit.



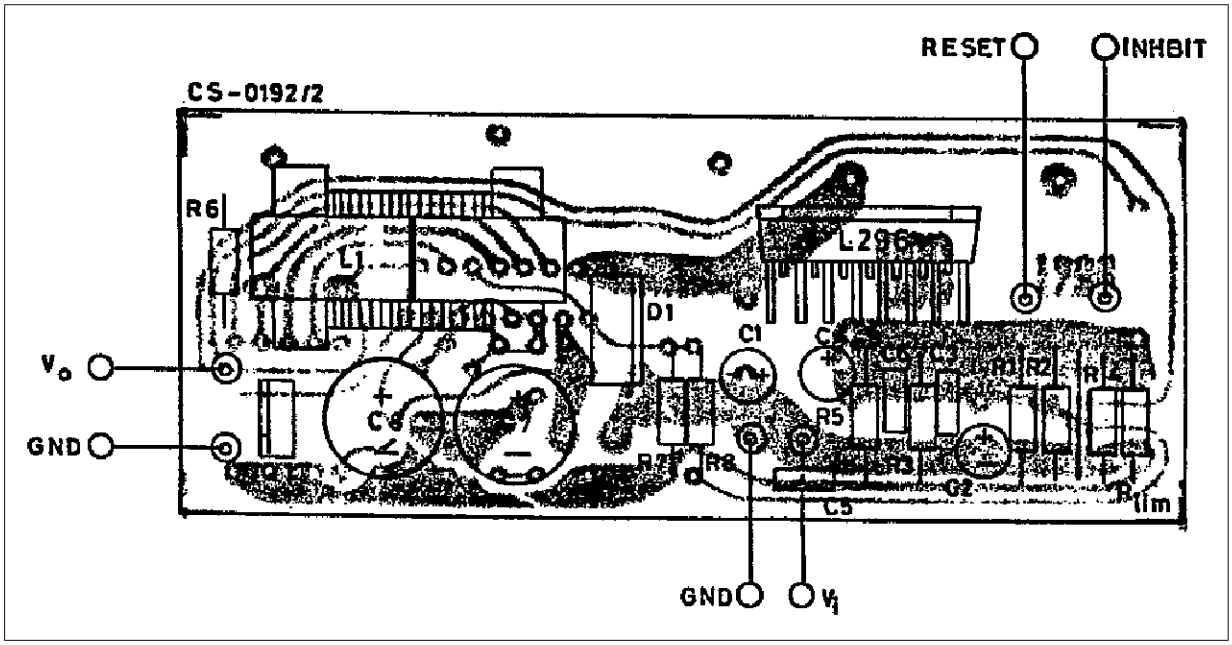
(*) Minimum value (10 µF) to avoid oscillations ; ripple consideration leads to typical value of 1000 µF or higher L1 : 58930 - MPP COGEMA 946044 ; GUP 20 COGEMA 946045

SUGGESTED INDUCTOR (L1)

Core Type	No Turns	Wire Gauge	Air Gap
Magnetics 58930 – A2MPP	43	1.0 mm	–
Thomson GUP 20 x 16 x 7	65	0.8 mm	1 mm
Siemens EC 35/17/10 (B6633& – G0500 – X127)	40	2 x 0.8 mm	–
VOGT 250 µH Toroidal Coil, Part Number 5730501800			

Resistor Values for Standard Output Voltages		
V_0	R8	R7
12 V	4.7 KΩ	6.2 KΩ
15 V	4.7 KΩ	9.1 KΩ
18 V	4.7 KΩ	12 KΩ
24 V	4.7 KΩ	18 KΩ

Figure 35 : P.C. Board and Component Layout of the Circuit of fig. 34 (1:1 scale)



SELECTION OF COMPONENT VALUES (see fig. 34)

Component	Recommended Value	Purpose	Allowed Rage		Notes
			Min.	Max.	
R1 R2	– 100 kΩ	Set Input Voltage Threshold for Reset.	–	220kΩ	R1/R2 $\frac{V_{i\,min}}{5} - 1$ If output voltage is sensed R1 and R2 may be limited and pin 12 connected to pin 10.
R3	4.3 kΩ	Sets Switching Frequency	1 kΩ	100kΩ	
R4	10 kΩ	Pull-down Resistor		22kΩ	May be omitted and pin 6 grounded if inhibit not used.
R5	15 kΩ	Frequency Compensation	10kΩ		
R6		Collector Load For Reset Output	$\frac{V_O}{0.05A}$		Omitted if reset function not used.
R7 R8	– 4.7 kΩ	Divider to Set Output Voltage	– –	– 1kΩ	R7/R8 = $\frac{V_O - V_{REF}}{V_{REF}}$ -
R_{iim}	–	Sets Current Limit Level	7.5kΩ		If R_{iim} is omitted and pin 4 left open the current limit is internally fixed.
C1	10 µF	Stability	2.2µF		
C2	2.2 µF	Sets Reset Delay	–	–	Omitted if reset function not used.
C3	2.2 nF	Sets Switching Frequency	1 nF	3.3nF	
C4	2.2 µF	Soft Start	1 µF	–	Also determines average short circuit current.
C5	33 nF	Frequency Compensation			
C6	390 pF	High Frequency Compensation	–	–	Not required for 5 V operation.
C7, C8 L1	100 µF 300 µH	Output Filter	– 100µH	–	
Q1		Crowbar Protection			The SCR must be able to withstand the peak discharge current of the output capacitor and the short circuit current of the device.
D1		Recirculation Diode			7A Schottky or 35 ns t_{rr} Diode.

Figure 36 : A Minimal 5.1 V Fixed Regulator. Very Few Components are Required.

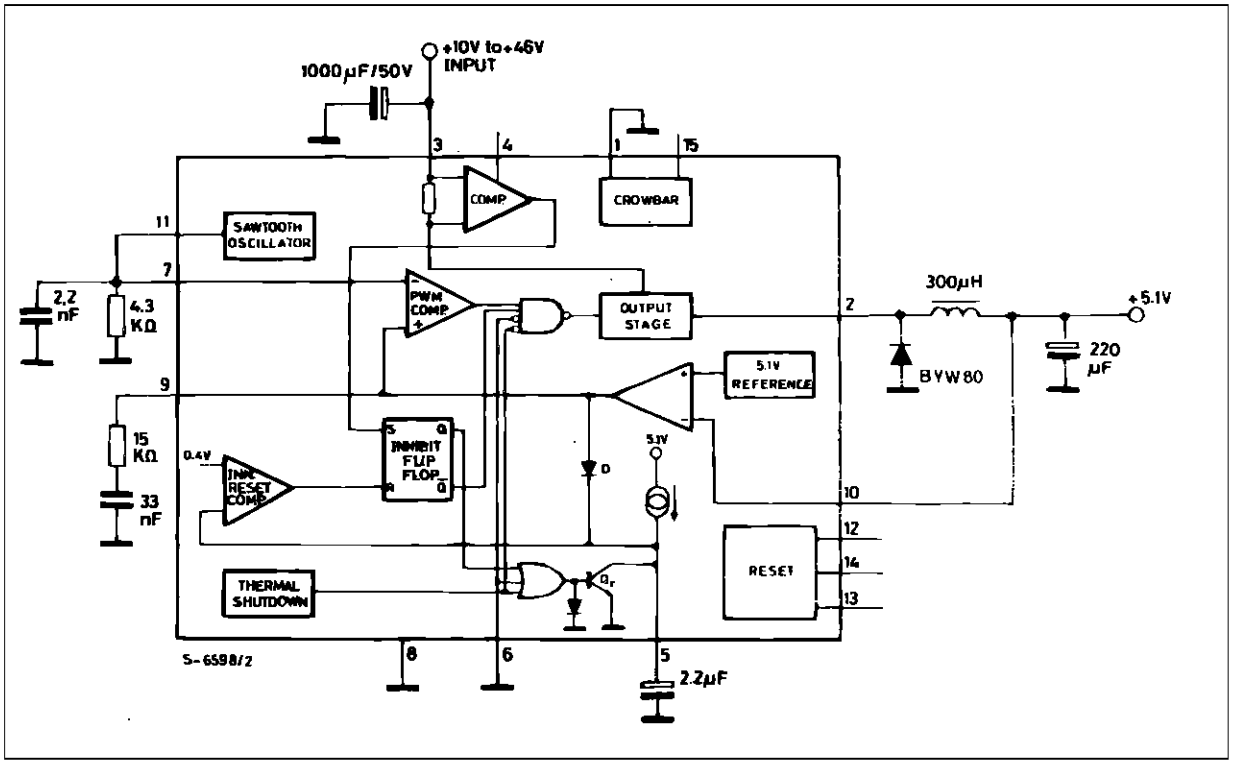


Figure 37 : 12 V/10 A Power Supply.

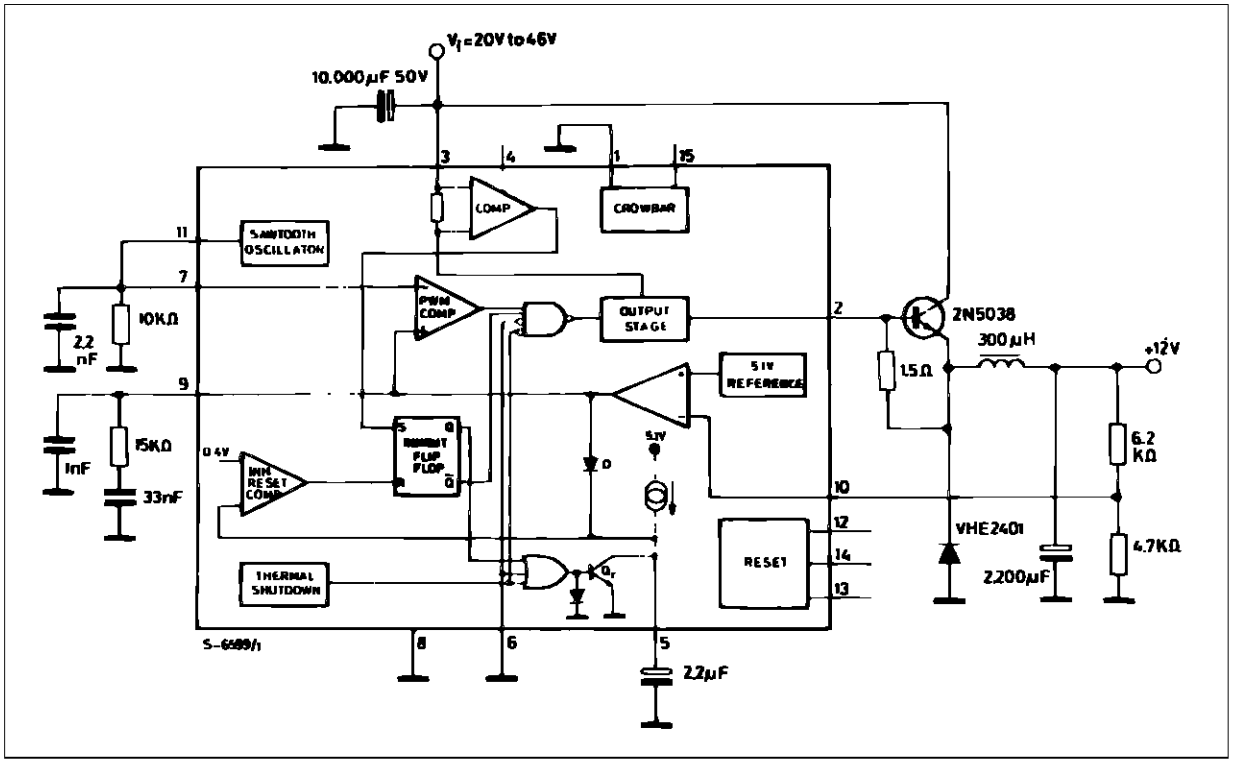
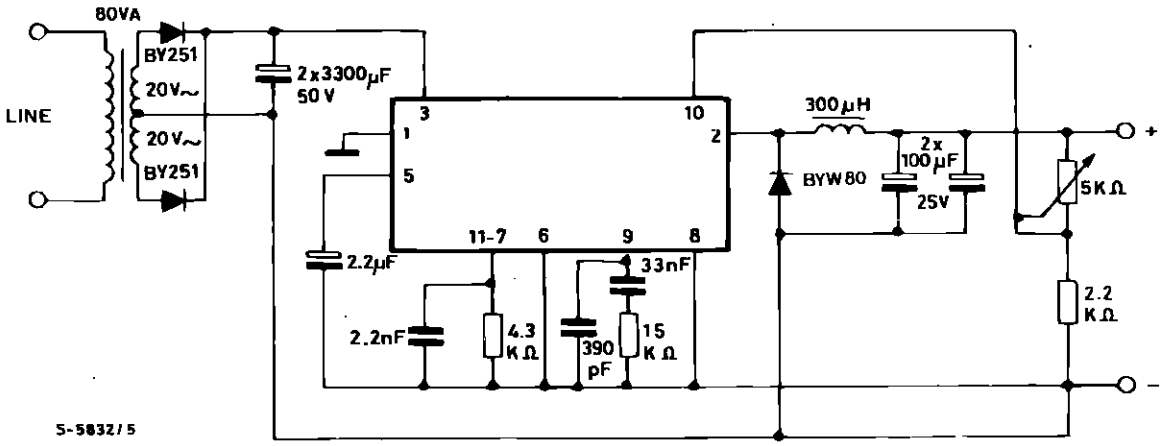
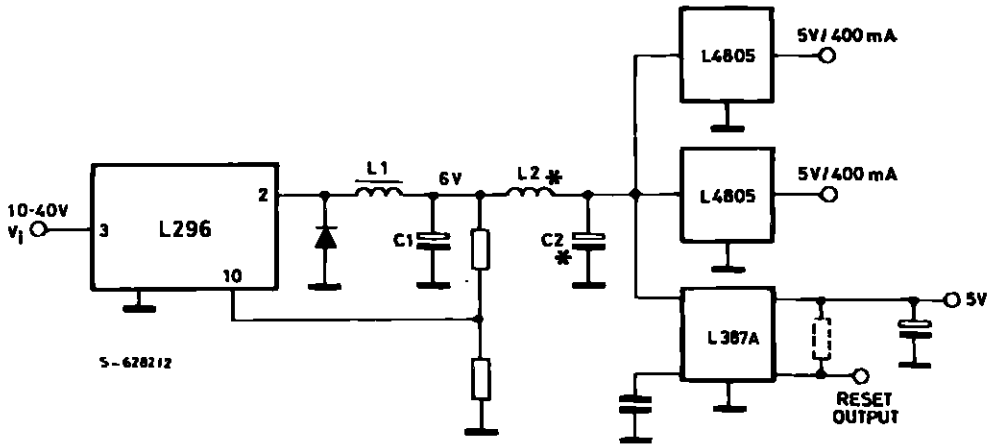


Figure 38 : Programmable Power Supply.



V_o = 5.1 to 15 V
I_o = 4 A max. (min. load current = 100 mA)
ripple ≤ 20 mV
load regulation (1 A to 4 A) = 10 mV (V_o = 5.1 V)
line regulation (220 V ± 15 % and to I_o = 3 A) = 15 mV (V_o = 5.1 V)

Figure 39 : Preregulator for Distributed Supplies.



(*) L2 and C2 are necessary to reduce the switching frequency spikes.

Figure 40 : In Multiple Supplies Several L296s can be Synchronized As Shown.

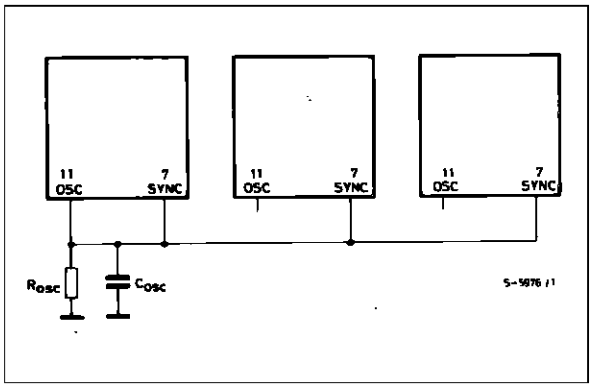


Figure 41 : Voltage Sensing for Remote Load.

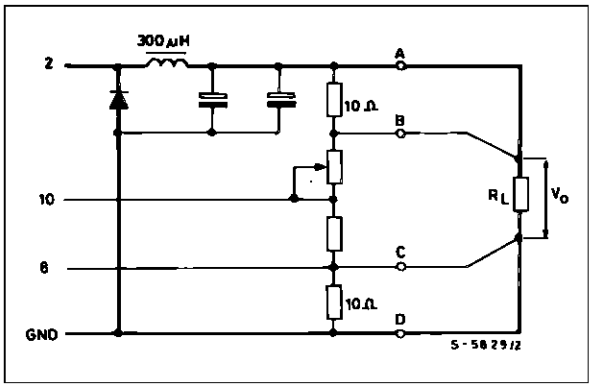


Figure 42 : A 5.1 V/15 V/24 V Multiple Supply. Note the Synchronization of the Three L296s.

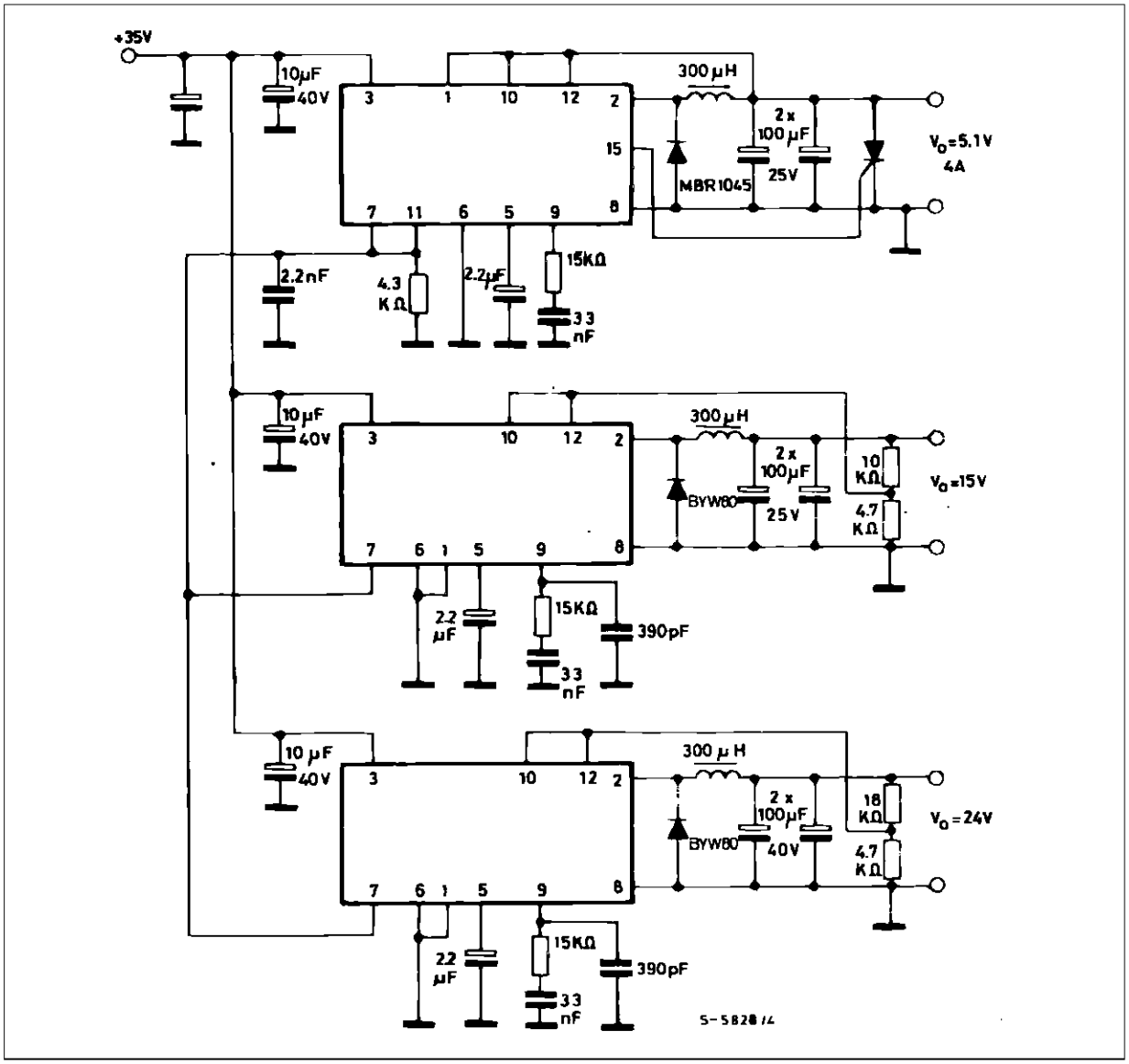
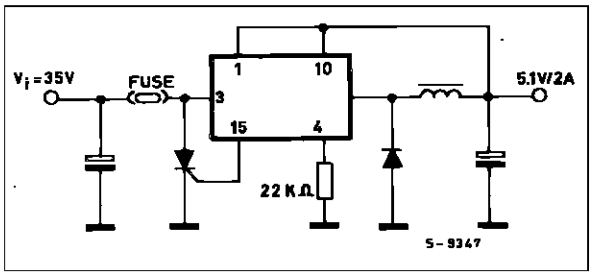


Figure 43 : 5.1V/2A Power Supply using External Limiting Current Resistor and Crow-bar Protection on the Supply Voltage (L296P only)

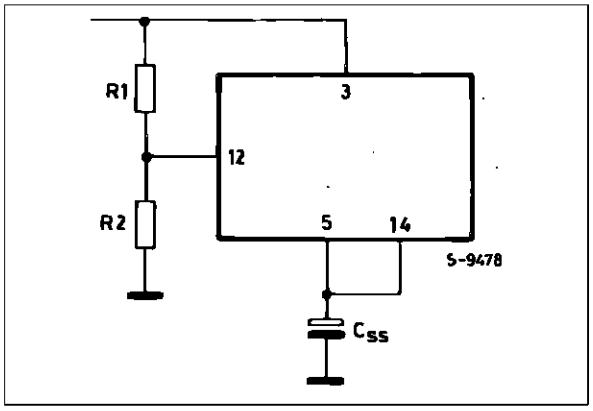


SOFT-START AND REPETITIVE POWER-ON

When the device is repetitively powered-on, the soft-start capacitor, C_{SS}, must be discharged rapidly to ensure that each start is "soft". This can be achieved economically using the reset circuit, as shown in Figure 44.

In this circuit the divider R1, R2 connected to pin 12 determines the minimum supply voltage, below which the open collector transistor at the pin 14 output discharges C_{SS}.

Figure 44

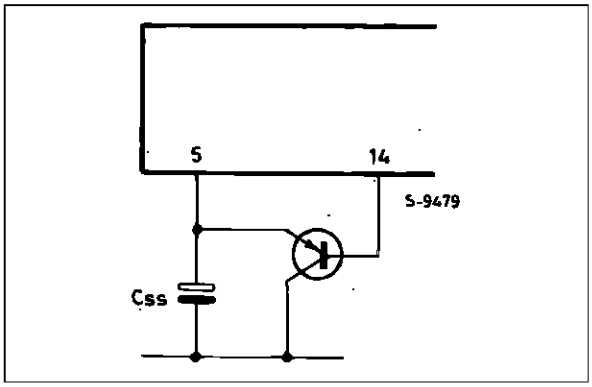


The approximate discharge times obtained with this circuit are :

CSS (µF)	tDIS (µs)
2.2	200
4.7	300
10	600

If these times are still too long, an external PNP transistor may be added, as shown in Figure 45 ; with this circuit discharge times of a few microseconds may be obtained.

Figure 45



HOW TO OBTAIN BOTH RESET AND POWER FAIL

Figure 46 illustrates how it is possible to obtain at the same time both the power fail and reset functions simply by adding one diode (D) and one resistor (R).

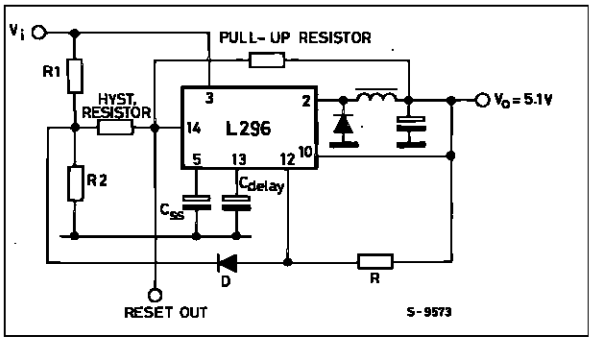
In this case the Reset delay time (pin 13) can only start when the output voltage is $V_O \geq V_{REF}$ - 100mV and the voltage accross R2 is higher than 4.5V.

With the hysteresis resistor it is possible to fix the input pin 12 hysteresis in order to increase immunity to the 100Hz ripple present on the supply voltage.

Moreover, the power fail and reset delay time are automatically locked to the soft-start. Soft-start and delayed reset are thus two sequential functions.

The hysteresis resistor should be In the range of aboit 100kΩ and the pull-up resistor of 1 to 2.2kΩ.

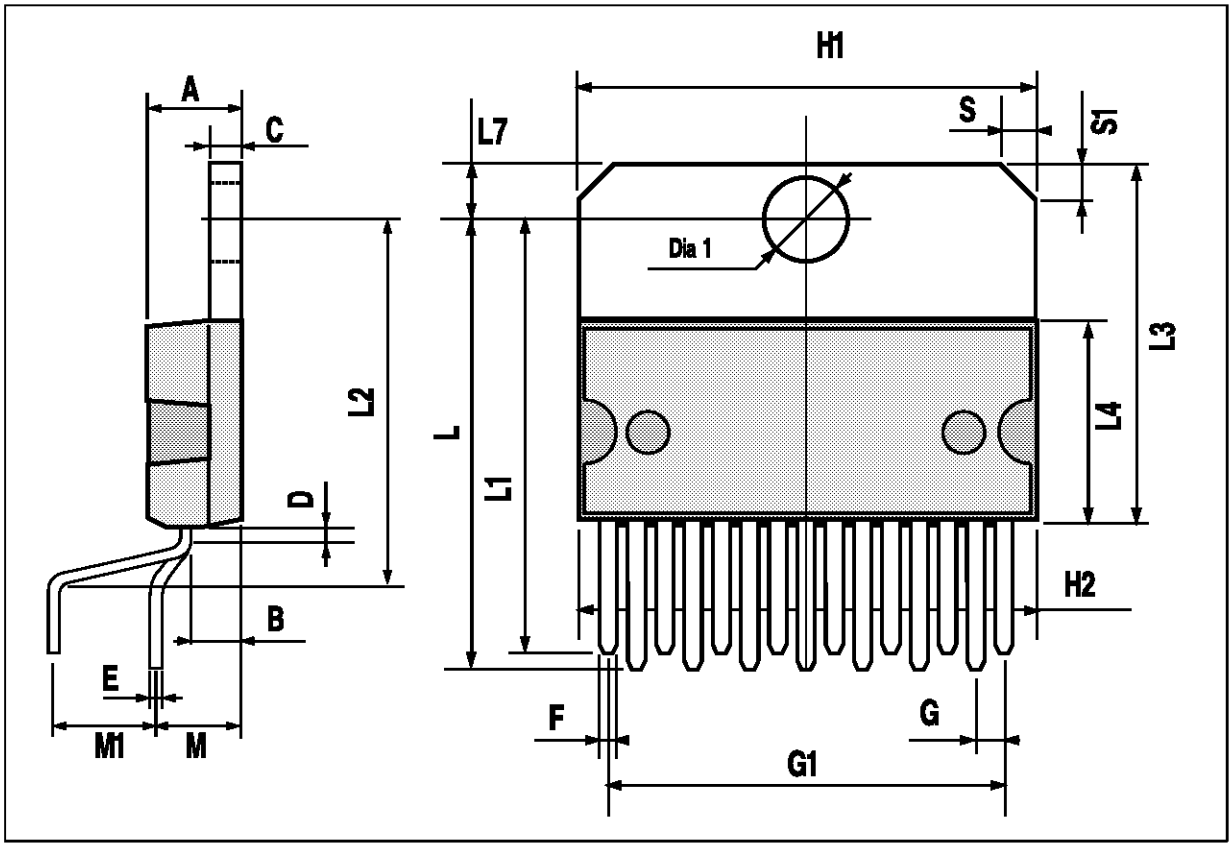
Figure 46



MULTIWATT15 VERTICAL PACKAGE MECHANICAL DATA

Dimensions	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			5			0.197
B			2.65			0.104
C			1.6			0.063
D		1			0.039	
E	0.49		0.55	0.019		0.022
F	0.66		0.75	0.026		0.030
G	1.14	1.27	1.4	0.045	0.050	0.055
G1	17.57	17.78	17.91	0.692	0.700	0.705
H1	19.6			0.772		
H2			20.2			0.795
L	22.1		22.6	0.870		0.890
L1	22		22.5	0.866		0.886
L2	17.65		18.1	0.695		0.713
L3	17.25	17.5	17.75	0.679	0.689	0.699
L4	10.3	10.7	10.9	0.406	0.421	0.429
L7	2.65		2.9	0.104		0.114
M	4.2	4.3	4.6	0.165	0.169	0.181
M1	4.5	5.08	5.3	0.177	0.200	0.209
S	1.9		2.6	0.075		0.102
S1	1.9		2.6	0.075		0.102
Dia. 1	3.65		3.85	0.144		0.152

MUL15V.TBL



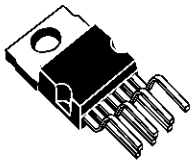
PMMUL15V.EPS

SGS-THOMSON MICROELECTRONICS

L4960

2.5A POWER SWITCHING REGULATOR

- 2.5A OUTPUT CURRENT
- 5.1V TO 40V OPUTPUT VOLTAGE RANGE
- PRECISE (± 2%) ON-CHIP REFERENCE
- HIGH SWITCHING FREQUENCY
- VERY HIGH EFFICIENCY (UP TO 90%)
- VERY FEW EXTERNAL COMPONENTS
- SOFT START
- INTERNAL LIMITING CURRENT
- THERMAL SHUTDOWN



HEPTAWATT

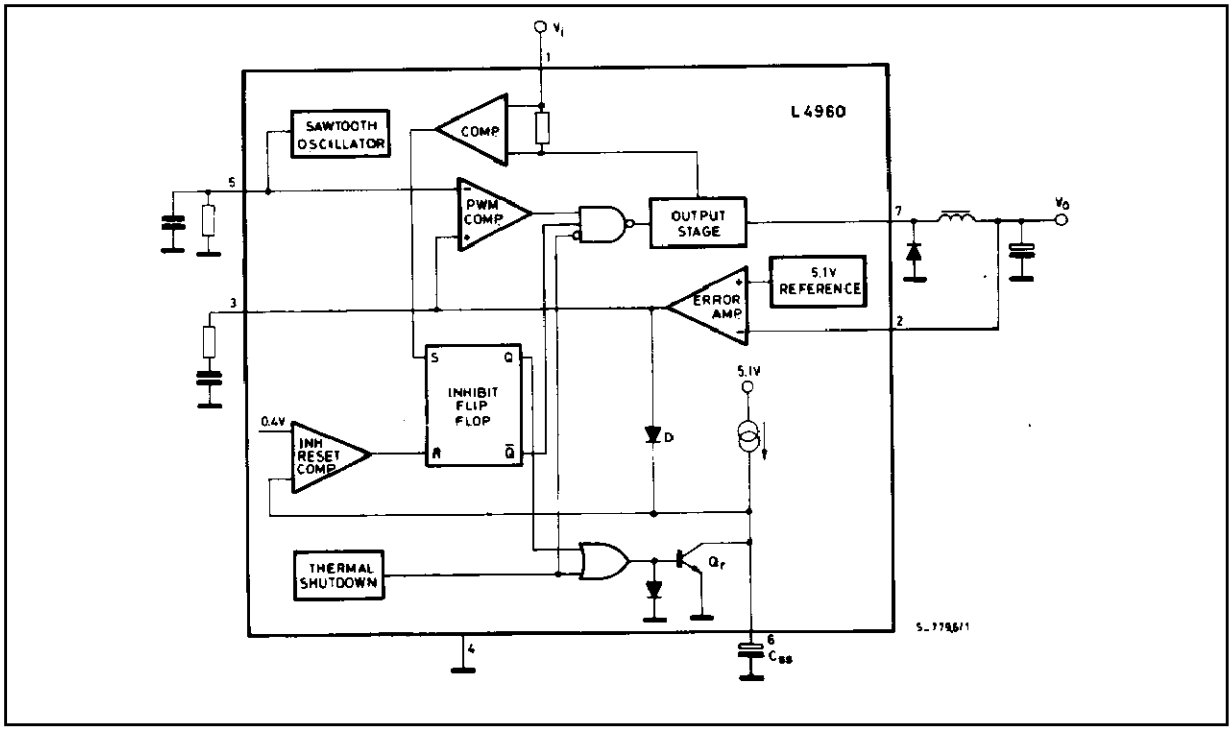
ORDERING NUMBERS: L4960 (Vertical)
L4960H (Horizontal)

DESCRIPTION

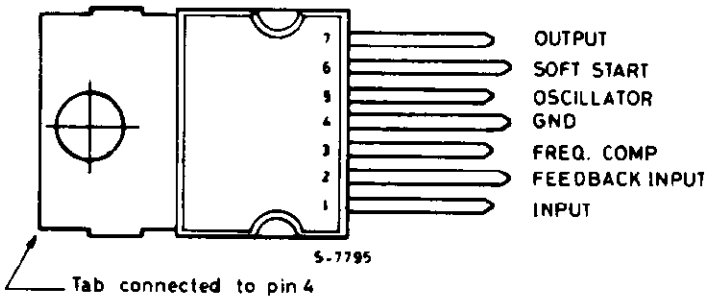
The L4960 is a monolithic power switching regulator delivering 2.5A at a voltage variable from 5V to 40V in step down configuration.
Features of the device include current limiting, soft start, thermal protection and 0 to 100% duty cycle for continuous operation mode.

The L4960 is mounted in a Heptawatt plastic power package and requires very few external components.
Efficient operation at switching frequencies up to 150KHz allows a reduction in the size and cost of external filter components.

BLOCK DIAGRAM



PIN CONNECTION (Top view)



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_1	Input voltage	50	V
$V_1 - V_7$	Input to output voltage difference	50	V
V_7	Negative output DC voltage	-1	V
	Negative output peak voltage at t = 0.1µs; f = 100KHz	-5	V
V_3, V_6	Voltage at pin 3 and 6	5.5	V
V_2	Voltage at pin 2	7	V
I_3	Pin 3 sink current	1	mA
I_5	Pin 5 source current	20	mA
P_{tot}	Power dissipation at $T_{case} \leq 90°C$	15	W
T_j, T_{stg}	Junction and storage temperature	-40 to 150	°C

PIN FUNCTIONS

N°	NAME	FUNCTION
1	SUPPLY VOLTAGE	Unregulated voltage input. An internal regulator powers the internal logic.
2	FEEDBACK INPUT	The feedback terminal of the regulation loop. The output is connected directly to this terminal for 5.1V operation; it is connected via a divider for higher voltages.
3	FREQUENCY COMPENSATION	A series RC network connected between this terminal and ground determines the regulation loop gain characteristics.
4	GROUND	Common ground terminal.
5	OSCILLATOR	A parallel RC network connected to this terminal determines the switching frequency.
6	SOFT START	Soft start time constant. A capacitor is connected between this terminal and ground to define the soft start time constant. This capacitor also determines the average short circuit output current.
7	OUTPUT	Regulator output.

THERMAL DATA

Symbol	Parameter		Value	Unit
$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max	4	°C/W
$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	50	°C/W

ELECTRICAL CHARACTERISTICS (Refer to the test circuit, T_j = 25 °C, V_i = 35V, unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
DYNAMIC CHARACTERISTICS						
V_o	Output voltage range	V_i = 46V I_o = 1A	V_{ref}		40	V
V_i	Input voltage range	$V_o = V_{ref}$ to 36V I_o = 2.5A	9		46	V
ΔV_o	Line regulation	V_i = 10V to 40V $V_o = V_{ref}$ I_o = 1A		15	50	mV
ΔV_o	Load regulation	$V_o = V_{ref}$ I_o = 0.5A to 2A		10	30	mV
V_{ref}	Internal reference voltage (pin 2)	V_i = 9V to 46V I_o = 1A	5	5.1	5.2	V
$\frac{\Delta V_{ref}}{\Delta T}$	Average temperature coefficient of refer voltage	T_j = 0°C to 125°C I_o = 1A		0.4		mV/°C
V_d	Dropout voltage	I_o = 2A		1.4	3	V
I_{om}	Maximum operating load current	V_i = 9V to 46V $V_o = V_{ref}$ to 36V	2.5			A
I_{7L}	Current limiting threshold (pin 7)	V_i = 9V to 46V $V_o = V_{ref}$ to 36V	3		4.5	A
I_{SH}	Input average current	V_i = 46V; output short-circuit		30	60	mA
η	Efficiency	f = 100KHz $V_o = V_{ref}$		75		%
		I_o = 2A V_o = 12V		85		%
SVR	Supply voltage ripple rejection	$\Delta V_i = 2V_{rms}$ f_{ripple} = 100Hz $V_o = V_{ref}$ Io = 1A	50	56		dB
f	Switching frequency		85	100	115	KHz
$\frac{\Delta f}{\Delta V_i}$	Voltage stability of switching frequency	V_i = 9V to 46V		0.5		%
$\frac{\Delta f}{\Delta T_j}$	Temperature stability of switching frequency	T_j = 0°C to 125°C		1		%
f_{max}	Maximum operating switching frequency	$V_o = V_{ref}$ I_o = 2A	120	150		KHz
T_{sd}	Thermal shutdown junction temperature			150		°C

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
DC CHARACTERISTICS							
I_{1Q}	Quiescent drain current	100% duty cycle pins 5 and 7 open	V_i = 46V		30	40	mA
		0% duty cycle			15	20	mA
$-I_{7L}$	Output leakage current	0% duty cycle				1	mA
SOFT START							
I_{6SO}	Source current			100	140	180	µA
I_{6SI}	Sink current			50	70	120	µA
ERROR AMPLIFIER							
V_{3H}	High level output voltage	V_2 = 4.7V	I_3 = 100µA	3.5			V
V_{3L}	Low level output voltage	V_2 = 5.3V	I_3 = 100µA			0.5	V
I_{3SI}	Sink output current	V_2 = 5.3V		100	150		µA
$-I_{3SO}$	Source output current	V_2 = 4.7V		100	150		µA
I_2	Input bias current	V_2 = 5.2V			2	10	µA
G_v	DC open loop gain	V_3 = 1V to 3V		46	55		dB
OSCILLATOR							
$-I_5$	Oscillator source current			5			mA

CIRCUIT OPERATION (refer to the block diagram)

The L4960 is a monolithic stepdown switching regulator providing output voltages from 5.1V to 40V and delivering 2.5A.

The regulation loop consists of a sawtooth oscillator, error amplifier, comparator and the output stage. An error signal is produced by comparing the output voltage with a precise 5.1V on-chip reference (zener zap trimmed to ± 2%).

This error signal is then compared with the sawtooth signal to generate the fixed frequency pulse width modulated pulses which drive the output stage.

The gain and frequency stability of the loop can be adjusted by an external RC network connected to pin 3. Closing the loop directly gives an output voltage of 5.1V. Higher voltages are obtained by inserting a voltage divider.

Output overcurrents at switch on are prevented by the soft start function. The error amplifier output is initially clamped by the external capacitor C_{SS} and allowed to rise, linearly, as this capacitor is charged by a constant current source. Output overload protection is provided in the form of a current limiter. The load current is sensed by an internal metal resistor connected to a comparator. When the load current exceeds a preset threshold this comparator sets a flip flop which disables the output stage and discharges the soft start capacitor. A second comparator resets the flip flop when the voltage across the soft start capacitor has fallen to 0.4V.

The output stage is thus re-enabled and the output voltage rises under control of the soft start network. If the overload condition is still present the limiter will trigger again when the threshold current is reached. The average short circuit current is limited to a safe value by the dead time introduced by the soft start network. The thermal overload circuit disables circuit operation when the junction temperature reaches about 150°C and has hysteresis to prevent unstable conditions.

Figure 1. Soft start waveforms

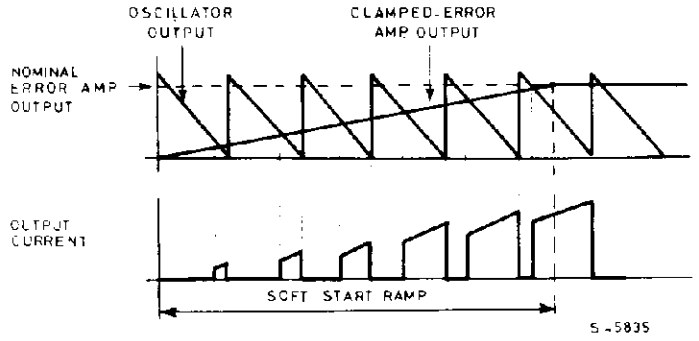


Figure 2. Current limiter waveforms

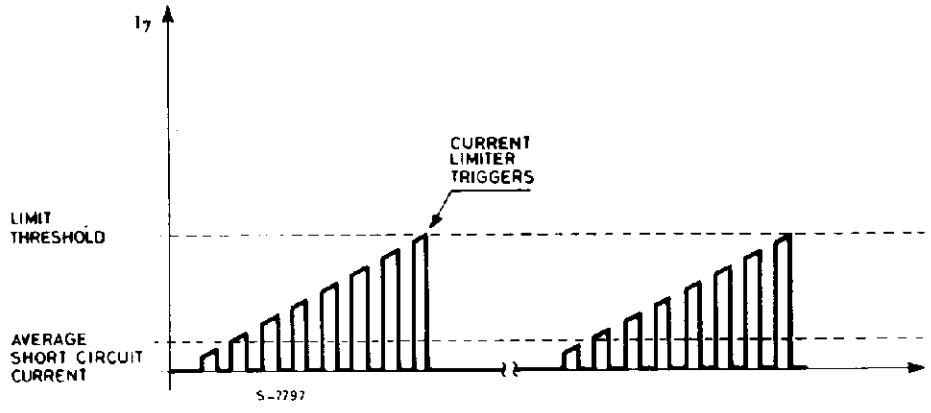
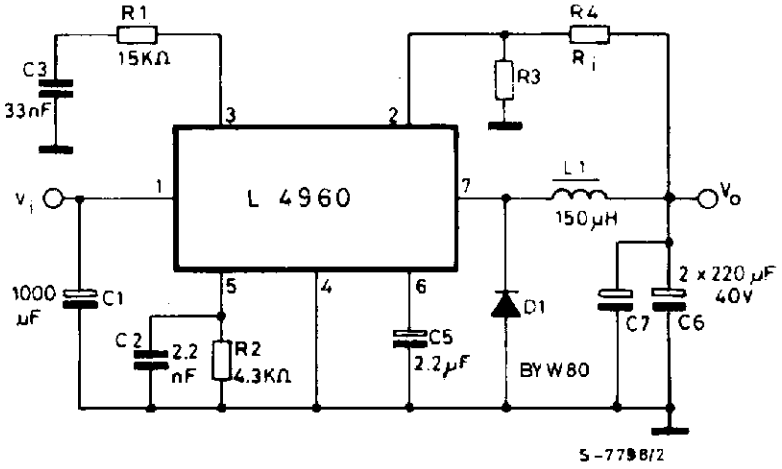


Figure 3. Test and application circuit



C6, C7: EKR (ROE)
L1 = 150µH at 5A (COGEMA 946042)
CORE TYPE: MAGNETICS 58206-A2 MPP
N° TURNS 45, WIRE GAUGE: 0.8mm (20 AWG)

Figure 4. Quiescent drain current vs. supply voltage (0% duty cycle)

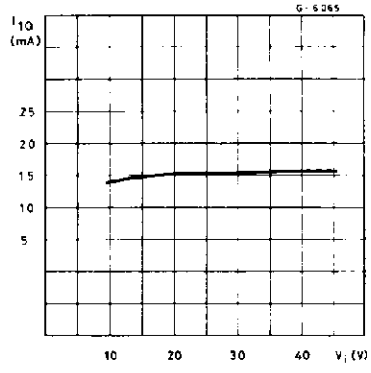


Figure 5. Quiescent drain current vs. supply voltage (100% duty cycle)

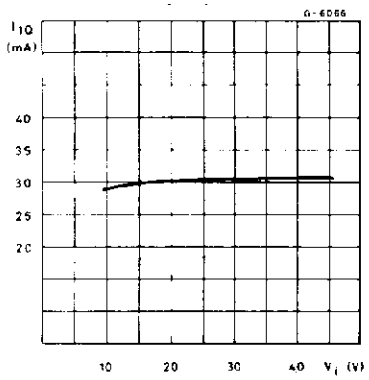


Figure 6. Quiescent drain current vs. junction temperature (0% duty cycle)

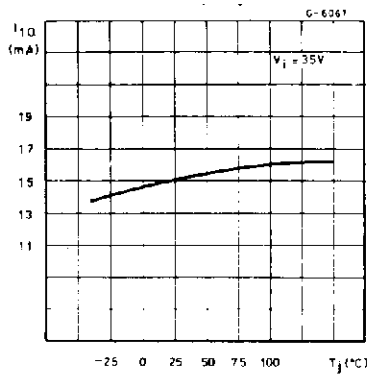


Figure 7. Quiescent drain current vs. junction temperature (100% duty cycle)

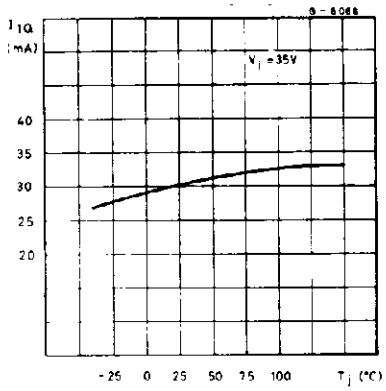


Figure 8. Reference voltage (pin 2) vs. V_i

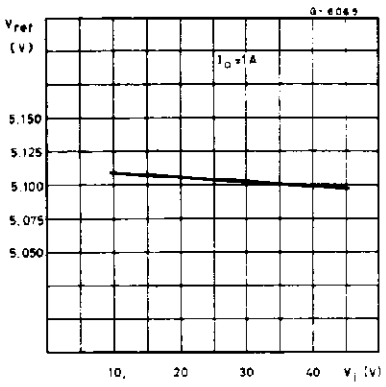


Figure 9. Reference voltage versus junction temperature (pin 2)

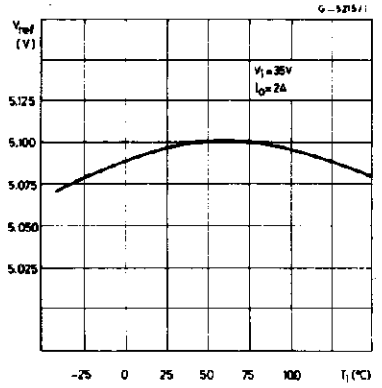


Figure 10. Open loop frequency and phase responde of error amplifier

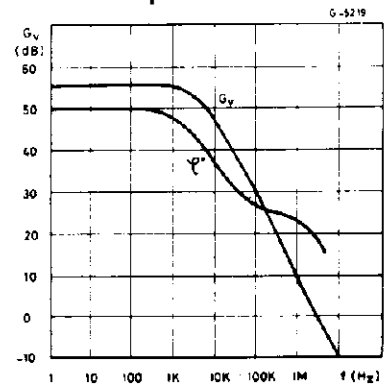


Figure 11. Switching frequency vs. input voltage

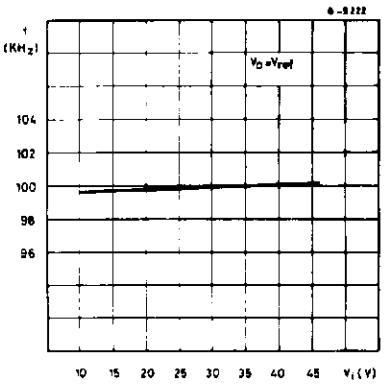


Figure 12. Switching frequency vs. junction temperature

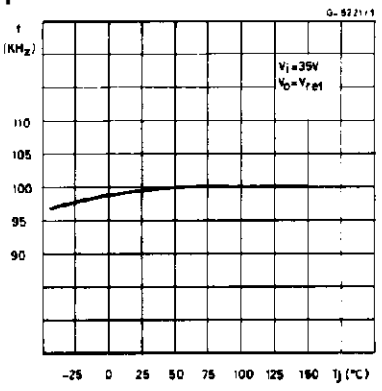


Figure 13. Switching frequency vs. R2 (see test circuit)

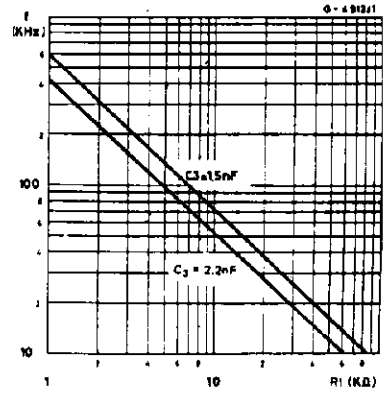


Figure 14. Line transient response

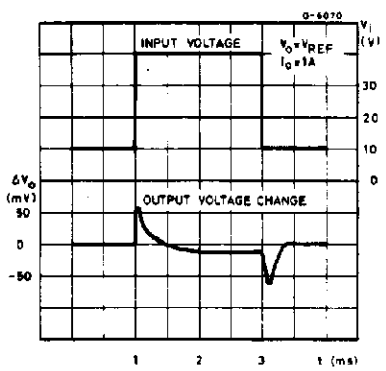


Figure 15. Load transient response

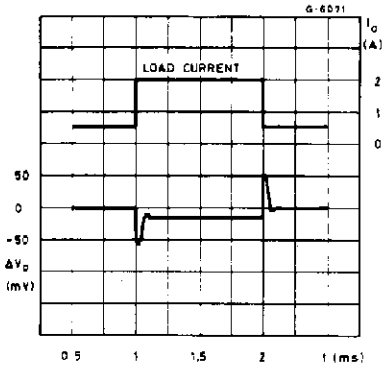


Figure 16. Supply voltage ripple rejection vs. frequency

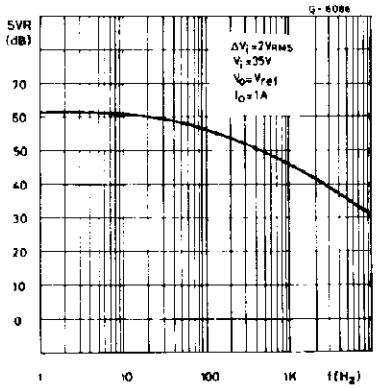


Figure 17. Dropout voltage between pin 1 and pin 7 vs. current at pin 7

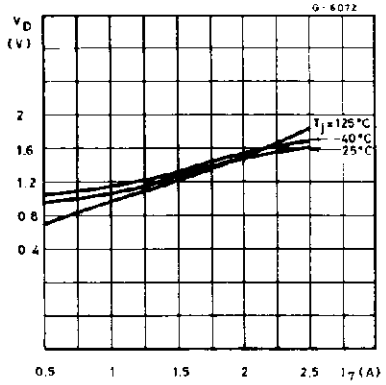


Figure 18. Dropout voltage between pin 1 and 7 vs. junction temperature

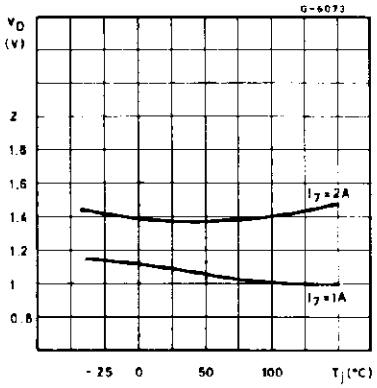


Figure 19. Power dissipation derating curve

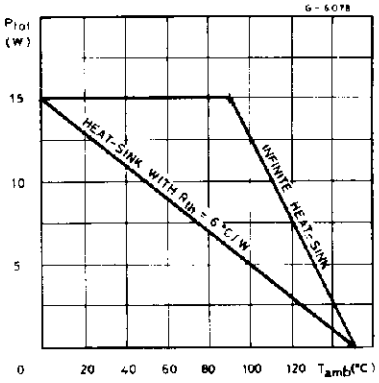


Figure 20. Efficiency vs. output current

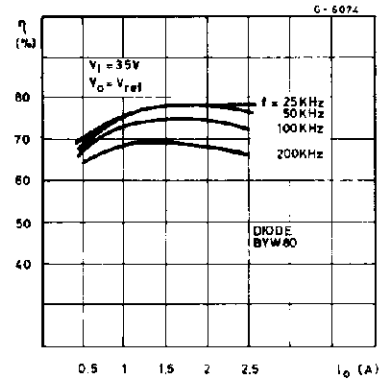


Figure 21. Efficiency vs. output current

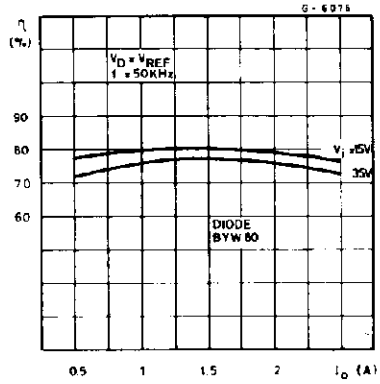


Figure 22. Efficiency vs. output current

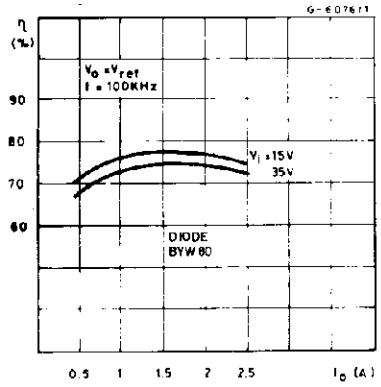
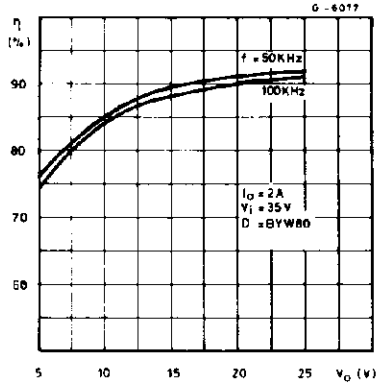
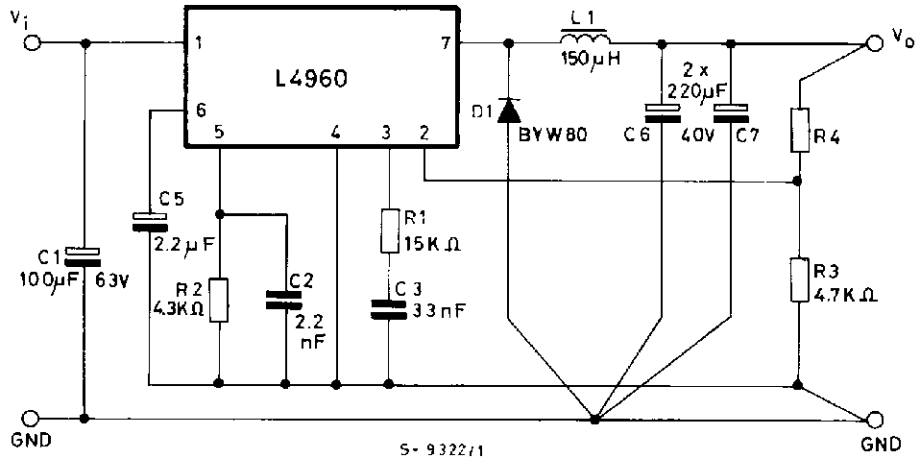


Figure 23. Efficiency vs. output voltage



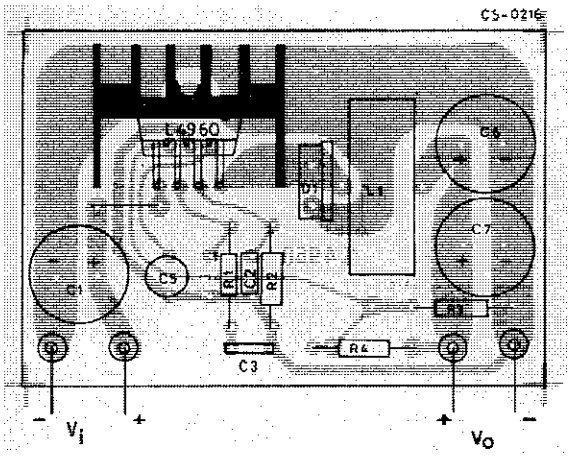
APPLICATION INFORMATION

Figure 24. Typical application circuit



C_1, C_6, C_7: EKR (ROE)
D_1: BYW80 OR 5A SCHOTTKY DIODE
SUGGESTED INDUCTOR: L_1 = 150µH at 5A
CORE TYPE: MAGNETICS 58206 - A2 - MPP
N° TURNS: 45, WIRE GAUGE: 0.8mm (20 AWG), COGEMA 946042
U15/GUP15: N° TURNS: 60, WIRE GAUGE: 0.8mm (20 AWG), AIR GAP: 1mm, COGEMA 969051.

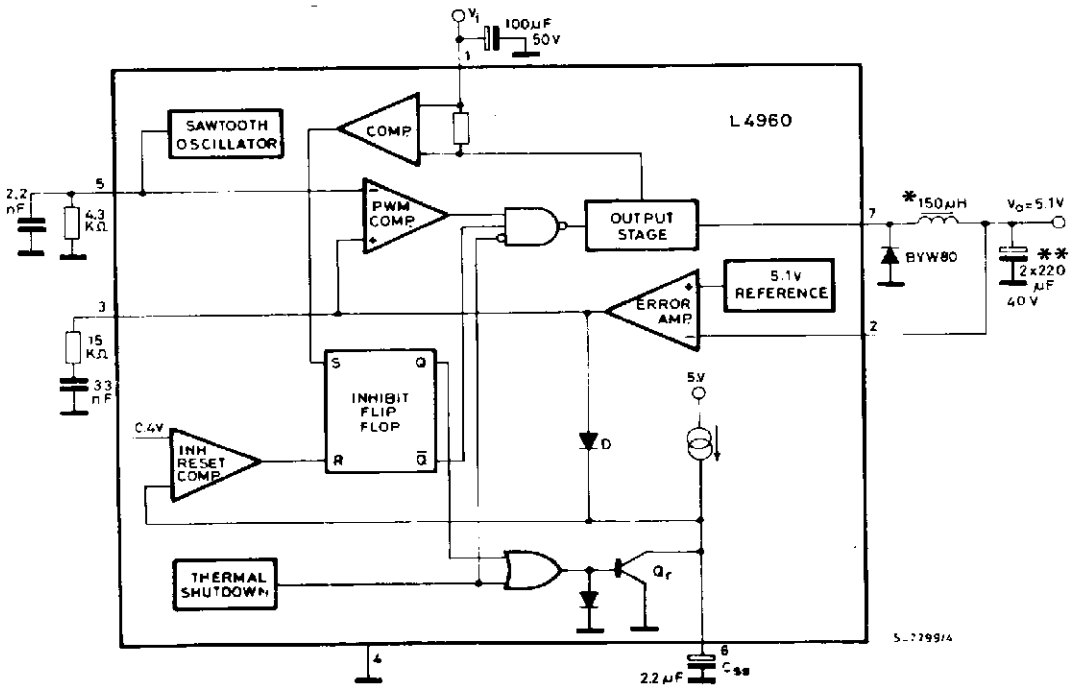
Figure 25. P.C. board and component layout of the Fig. 24 (1 : 1 scale)



Resistor values for standard output voltages		
V_o	R3	R4
12V	4.7KΩ	6.2KΩ
15V	4.7KΩ	9.1KΩ
18V	4.7KΩ	12KΩ
24V	4.7KΩ	18KΩ

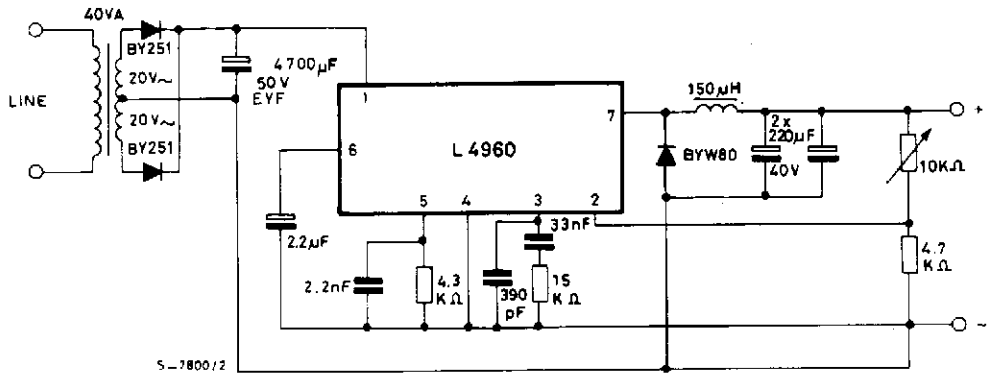
APPLICATION INFORMATION

Figure 26. A minimal 5.1V fixed regulator; Very few component are required



* COGEMA 946042 (TOROID CORE)
969051 (U15 CORE)
** EKR (ROE)

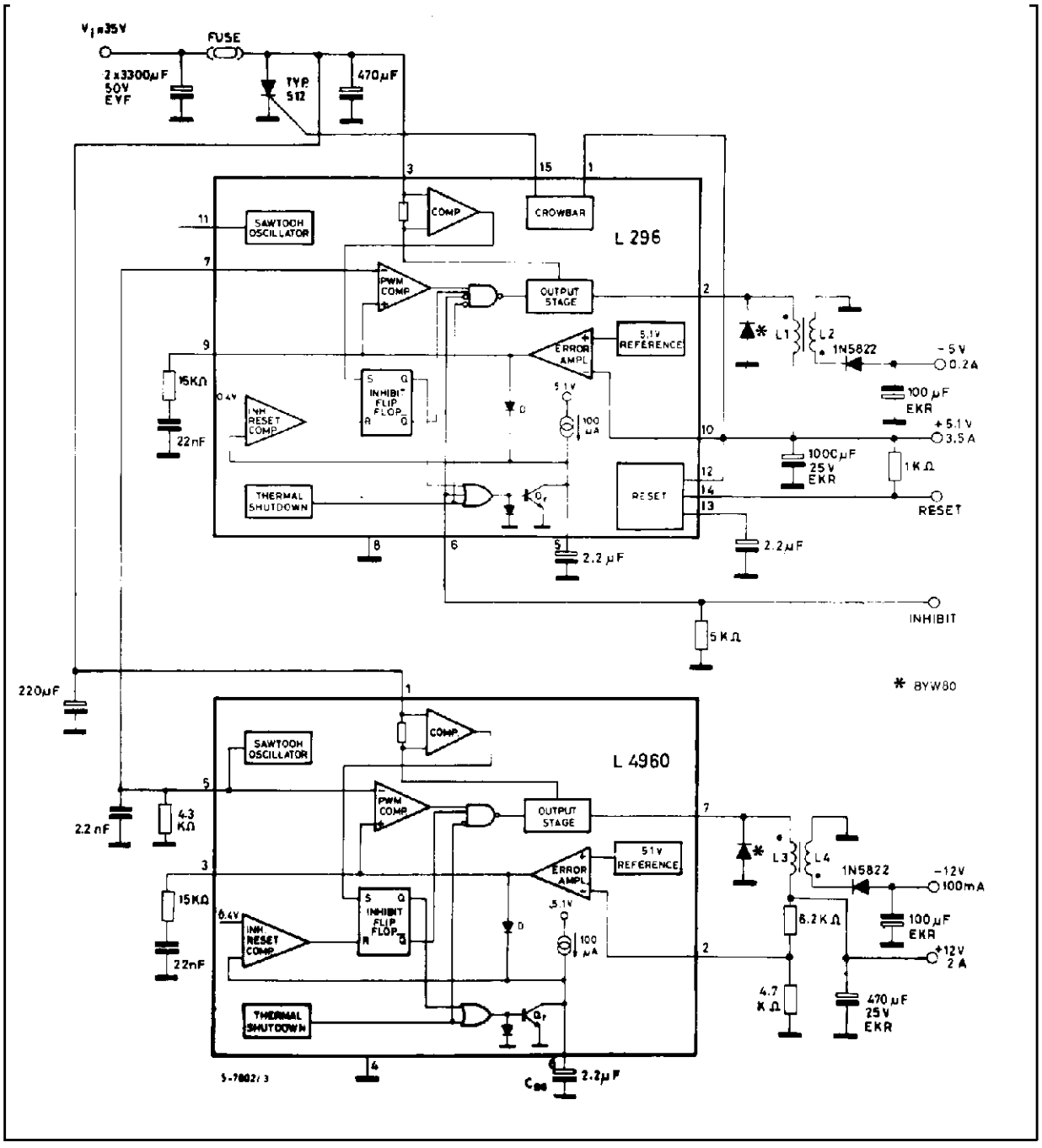
Figure 27. Programmable power supply



V_o = 5.1V to 15V
I_o = 2.5A max
Load regulation (1A to 2A) = 10mV (V_o = 5.1V)

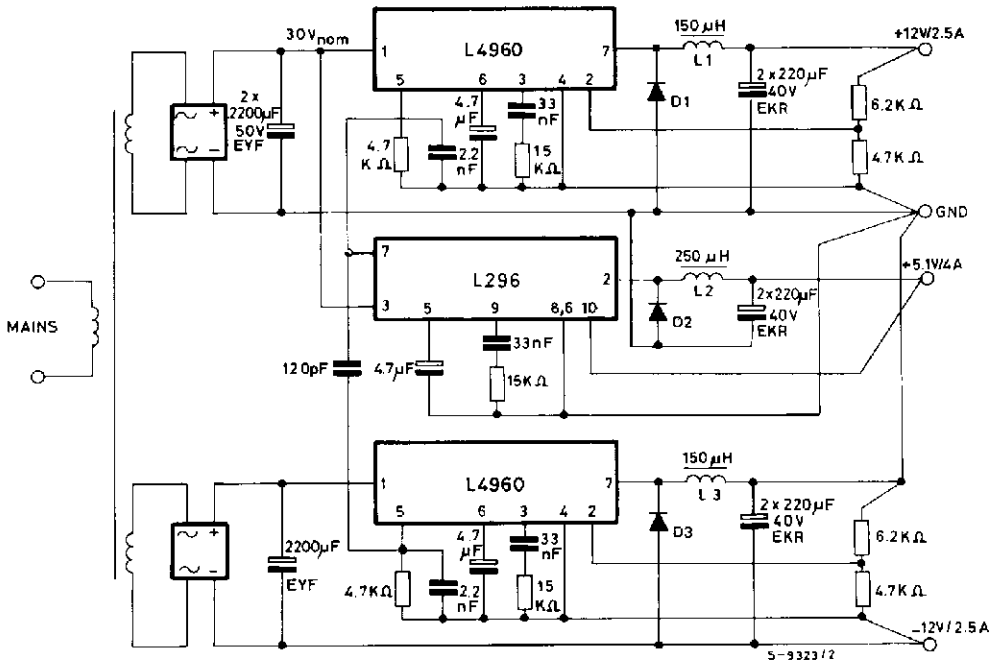
APPLICATION INFORMATION (continued)

Figure 28. Microcomputer supply with + 5.1V, -5V, +12V and -12V outputs



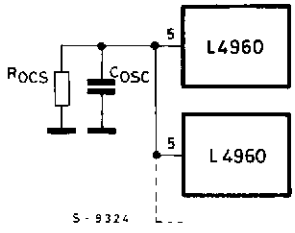
APPLICATION INFORMATION (continued)

Figure 29. DC-DC converter 5.1V/4A, ± 12V/2.5A; a suggestion how to synchronize a negative output



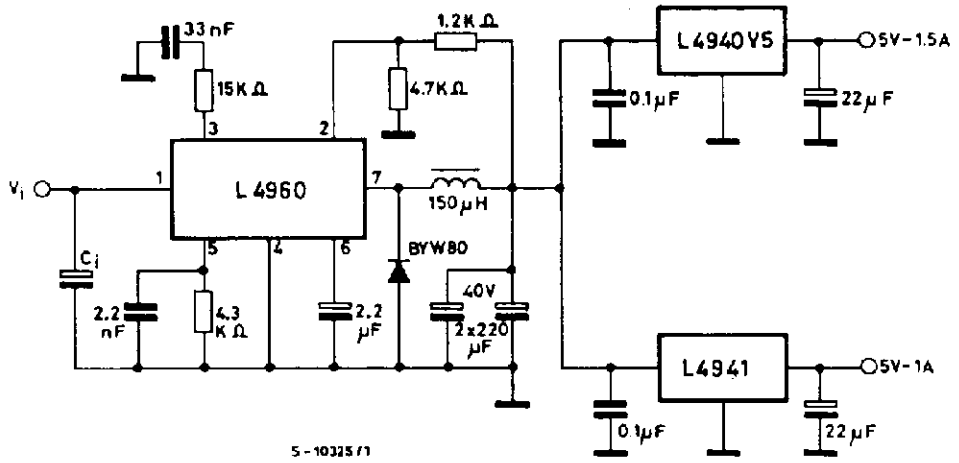
L1, L3 = COGEMA 946042 (969051)
L2 = COGEMA 946044 (946045)
D_1, D_2, D_3 = BYW80

Figure 30. - In multiple supplies several L4960s can be synchronized as shown



APPLICATION INFORMATION (continued)

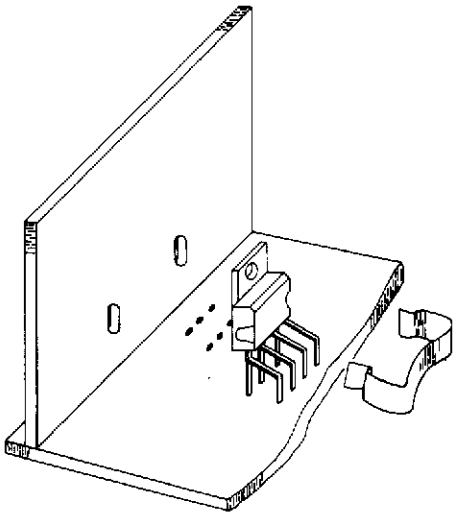
Figure 31. Regulator for distributed supplies



MOUNTING INSTRUCTION

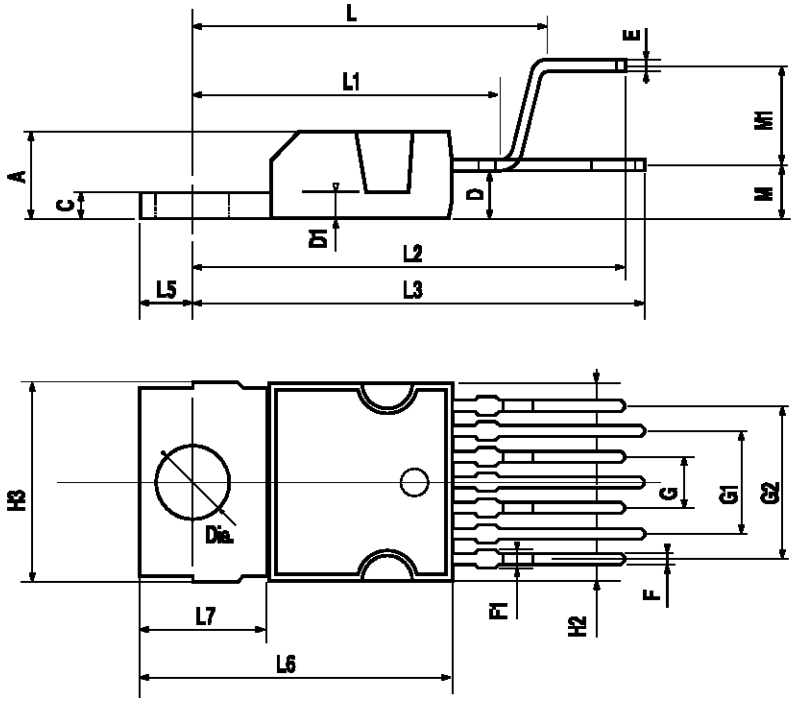
The power dissipated in the circuit must be removed by adding an external heatsink.
Thanks to the Heptawatt package attaching the hetsink is very simple, a screw or a compression spring (clip) being sufficient. Between the heatsink and the package it is better to insert a layer of silicon grease, to optimize the thermal contact, no electrical isolation is needed between the two surfaces.

Figure 32. Mounting example



HEPTAWATT PACKAGE MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			4.8			0.189
C			1.37			0.054
D	2.4		2.8	0.094		0.110
D1	1.2		1.35	0.047		0.053
E	0.35		0.55	0.014		0.022
F	0.6		0.8	0.024		0.031
F1			0.9			0.035
G	2.41	2.54	2.67	0.095	0.100	0.105
G1	4.91	5.08	5.21	0.193	0.200	0.205
G2	7.49	7.62	7.8	0.295	0.300	0.307
H2			10.4			0.409
H3	10.05		10.4	0.396		0.409
L		16.97			0.668	
L1		14.92			0.587	
L2		21.54			0.848	
L3		22.62			0.891	
L5	2.6		3	0.102		0.118
L6	15.1		15.8	0.594		0.622
L7	6		6.6	0.236		0.260
M		2.8			0.110	
M1		5.08			0.200	
Dia	3.65		3.85	0.144		0.152

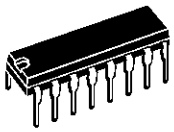


SGS-THOMSON MICROELECTRONICS

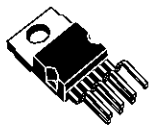
L4962

1.5A POWER SWITCHING REGULATOR

- 1.5A OUTPUT CURRENT
- 5.1V TO 40V OUTPUT VOLTAGE RANGE
- PRECISE (± 2%) ON-CHIP REFERENCE
- HIGH SWITCHING FREQUENCY
- VERY HIGH EFFICIENCY (UP TO 90%)
- VERY FEW EXTERNAL COMPONENTS
- SOFT START
- INTERNAL LIMITING CURRENT
- THERMAL SHUTDOWN



POWERDIP
(12 + 2 + 2)



HEPTAWATT

ORDERING NUMBERS : L4962/A (12 + 2 + 2 Powerdip)
L4962E/A (Heptawatt)
L4962EH/A (Horizontal Heptawatt)

DESCRIPTION

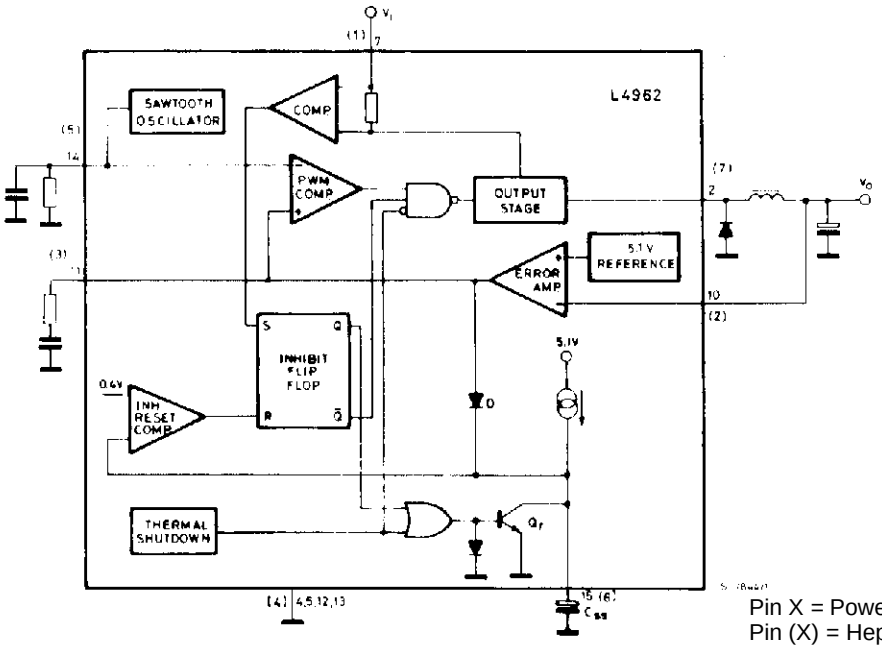
The L4962 is a monolithic power switching regulator delivering 1.5A at a voltage variable from 5V to 40V in step down configuration.

Features of the device include current limiting, soft start, thermal protection and 0 to 100% duty cycle for continuous operating mode.

The L4962 is mounted in a 16-lead Powerdip plastic package and Heptawatt package and requires very few external components.

Efficient operation at switching frequencies up to 150KHz allows a reduction in the size and cost of external filter components.

BLOCK DIAGRAM

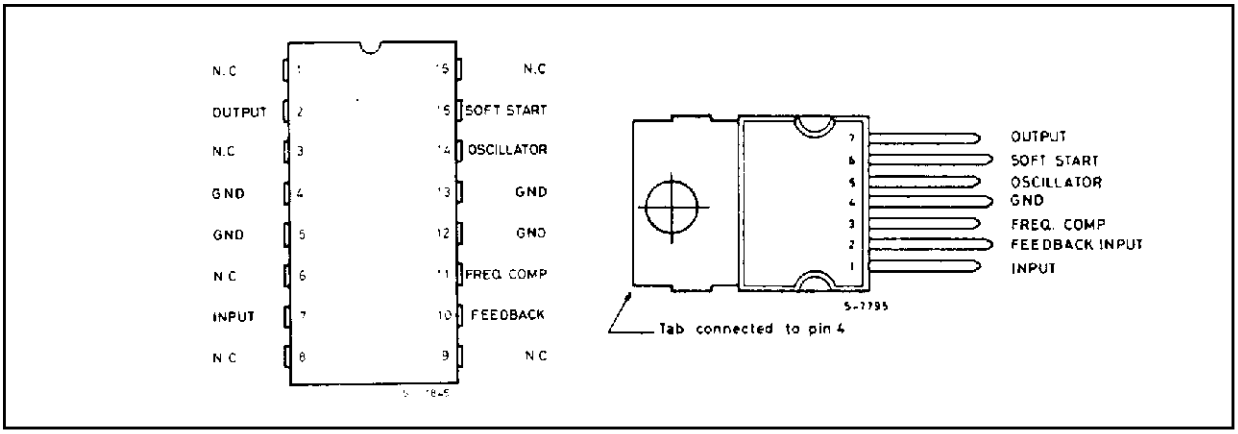


Pin X = Powerdip
Pin (X) = Heptawatt

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_7	Input voltage	50	V
$V_7 - V_2$	Input to output voltage difference	50	V
V_2	Negative output DC voltage	-1	V
	Output peak voltage at t = 0.1µs; f = 100KHz	-5	V
V_{11}, V_{15}	Voltage at pin 11, 15	5.5	V
V_{10}	Voltage at pin 10	7	V
I_{11}	Pin 11 sink current	1	mA
I_{14}	Pin 14 source current	20	mA
P_{tot}	Power dissipation at $T_{pins} \leq 90°C$ (Powerdip) $T_{case} \leq 90°C$ (Heptawatt)	4.3 15	W W
T_j, T_{stg}	Junction and storage temperature	-40 to 150	°C

PIN CONNECTION (Top view)



THERMAL DATA

Symbol	Parameter		Heptawatt	Powerdip
$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max	4°C/W	-
$R_{th\ j\text{-}pins}$	Thermal resistance junction-pins	max	-	14°C/W
$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	50°C/W	80°C/W*

* Obtained with the GND pins soldered to printed circuit with minimized copper area.

PIN FUNCTIONS

HEPTAWATT	POWERDIP	NAME	FUNCTION
1	7	SUPPLY VOLTAGE	Unregulated voltage input. An internal regulator powers the internal logic.
2	10	FEEDBACK INPUT	The feedback terminal of the regulation loop. The output is connected directly to this terminal for 5.1V operation; it is connected via a divider for higher voltages.
3	11	FREQUENCY COMPENSATION	A series RC network connected between this terminal and ground determines the regulation loop gain characteristics.

PIN FUNCTIONS (cont'd)

HEPTAWATT	POWERDIP	NAME	FUNCTION
4	4, 5, 12, 13	GROUND	Common ground terminal.
5	14	OSCILLATOR	A parallel RC network connected to this terminal determines the switching frequency. This pin must be connected to pin 7 input when the internal oscillator is used.
6	15	SOFT START	Soft start time constant. A capacitor is connected between this terminal and ground to define the soft start time constant. This capacitor also determines the average short circuit output current.
7	2	OUTPUT	Regulator output.
	1, 3, 6, 8, 9, 16		N.C.

ELECTRICAL CHARACTERISTICS (Refer to the test circuit, T_j = 25 °C, V_i = 35V, unless otherwise specified)

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
DYNAMIC CHARACTERISTICS							
V_o	Output voltage range	V_i = 46V	I_o = 1A	V_{ref}		40	V
V_i	Input voltage range	$V_o = V_{ref}$ to 36V	I_o = 1.5A	9		46	V
ΔV_o	Line regulation	V_i = 10V to 40V $V_o = V_{ref}$	I_o = 1A		15	50	mV
ΔV_o	Load regulation	$V_o = V_{ref}$	I_o = 0.5A to 1.5A		8	20	mV
V_{ref}	Internal reference voltage (pin 10)	V_i = 9V to 46V	I_o = 1A	5	5.1	5.2	V
$\frac{\Delta V_{ref}}{\Delta T}$	Average temperature coefficient of refer. voltage	T_j = 0°C to 125°C I_o = 1A			0.4		mV/°C
V_d	Dropout voltage	I_o = 1.5A			1.5	2	V
I_{om}	Maximum operating load current	V_i = 9V to 46V $V_o = V_{ref}$ to 36V		1.5			A
I_{2L}	Current limiting threshold (pin 2)	V_i = 9V to 46V $V_o = V_{ref}$ to 36V		2		3.3	A
I_{SH}	Input average current	V_i = 46V; output short-circuit			15	30	mA
η	Efficiency	f = 100KHz	$V_o = V_{ref}$		70		%
		I_o = 1A	V_o = 12V		80		%
SVR	Supply voltage ripple rejection	$\Delta V_i = 2V_{rms}$ f_{ripple} = 100Hz $V_o = V_{ref}$	Io = 1A	50	56		dB

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
DYNAMIC CHARACTERISTICS (cont'd)						
f	Switching frequency		85	100	115	KHz
$\frac{\Delta f}{\Delta V_i}$	Voltage stability of switching frequency	V_i = 9V to 46V		0.5		%
$\frac{\Delta f}{\Delta T_j}$	Temperature stability of switching frequency	T_j = 0°C to 125°C		1		%
f_{max}	Maximum operating switching frequency	$V_o = V_{ref}$ I_o = 1A	120	150		KHz
T_{sd}	Thermal shutdown junction temperature			150		°C
DC CHARACTERISTICS						
I_{7Q}	Quiescent drain current	100% duty cycle pins 2 and 14 open; V_i = 46V		30	40	mA
		0% duty cycle; V_i = 46V		15	20	mA
$-I_{2L}$	Output leakage current	0% duty cycle; V_i = 46V			1	mA
SOFT START						
I_{15SO}	Source current		100	140	180	µA
I_{15SI}	Sink current		50	70	120	µA
ERROR AMPLIFIER						
V_{11H}	High level output voltage	V_{10} = 4.7V I_{11} = 100µA	3.5			V
V_{11L}	Low level output voltage	V_{10} = 5.3V I_{11} = 100µA			0.5	V
I_{11SI}	Sink output current	V_{10} = 5.3V	100	150		µA
$-I_{11SO}$	Source output current	V_{10} = 4.7V	100	150		µA
I_{10}	Input bias current	V_{10} = 5.2V		2	10	µA
G_v	DC open loop gain	V_{11} = 1V to 3V	46	55		dB
OSCILLATOR						
$-I_{14}$	Oscillator source current		5			mA

CIRCUIT OPERATION (refer to the block diagram)

The L4962 is a monolithic stepdown switching regulator providing output voltages from 5.1V to 40V and delivering 1.5A.

The regulation loop consists of a sawtooth oscillator, error amplifier, comparator and the output stage. An error signal is produced by comparing the output voltage with a precise 5.1V on-chip reference (zener zap trimmed to ± 2%).

This error signal is then compared with the sawtooth signal to generate the fixed frequency pulse width modulated pulses which drive the output stage.

The gain and frequency stability of the loop can be adjusted by an external RC network connected to pin 11. Closing the loop directly gives an output voltage of 5.1V. Higher voltages are obtained by inserting a voltage divider.

Output overcurrents at switch on are prevented by the soft start function. The error amplifier output is initially clamped by the external capacitor C_{SS} and allowed to rise, linearly, as this capacitor is charged by a constant current source. Output overload protection is provided in the form of a current limiter. The load current is sensed by an internal metal resistor connected to a comparator. When the load current exceeds a preset threshold this comparator sets a flip flop which disables the output stage and discharges the soft start capacitor. A second comparator resets the flip flop when the voltage across the soft start capacitor has fallen to 0.4V.

The output stage is thus re-enabled and the output voltage rises under control of the soft start network. If the overload condition is still present the limiter will trigger again when the threshold current is reached. The average short circuit current is limited to a safe value by the dead time introduced by the soft start network. The thermal overload circuit disables circuit operation when the junction temperature reaches about 150°C and has hysteresis to prevent unstable conditions.

Figure 1. Soft start waveforms

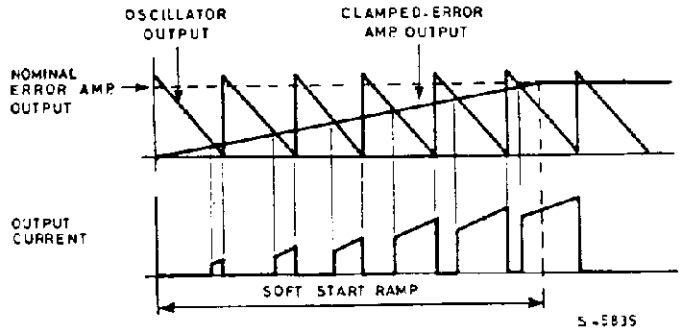


Figure 2. Current limiter waveforms

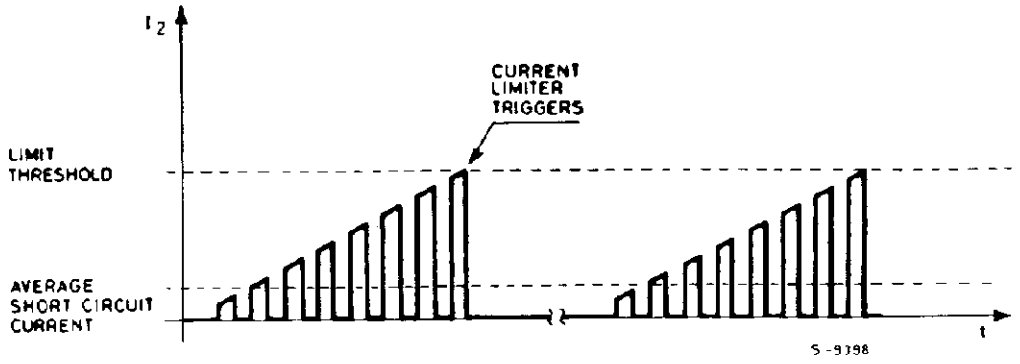
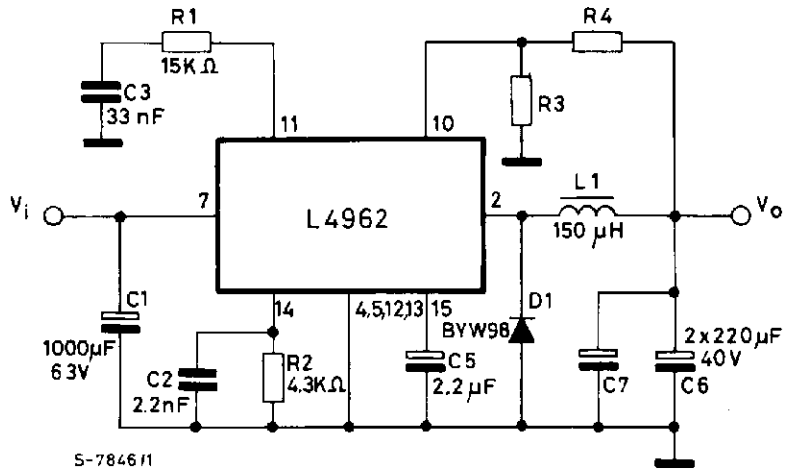


Figure 3. Test and application circuit (Powerdip)



1) D_1: BYW98 or 3A Schottky diode, 45V of VRRM;
2) L_1: CORE TYPE - MAGNETICS 58120 - A2 MPP
   N° TURNS 45, WIRE GAUGE: 0.8mm (20 AWG)
3) C_6, C_7: ROE, EKR 220µF 40V

Figure 4. Quiescent drain current vs. supply voltage (0% duty cycle)

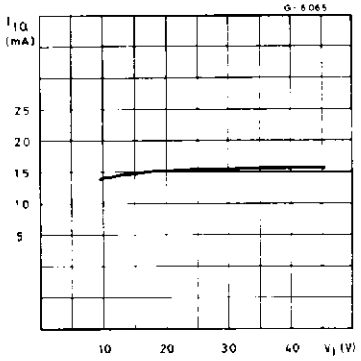


Figure 5. Quiescent drain current vs. supply voltage (100% duty cycle)

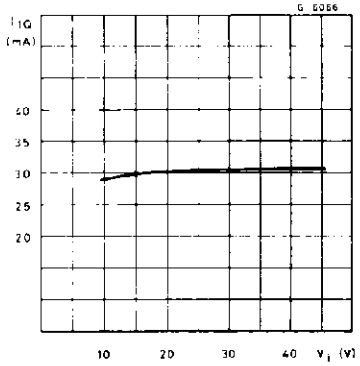


Figure 6. Quiescent drain current vs. junction temperature (0% duty cycle)

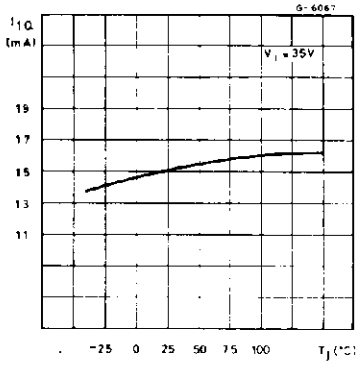


Figure 7. Quiescent drain current vs. junction temperature (100% duty cycle)

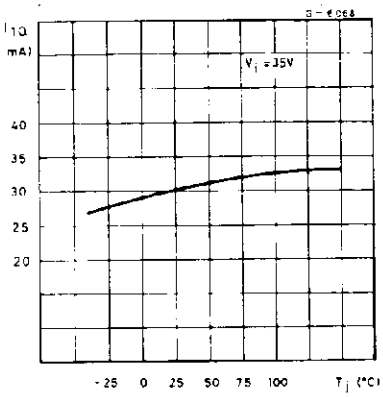


Figure 8. Reference voltage (pin 10) vs. V_i rdip) vs. V_i

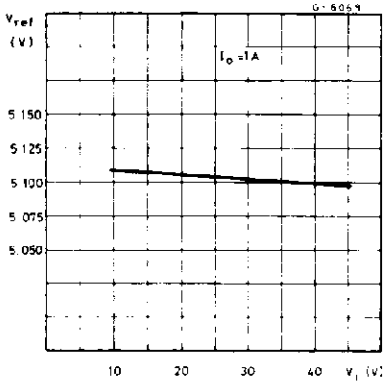


Figure 9. Reference voltage (pin 10) vs. junction temperature

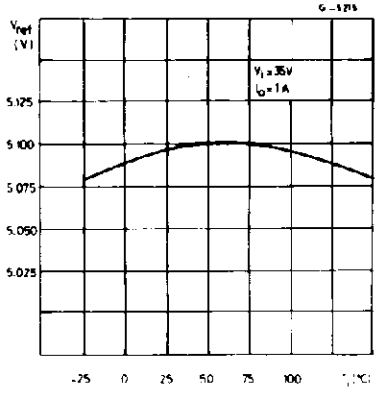


Figure 10. Open loop frequency and phase re- sponse of error amplifier

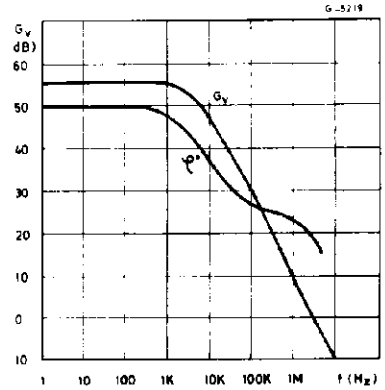


Figure 11. Switching frequency vs. input voltage

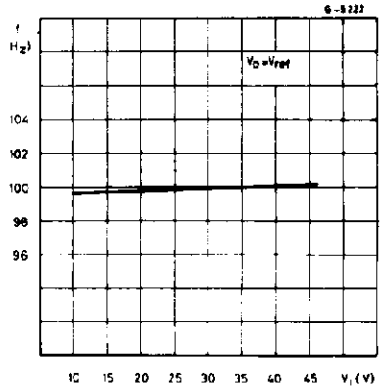


Figure 12. Switching frequency vs. junction temperature

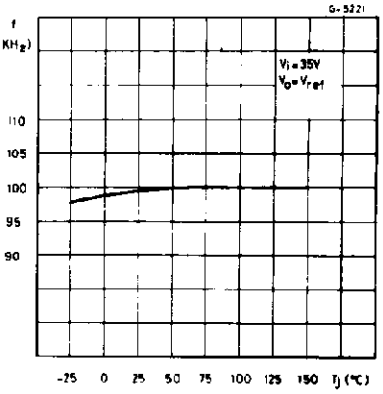


Figure 13. Switching frequency vs. R2 (see test circuit)

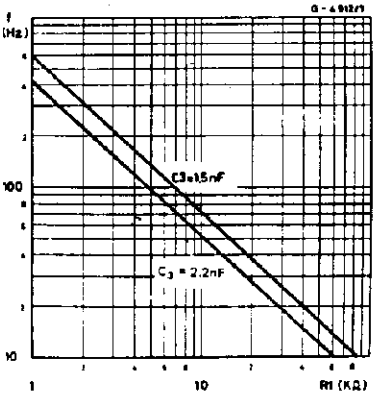


Figure 14. Line transient response

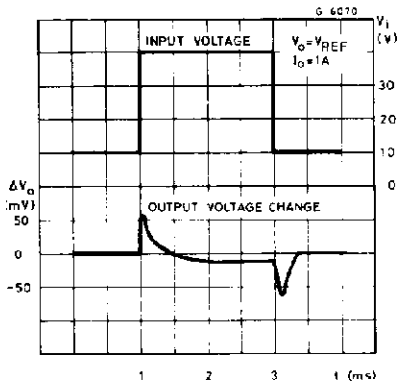


Figure 15. Load transient response

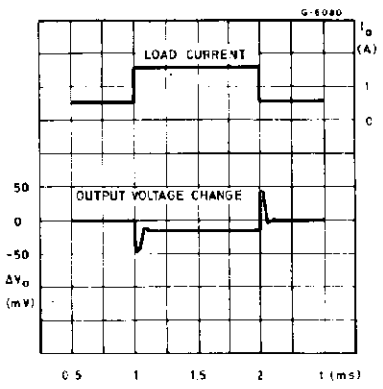


Figure 16. Supply voltage ripple rejection vs. frequency

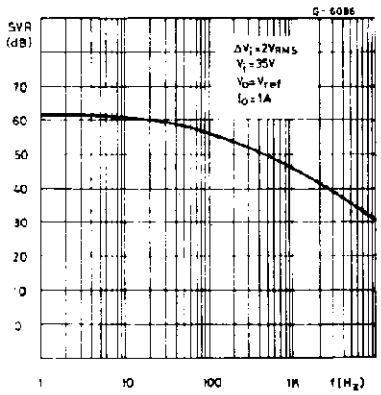


Figure 17. Dropout voltage between pin 7 and pin 2 vs. current at pin 2

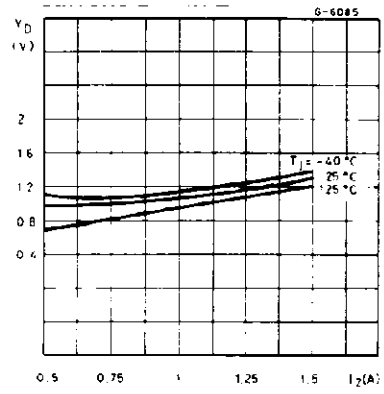


Figure 18. Dropout voltage between pin 7 and 2 vs. junction temperature

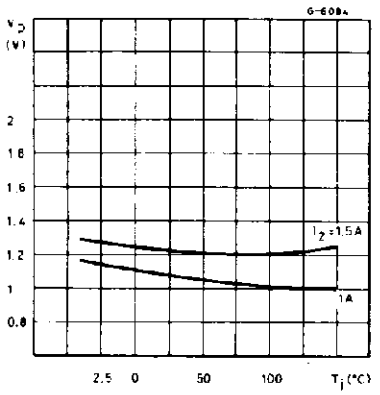


Figure 19. Efficiency vs. output current

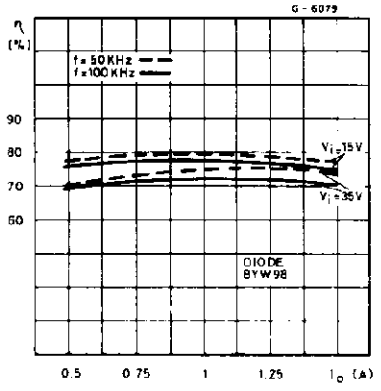


Figure 20. Efficiency vs. output current

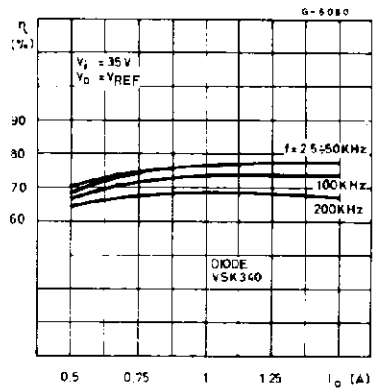


Figure 21. Efficiency vs. output current

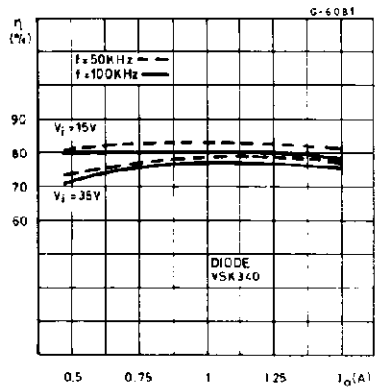


Figure 22. Efficiency vs. output voltage

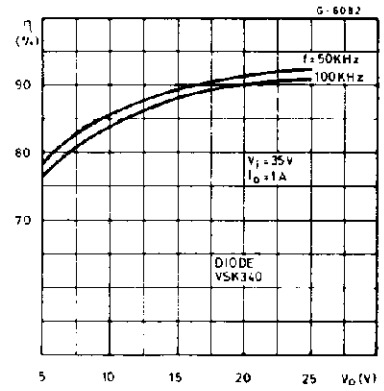


Figure 23. Efficiency vs. output voltage

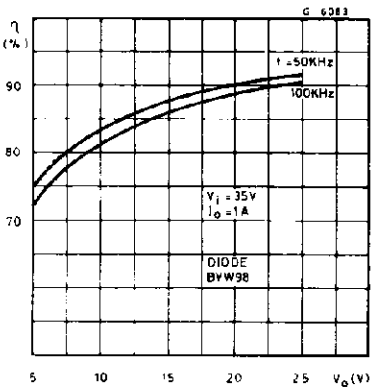
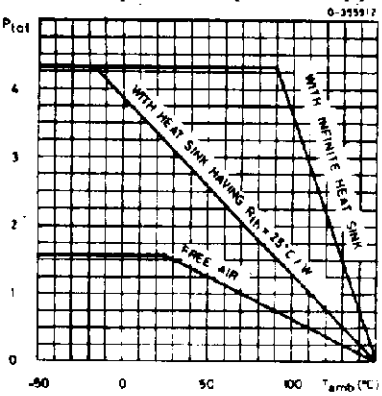
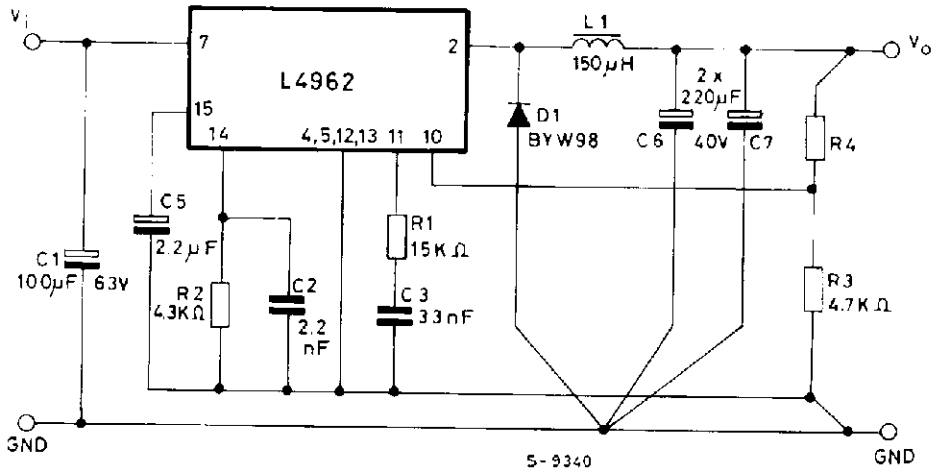


Figure 24. Maximum allowable power dissipation vs. ambient temperature (Powerdip)



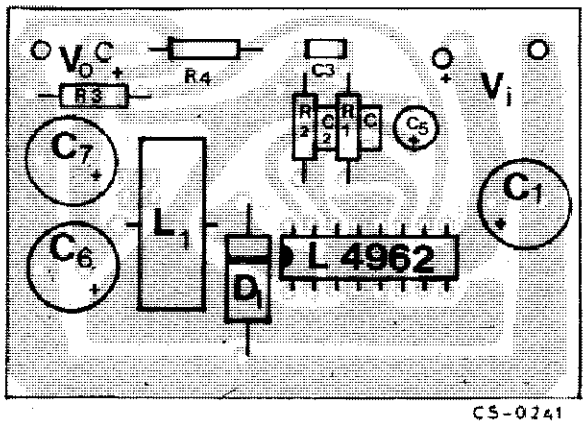
APPLICATION INFORMATION

Figure 25. Typical application circuit



C_1, C_6, C_7: EKR (ROE)
D_1: BYW98 OR VISK340 (SCHOTTKY)
SUGGESTED INDUCTORS: (L_1) = MAGNETICS 58120 - A2MPP - 45 TURNS - WIRE GAUGE 0.8mm (20AWG) COGEMA 946043
OR U15, GUP15, 60 TURNS 1mm, AIR GAP 0.8mm (20 AWG) - COGEMA 969051.

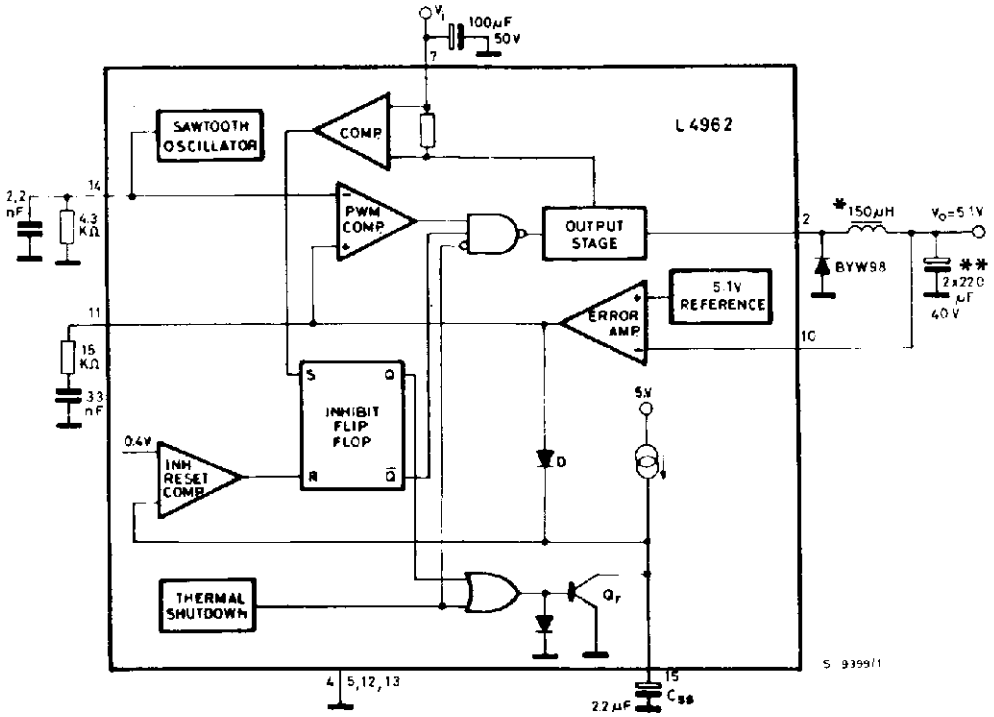
Figure 26. P.C. board and component layout of the circuit of Fig. 25 (1 : 1 scale)



Resistor values for standard output 7 voltages		
V_o	R3	R4
12V	4.7KΩ	6.2KΩ
15V	4.7KΩ	9.1KΩ
18V	4.7KΩ	12KΩ
24V	4.7KΩ	18KΩ

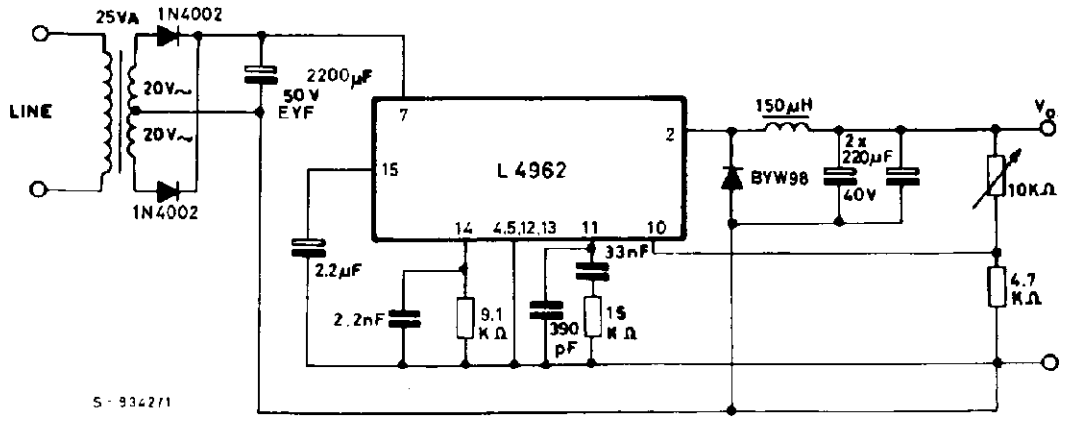
APPLICATION INFORMATION (continued)

Figure 27. - A minimal 5.1V fixed regulator; Very few component are required



* COGEMA 946043 (TOROID CORE)
969051 (U15 CORE)
** EKR (ROE)

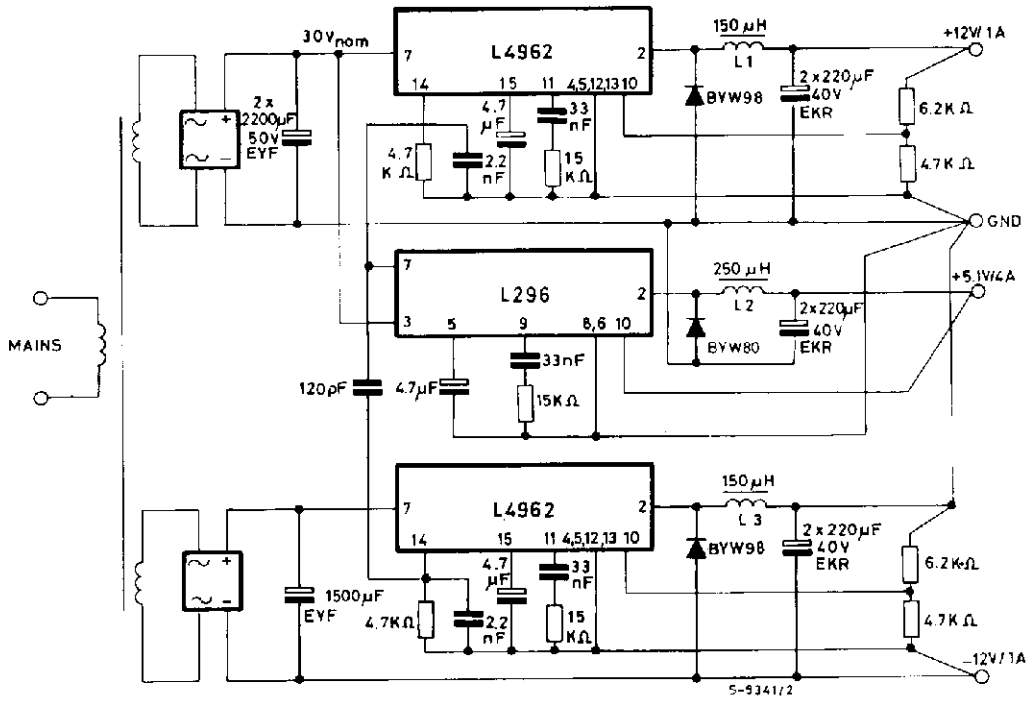
Figure 28. Programmable power supply



V_o = 5.1V to 15V
I_o = 1.5A max
Load regulation (0.5A to 1.5A) = 10mV (V_o = 5.1V)
Line regulation (220V ± 15% and to I_o = 1A) = 15mV (V_o = 5.1V)

APPLICATION INFORMATION (continued)

Figure 29. DC-DC converter 5.1V/4A, ± 12V/1A. A suggestion how to synchronize a negative output



L1, L3 = COGEMA 946043 (969051)
L2 = COGEMA 946044 (946045)

Figure 30. In multiple supplies several L4962s can be synchronized as shown

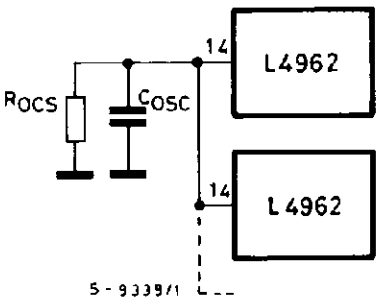
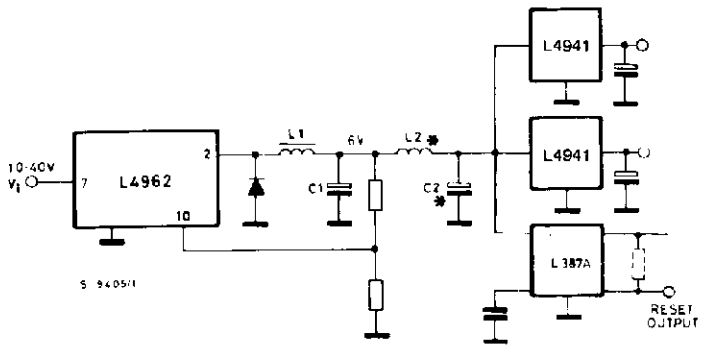


Figure 31. Preregulator for distributed supplies



* L2 and C2 are necessary to reduce the switching frequency spikes when linear regulators are remote from L4962

MOUNTING INSTRUCTION

The Rth-j-amb of the L4962 can be reduced by soldering the GND pins to a suitable copper area of the printed circuit board (Fig. 32).
The diagram of figure 33 shows the $R_{th\text{-}j\text{-}amb}$ as a function of the side "l" of two equal square copper areas having the thickness of 35µ (1.4 mils). During soldering the pins temperature must not exceed 260°C and the soldering time must not be longer than 12 seconds.
The external heatsink or printed circuit copper are must be connected to electrical ground.

Figure 32. Example of P.C. board copper area which is used as heatsink

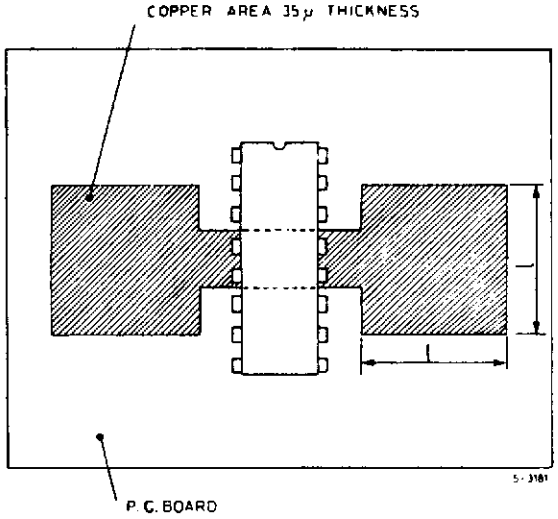
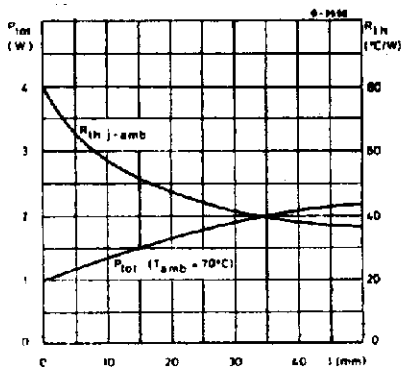
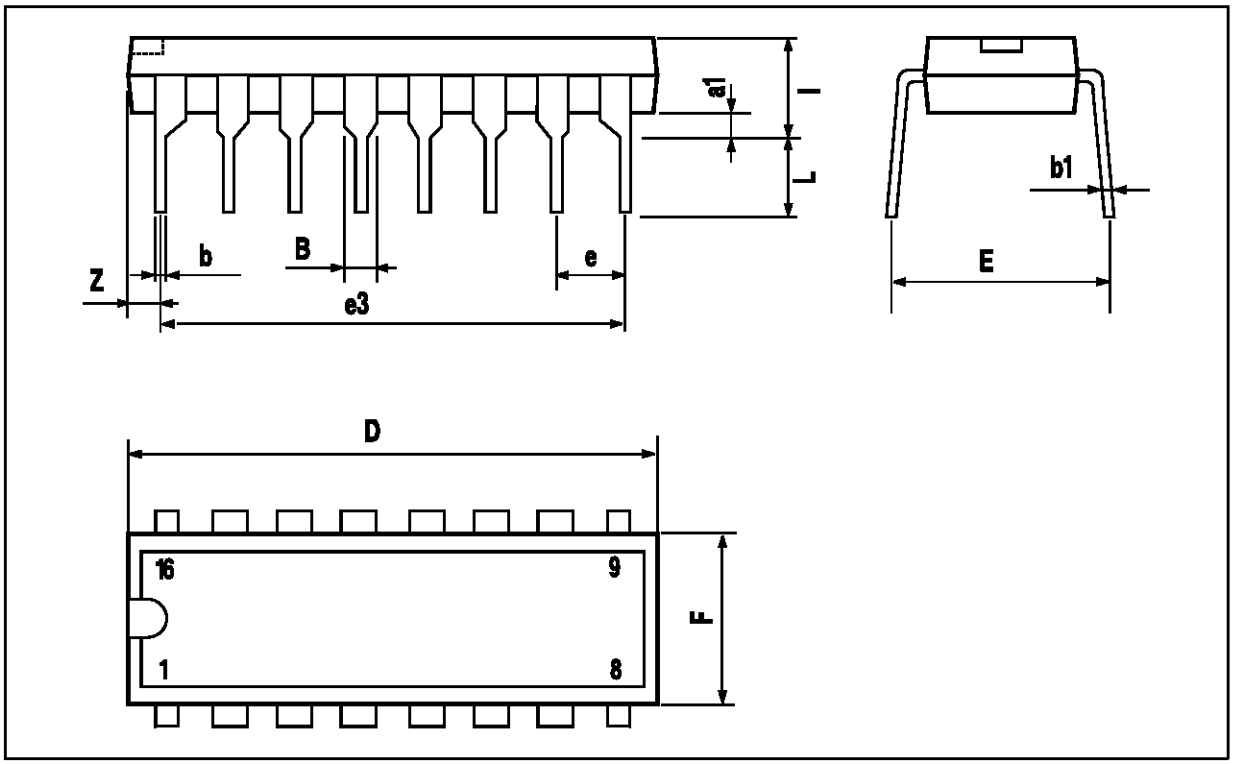


Figure 33. Maximum dissipable power and junction to ambient thermal resistance vs. side "l"



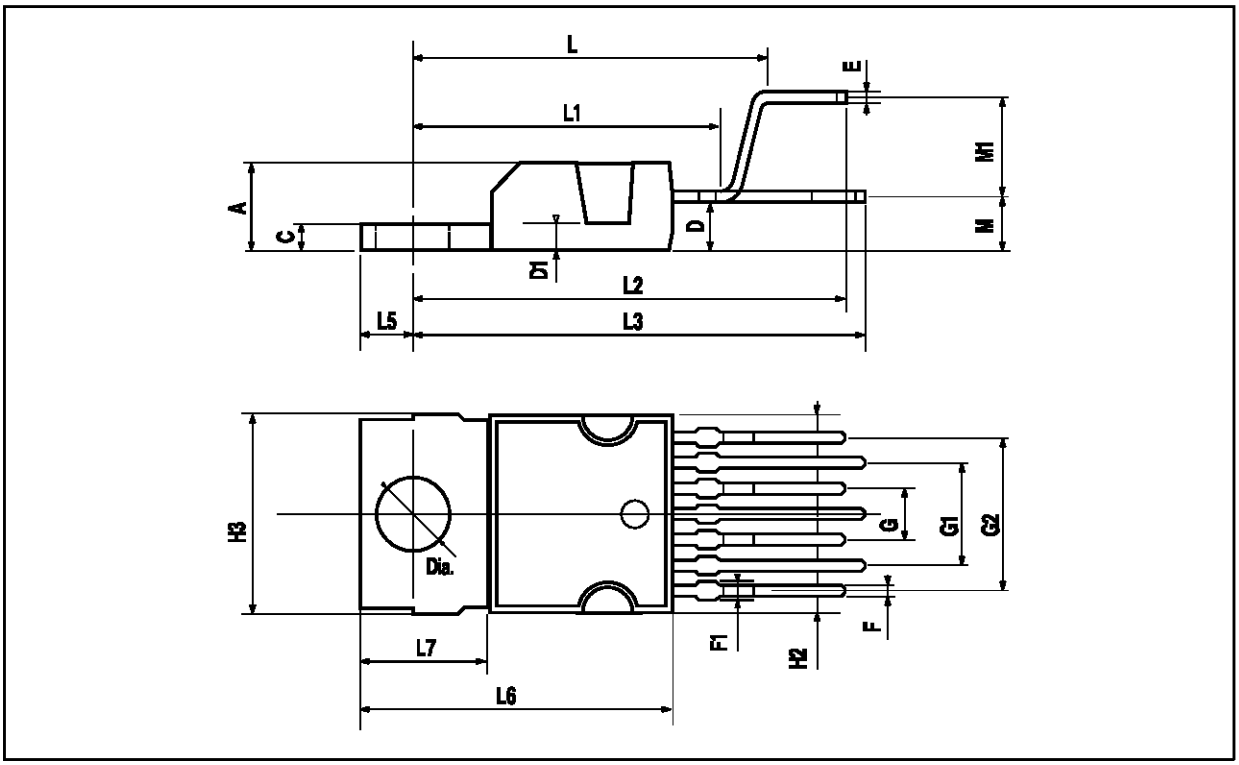
POWERDIP PACKAGE MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
a1	0.51			0.020		
B	0.85		1.40	0.033		0.055
b		0.50			0.020	
b1	0.38		0.50	0.015		0.020
D			20.0			0.787
E		8.80			0.346	
e		2.54			0.100	
e3		17.78			0.700	
F			7.10			0.280
I			5.10			0.201
L		3.30			0.130	
Z			1.27			0.050



HEPTAWATT PACKAGE MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			4.8			0.189
C			1.37			0.054
D	2.4		2.8	0.094		0.110
D1	1.2		1.35	0.047		0.053
E	0.35		0.55	0.014		0.022
F	0.6		0.8	0.024		0.031
F1			0.9			0.035
G	2.41	2.54	2.67	0.095	0.100	0.105
G1	4.91	5.08	5.21	0.193	0.200	0.205
G2	7.49	7.62	7.8	0.295	0.300	0.307
H2			10.4			0.409
H3	10.05		10.4	0.396		0.409
L		16.97			0.668	
L1		14.92			0.587	
L2		21.54			0.848	
L3		22.62			0.891	
L5	2.6		3	0.102		0.118
L6	15.1		15.8	0.594		0.622
L7	6		6.6	0.236		0.260
M		2.8			0.110	
M1		5.08			0.200	
Dia	3.65		3.85	0.144		0.152

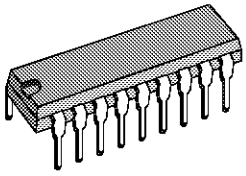


SGS-THOMSON MICROELECTRONICS

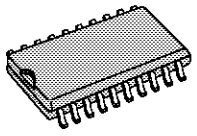
L4963
L4963D

1.5A SWITCHING REGULATOR

- 1.5A OUTPUT LOAD CURRENT
- 5.1 TO 36V OUTPUT VOLTAGE RANGE
- DISCONTINUOUS VARIABLE FREQUENCY MODE
- PRECISE (+/–2%) ON CHIP REFERENCE
- VERY HIGH EFFICIENCY
- VERY FEW EXTERNAL COMPONENTS
- NO FREQ. COMPENSATION REQUIRED
- RESET AND POWER FAIL OUTPUT FOR MICROPROCESSOR
- INTERNAL CURRENT LIMITING
- THERMAL SHUTDOWN



Powerdip12+3+3



SO20

ORDERING NUMBERS:

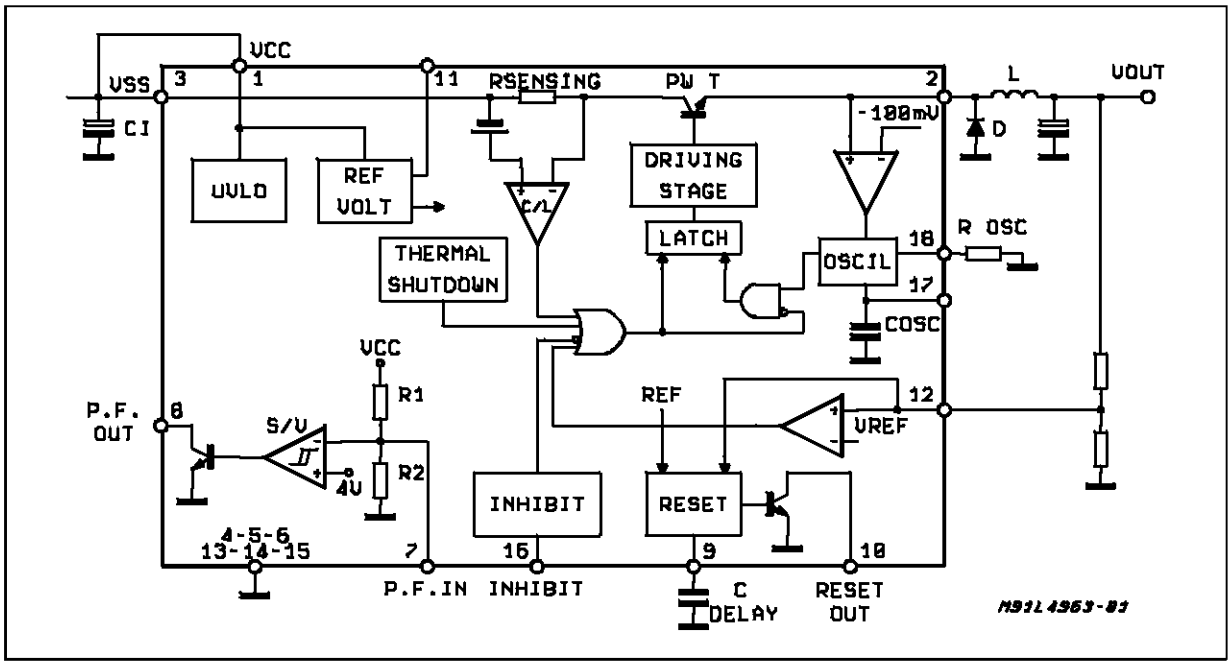
L4963W L4963D

DESCRIPTION

The L4963 is a monolithic power switching regulator delivering 1.5A at 5.1V. The output voltage is adjustable from 5.1V to 36V, working in discontinuous variable frequency mode. Features of the device include remote inhibit, internal current limiting and thermal protection, reset and power fail outputs for microprocessor.

The L4963 is mounted in a 12+3+3 lead Powerdip (L4963) and SO20 large (L4963D) plastic packages and requires very few external components.

BLOCK DIAGRAM

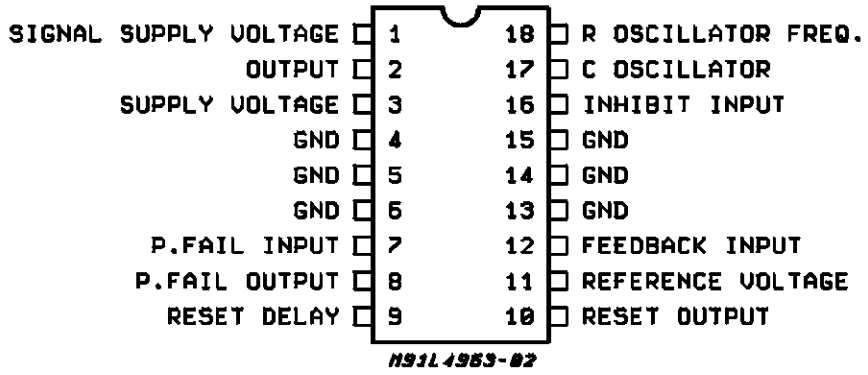


ABSOLUTE MAXIMUM RATINGS

Symbol		Parameter	Value	Unit
SO20	Powerdip			
V_i		Input Voltage (pin 1 and pin 3 connected togheter)	47	V
V_3–V_2		Input to Output Voltage Difference	47	V
V_2		Negative Output DC Voltage	–1	V
V_2		Negative Output Peak Voltage at t=0.2 µs, f=50kHz	–5	V
V_8	V_7	Power Fail Input	25	V
V_9, V_{11}	V_8, V_{10}	Reset and Power Fail Output	V_i	
V_{10}	V_9	Reset Delay Input	5.5	V
V_{13}, V_{18}	V_{12}, V_{16}	Feedback and Inhibit Inputs	7	V
V_{19}, V_{20}	V_{17}, V_{18}	Oscillator Inputs	5.5	V
P_{tot}		Total Power Dissipation Tpins ≤ 90°C (Power DIP) (T_{amb} = 70°C no copper area on PCB) (T_{amb} = 70°C, 4cm^2 copper area on PCB)	5 1.3 2	W W W
T_{stg}, T_j		Storage & Junction Temperature (Tamb = 70°C 6cm^2 copper area on PCB)	–40 to 150 1.45	°C W
P_{tot}		Total Power Dissipation Tpins ≤90°C (SO20L)	4	W

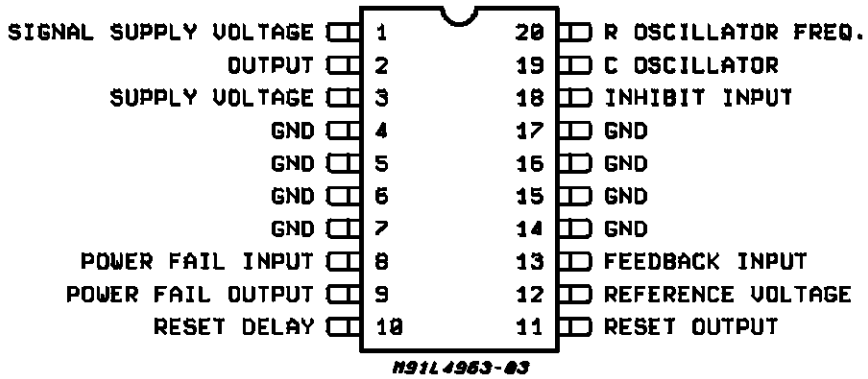
PIN CONNECTION (top view)

Powerdip18



N91L4963-02

SO20



N91L4963-03

PIN FUNCTIONS

SO20L	Power DIP	Name	Description
1	1	SIGNAL SUPPLY VOLTAGE	Must be Connected to pin 3
2	2	OUTPUT	Regulator output
3	3	SUPPLY VOLTAGE	Unregulated voltage input. An internal regulator powers the internal logic.
4, 5, 6, 7 14, 15, 16, 17	4, 5, 6 13, 14, 15	GROUND	Common ground terminal
8	7	POWER FAIL INPUT	Input of the power fail circuit. The threshold can be modified introducing an external voltage divider between the Supply Voltage and GND.
9	8	POWER FAIL OUTPUT	Open collector power fail signal output. This output is high when the supply voltage is safe.
10	9	RESET DELAY	A capacitor connected between this terminal and ground determines the reset signal delay time.
11	10	RESET OUTPUT	Open collector reset signal output. This output is high when the output voltage value is correct.
12	11	REFERENCE VOLTAGE	Reference voltage output.
13	12	FEEDBACK INPUT	Feedback terminal of the regulation loop. The output is connected directly to this terminal for 5.1V operation; it is connected via a divider for higher voltages.
18	16	INHIBIT INPUT	TTL level remote inhibit. A logic low level on this input disables the device.
19	17	C OSCILLATOR	Oscillator waveform. A capacitor connected between this terminal and ground modifies the maximum oscillator frequency.
20	18	R OSCILLATOR FREQ.	A resistor connected between this terminal and ground defines the maximum switching frequency.

THERMAL DATA

Symbol	Parameter		SO20	Powerdip	Unit
$R_{th\ j\text{-}pins}$	Thermal Resistance Junction to Pins	max.	15	12	°C/W
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction to Ambient (*)	max.	85	80	°C/W

(*) See Fig. 28

CIRCUIT DESCRIPTION (Refer to Block Diagram)

The L4963 is a monolithic stepdown regulator providing 1.5A at 5.1V working in discontinuous variable frequency mode. In normal operation the device resonates at a frequency depending primarily on the inductance value, the input and output voltage and the load current. The maximum switching however can be limited by an internal oscillator, which can be programmed by only one external resistor.

The fondamental regulation loop consists of two comparators, a precision 5.1V on-chip reference and a drive latch. Briefly the operation is as follows: when the choke ends its discharge the catch freewheeling recirculation filter diode begins to come out of forward conduction so the output voltage of the device approaches ground. When the output voltage reaches –0.1V the internal comparator sets the latch and the power stage is turned on. Then the inductor current rises linearly until the voltage sensed at the feedback input reaches the 5.1V reference.

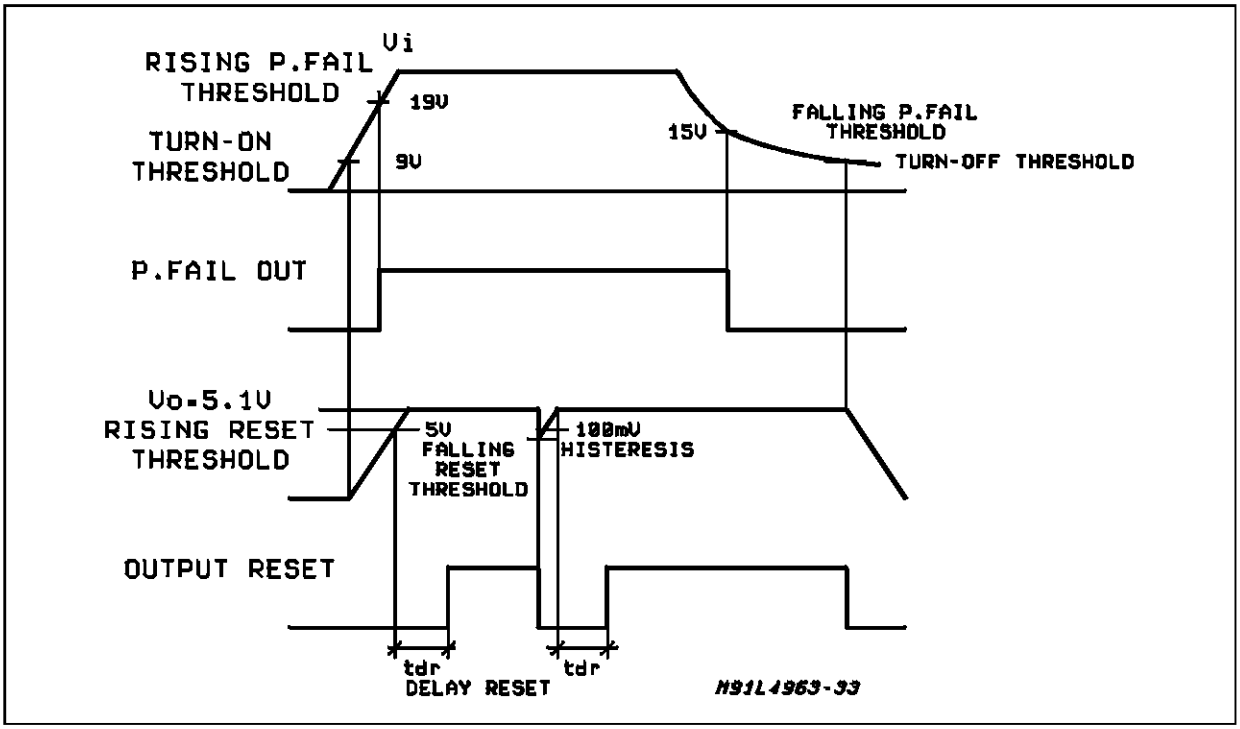
The second comparator then resets the latch and the output stage is turned off. The current in the choke falls linearly until it is fully discharged, then the cycle repeats. Closing the loop directly gives an output voltage of 5.1V. Higher output voltages are obtained by inserting a voltage divider and this method of control requires no frequency compensation network. At output voltages greater than 5.1V the available output current must be derated due to the increased power dissipation of the device.

Output overload protection is provided by an internal current limiter. The load current is sensed by a on-chip metal resistor connected to a comparator which resets the latch and turns off the power stage in overload condition. The reset circuits (see fig. 1) generates an output high signal when the output voltage value is correct. It has an open collector output and the output signal delay time can be programmed with an external capacitor. A power-fail circuit is also available and is used to monitor the supply voltage. Its output goes high when the supply voltage reaches a pre-programmed treshold set by a voltage divider to its input from the supply to ground. With the input left open the threshold is approximately equal to 5.1V. The output of the power fail is an open collector.

A TTL level inhibit is provided for applications such as remote on/off control. This input is activated by a low logic level and disables circuits operation.

The thermal overload circuit disables the device when the junction temperature is about 150°C and has hysteresis to prevent unstable conditions.

Figure 1: Reset and Power Fail Function



ELECTRICAL CHARACTERISTIC (Refer to the test circuit V_i = 30V T_j = 25°C unless otherwise specified)

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit	Fig.
DYNAMIC CHARACTERISTICS								
V_o	Output Voltage Range	V_i = 46V I_o = 0.5A		V_{ref}		36	V	2
V_i	Input Voltage Range	V_o = V_{ref} to 36V I_o = 0.5A		9		46	V	2
V_{12}	Feedback Voltage	V_i = 9 to 46V I_o = 0.5A		5	5.1	5.2	V	2
I_{12}	Input Bias Current	V_i = 15V V_{12} = 6V V_{17f} = 5V			5	20	µA	3a
V_{OS12}	Input Offset Voltage				5	10	mV	3a
ΔV_o	Line Regulation	V_i = 9 to 46V V_o = V_{ref} I_o = 0.5A			15	50	mV	2
ΔV_o	Load Regulation	V_o = V_{ref} I_o = 0.5 to 1.5A			15	45	mV	2
V_d	Dropout Voltage Between pin 3 and pin 2	I_2 = 3A V_i = 20V			1.5	2	V	2
I_{2L}	Current Limiting	V_i = 9 to 46V V_o = V_{ref} to 28V		3.5		6.5	A	2
I_o	Maximum Operating Load Current	V_i = 9 to 46V V_o = V_{ref}		1.5			A	2
SVR	Supply Voltage Ripple Rejection	V_i = 2Vrms V_o = V_{ref} fripple = 100Hz I_o = 1.5A		50	56		dB	2
V_{11}	Reference Voltage	V_i = 9 to 46V O < I_{11} < 5mA		5	5.1	5.2	V	3a
	Average Temperature Coefficient of Ref. Volt.	T_j = 0 to 125 °C			0.4		mV/°C	–
ΔV_{11}	V_{ref} Line Regulation	V_i = 9 to 46V			10	20	mV	3a
ΔV_{11}	V_{ref} Line Regulation	I_{ref} = 0 to 5mA V_i = 46V R_{osc} = 51KΩ		65 69	7	15	mV	3a
η	Efficiency	I_o = 1.5A V_o = V_{ref}		65	75		%	2
T_{sd}	Thermal Shutdown Junction Temperature			145	150		°C	–
	Hysteresis				30		°C	–
DC CHARACTERISTICS								
I_q	Quescent Drain Current	V_i = 46V I_o = 0mA	V_{16} = V_{12} = 0		14	20	mA	3a
			V_{16} = V_{ref} V_{12} = 5.3V		11	16	mA	3a
INHIBIT								
V_{16L}	Low Input Voltage	V_i = 9 to 46V		0.3		0.8	V	2
V_{16H}	High Input Voltage	V_i = 9 to 46V		2		5.5	V	2
I_{16L}	Input Current with Low Input Voltage	V_{16} = 0.8V			50	100	µA	2
I_{16L}	Input Current with High Input Voltage	V_{16} = 2V			10	20	µA	2

ELECTRICAL CHARACTERISTIC (Continued)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit	Fig.
RESET							
V_{12}	Rising Threshold Voltage	V_i = 9 to 46V	V_{ref} –150	V_{ref} –100	V_{ref} –50	mV	3b
V_{12}	Falling Threshold Voltage	V_i = 9 to 46V	V_{ref} –150	V_{ref} –200	V_{ref} –250	mV	3b
V_{9D}	Delay Rising Thereshold Voltage	V_7 = OPEN	4.3	4.5	4.7	V	3b
V_{9F}	Delay Falling Thereshold Voltage		1	1.5	2	V	3b
$-I_{9SO}$	Delay Source Current	V_9 = 4.7V V_{12} = 5.3V	70	110	140	µA	3b
I_{9SI}	Delay Sink Current	V_9 = 4.7V V_{12} = 4.7V	10			mA	3b
I_{10}	Output Leakage Current	V_i = 46V V_7 = 8.5V	50			µA	3b
V_{10}	Output Saturation Volt.	I_{10} = 15mA; V_I = 3 to 46V			0.4	V	3b
POWER FAIL							
V_R	Rising Threshold Voltage	Pin7 = open	17.5	19	20.5	V	3C
V_F	Falling Threshold Voltage	Pin7 = open	14.25	15	15.75	V	3c
V_7	Rising Threshold Voltage	V_i = 20V	4.14	4.5	4.86	V	–
V_7	Falling Threshold Voltage	V_i = 20V	3.325	3.5	3.675	V	–
V_s	Output Saturation Volt.	I_a = 5mA			0.4	V	3c
I_s	Output Leakage Current	V_i = 46V			50	µA	3c
OSCILLATOR							
f	Oscillator Frequency	R_T = 51KΩ	46	60	79	kHz	–
f	Oscillator Frequency	V_I = 9 to 46V T_j = 0 to 125°C R_T = 51KΩ	42		83	kHz	–

Figure 2: Test Circuit

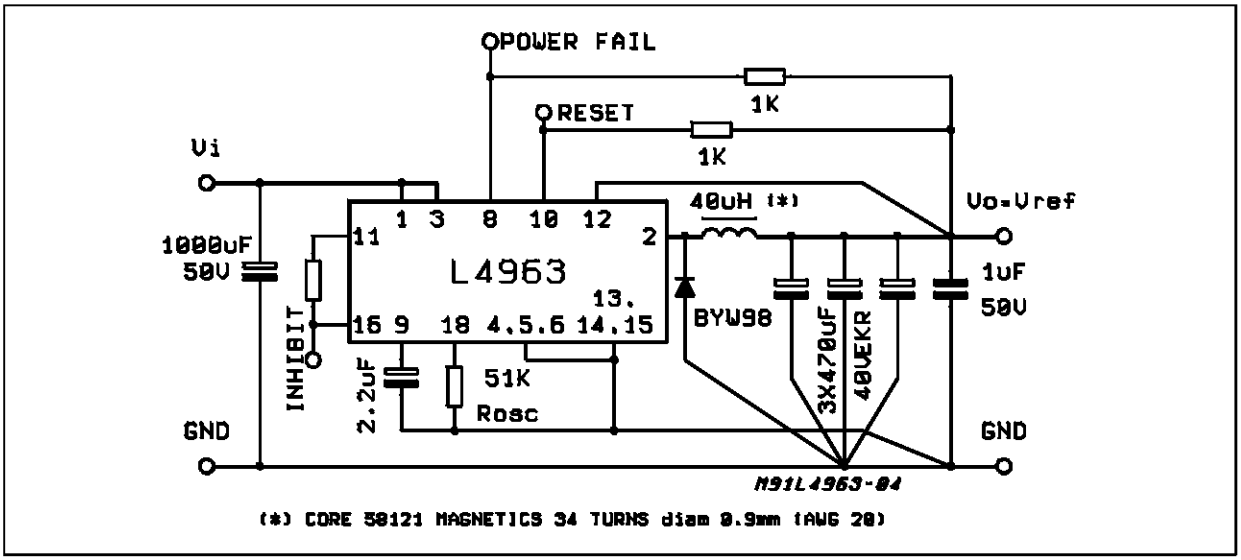


Figure 3: DC Test Circuit

Figure 3a

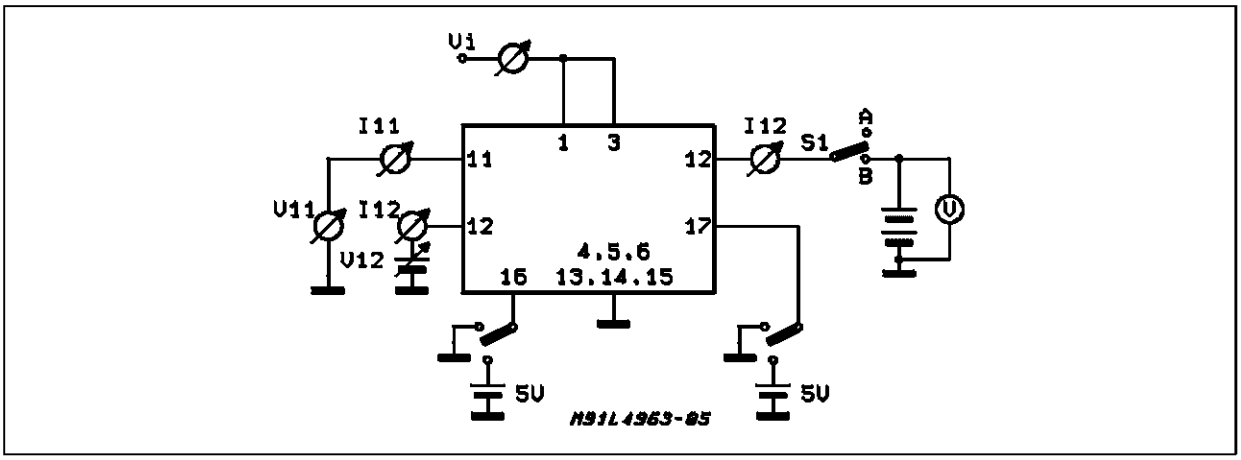


Figure 3b

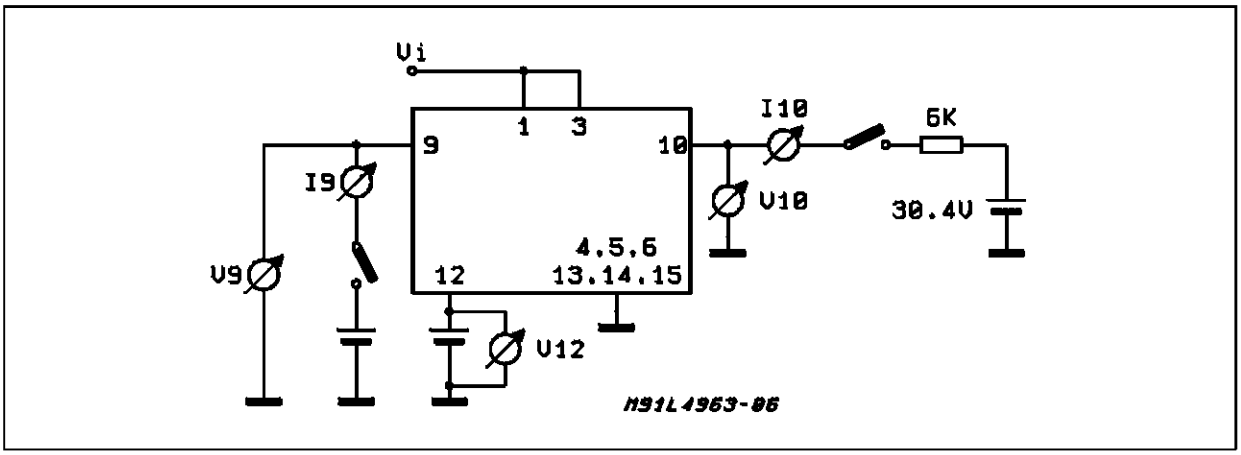


Figure 3c

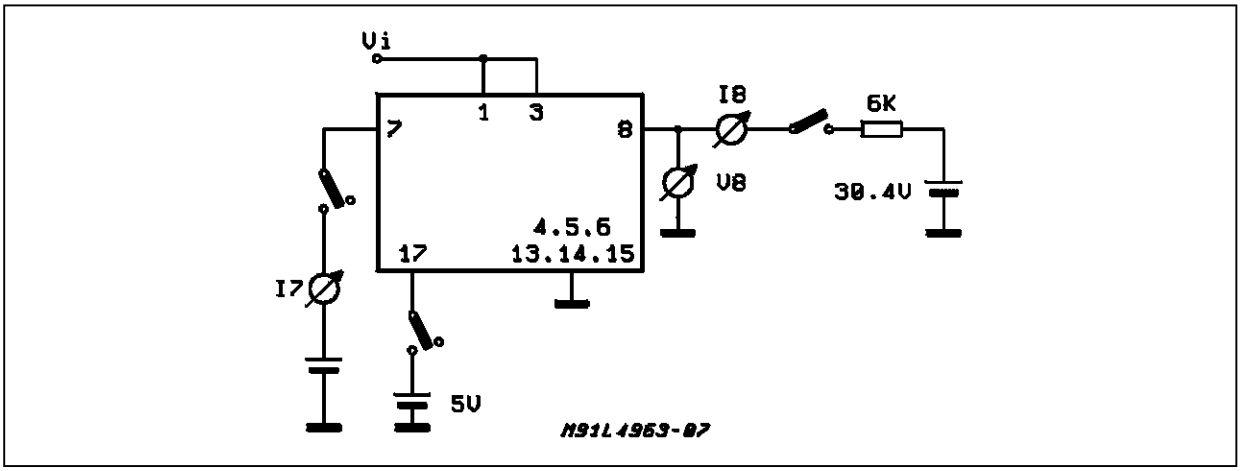


Figure 4: Quiescent Drain Current vs. Supply Voltage (0% Duty Cycle)

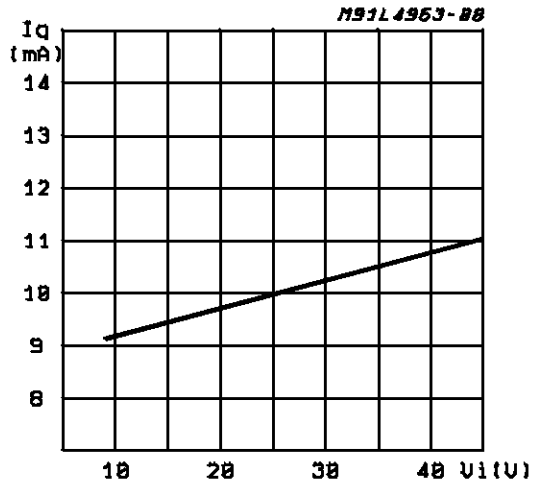


Figure 5: Quiescent Drain Current vs. Supply Voltage (100% Duty Cycle)

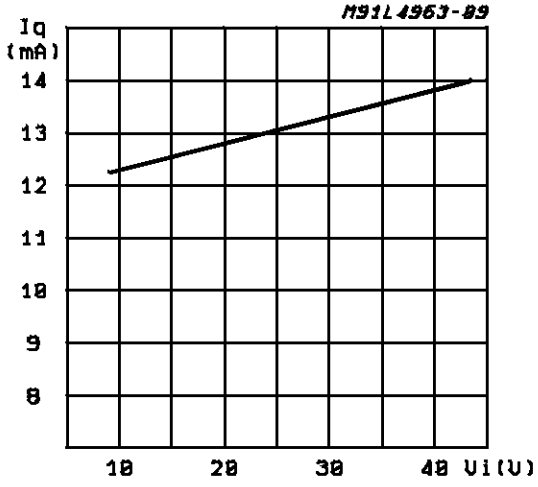


Figure 6: Quiescent Drain Current vs. Junction Temperature (0% Duty Cycle)

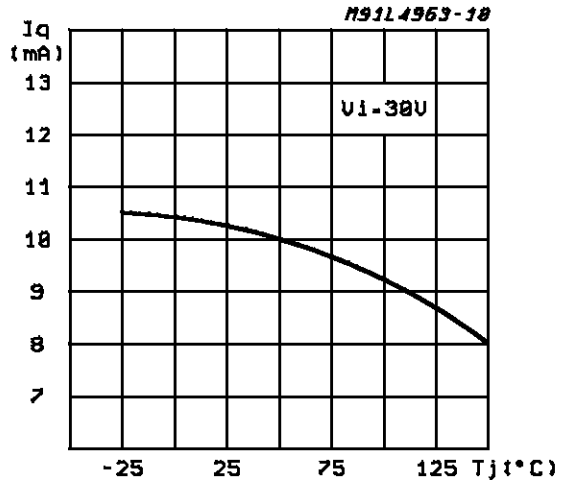


Figure 7: Quiescent Drain Current vs. Junction Temperature (100% Duty Cycle)

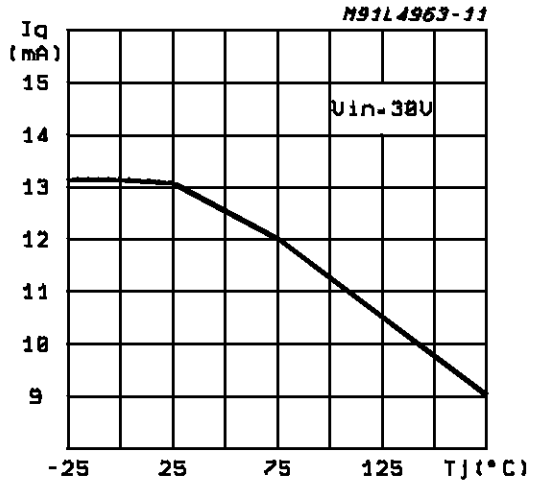


Figure 8: Reference Voltage vs. V_i

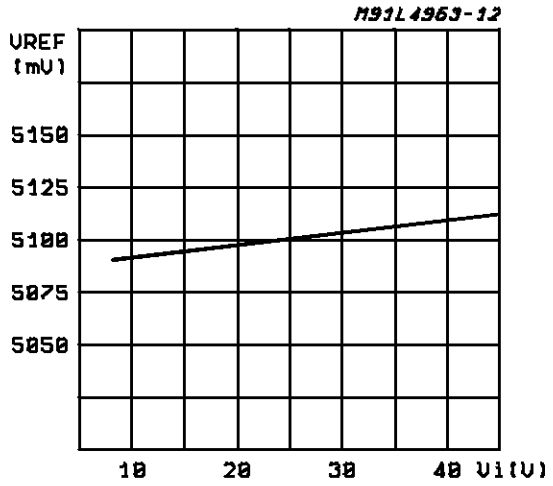


Figure 9: Reference Voltage vs. T_j

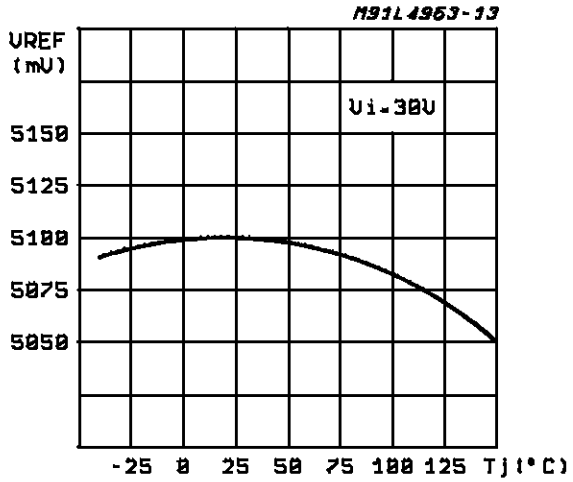


Figure 10: Line Transient Response

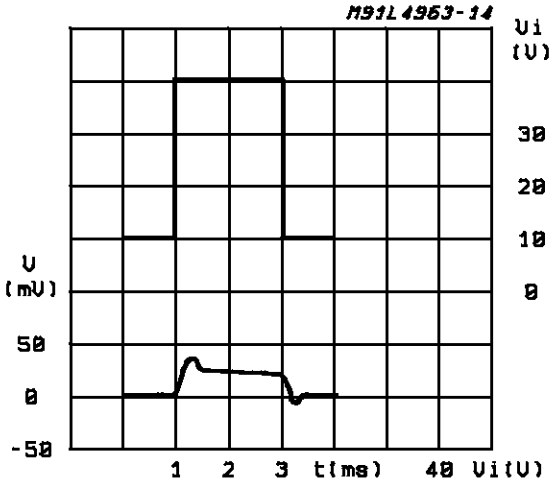


Figure 11: Load Transient

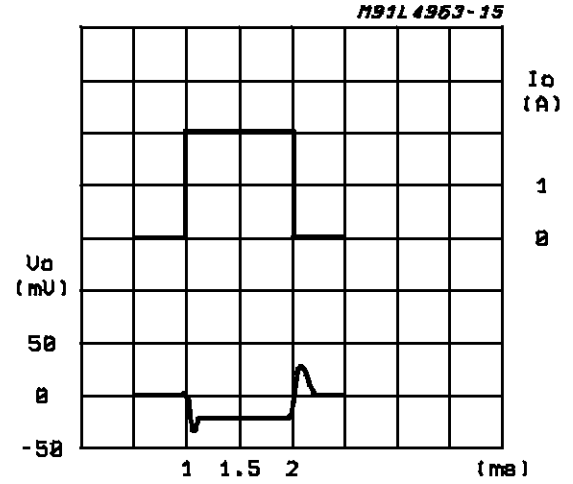


Figure 12: Supply Voltage Ripple Rejection vs. Frequency

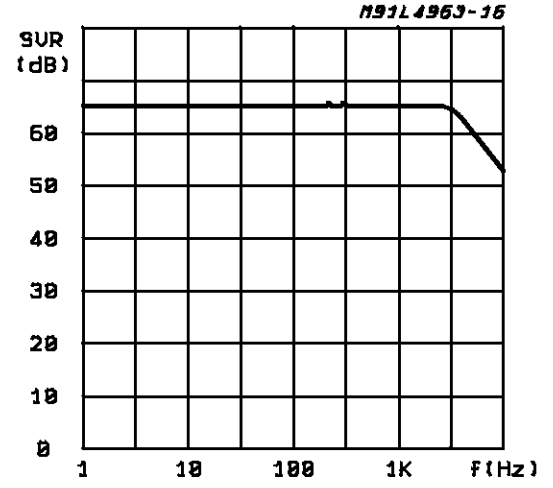


Figure 13: Dropout Voltage Between pi3 and 2 vs. Current at pin2

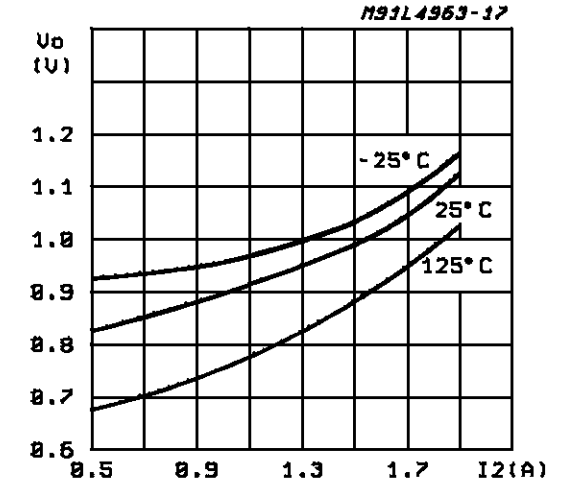


Figure 14: Dropout Voltage Between pin3 and 2 vs. Junction Temperature

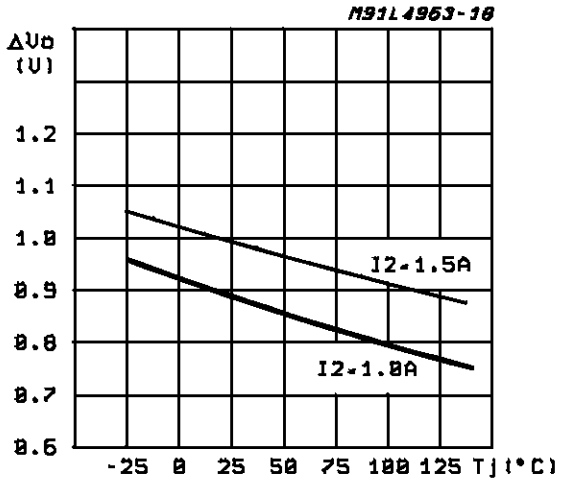


Figure 15: Maximum Allowable PowerDissipation vs. Ambient Temperature (Powerdip Package Only)

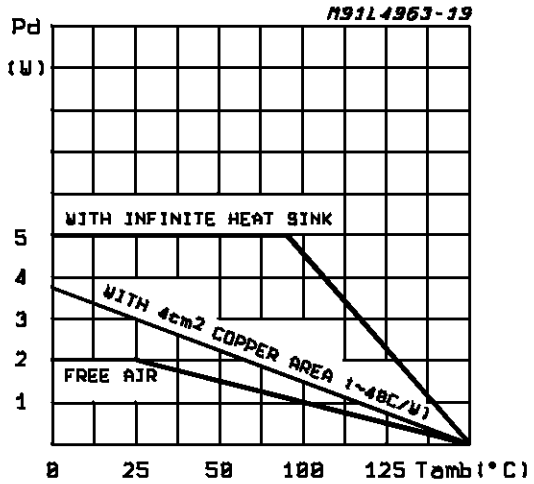


Figure 16: Power Dissipation (device only) vs. Input Voltage (Powerdip Package Only)

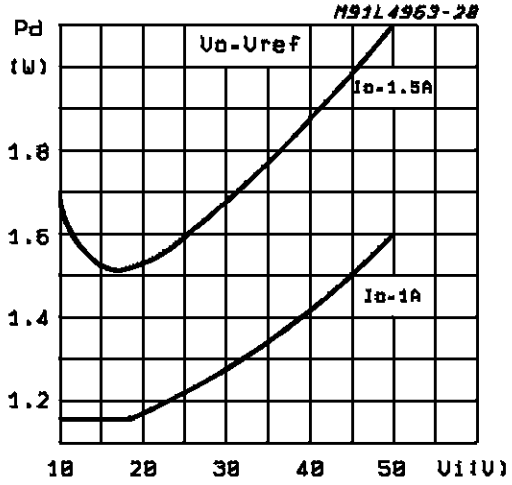


Figure 17: Power Dissipation (device only) vs. Output Voltage (Powerdip Package Only)

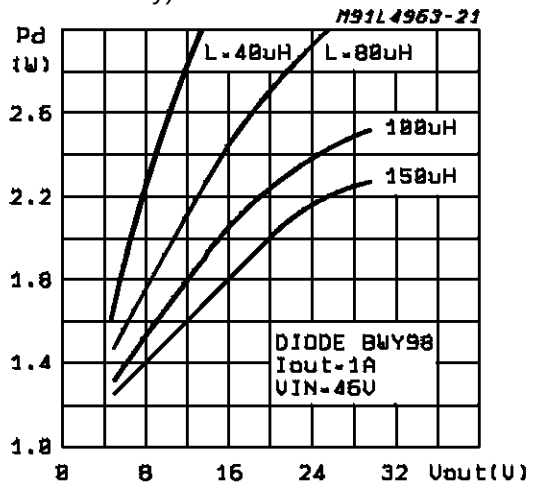


Figure 18: Voltage and Current Waveform at pin2

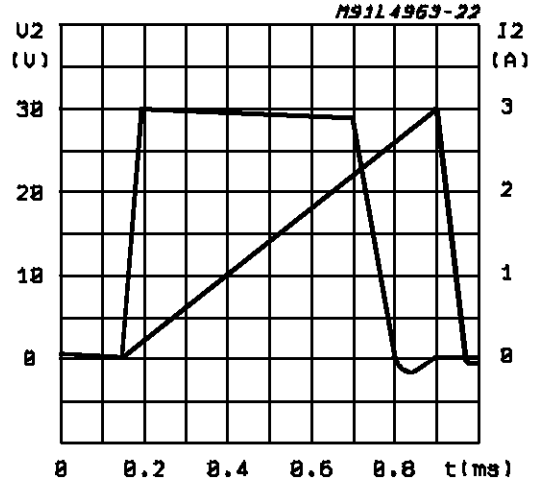


Figure 19: Efficiency vs. Output Current (Powerdip Package Only)

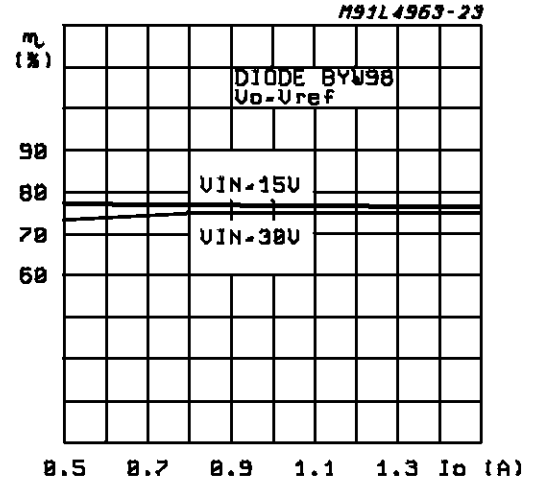


Figure 20: Efficiency vs. Output Voltage (Powerdip Package Only)

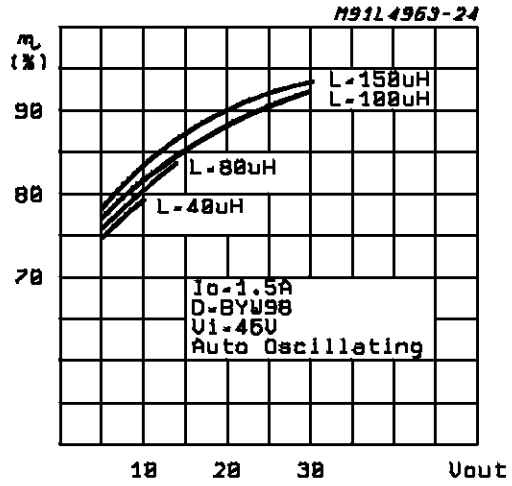


Figure 21: Current Limit vs. Junction Temperature V_i = 30V

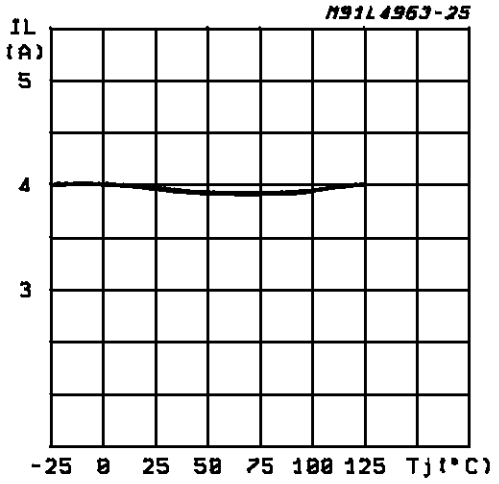


Figure 22: Current Limit vs. Input Voltage

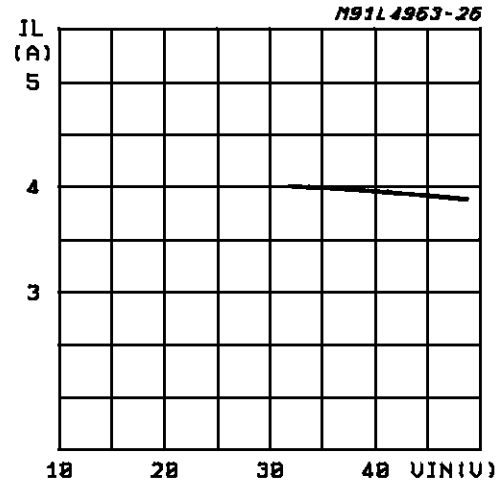


Figure 23: Oscillator Frequency vs. R2 (see fig. 26)

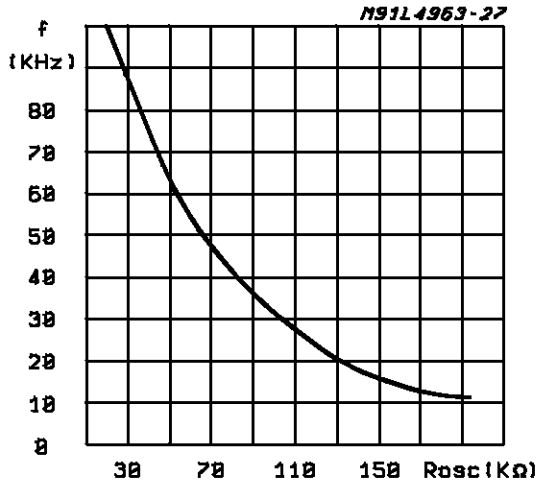


Figure 24: Oscillator Frequency vs. Junction Temperature

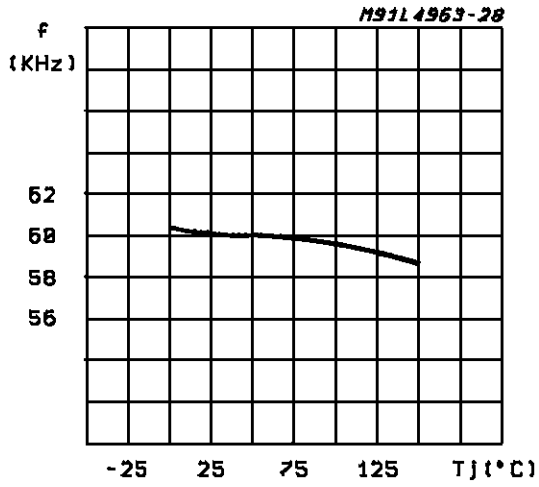


Figure 25: Oscillator Frequency vs. Input Voltage

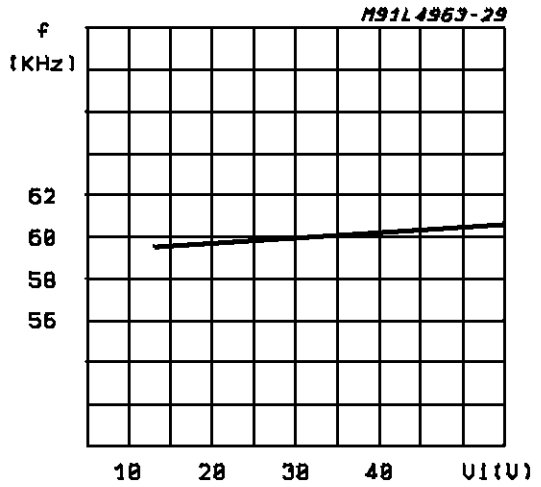
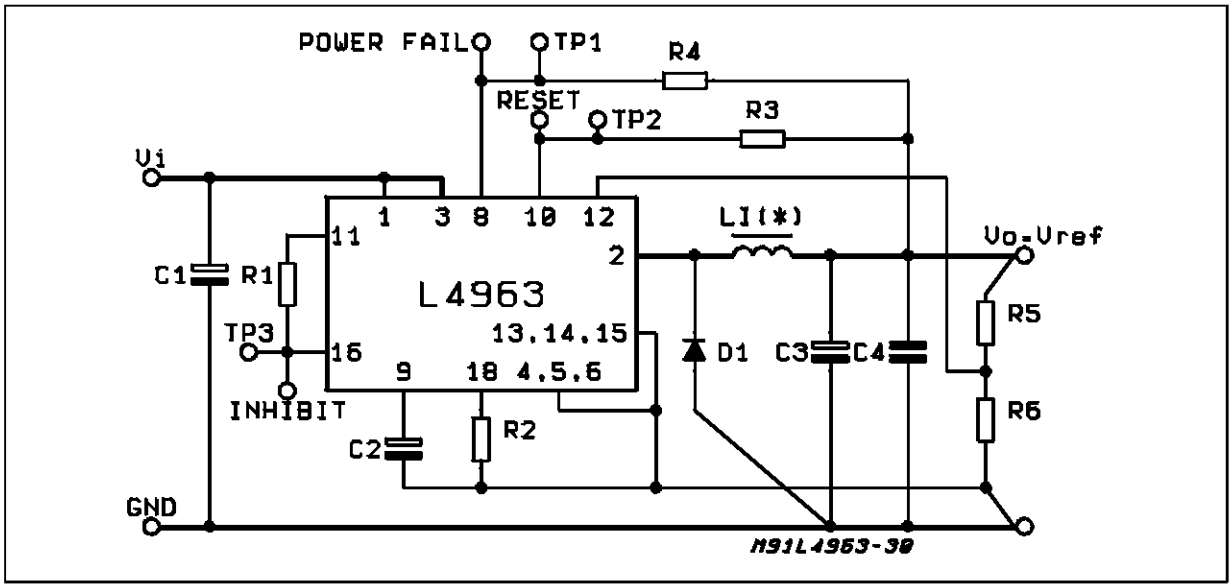


Figure 26: Evaluation Board Circuit



PART LIST

CAPACITOR	
C1	1000µF 50V EKR (*)
C2	2.2mF 16V
C3	1000µF 40V with low ESR
C4	1µF 50V film
RESISTOR	
R1	1KΩ
R2	51KΩ
R3	1KΩ
R4	1KΩ
R5, R6	see table

Resistor Values for Standard Output Voltages		
V_O	**R6**	**R5**
12	4.7KΩ	6.2KΩ
15	4.7KΩ	9.1KW
18	4.7KΩ	12KW
24	4.7KΩ	18KW

Diode: BYW98
Core: L = 40µH Magnetics 58121-A2MPP 34 Turns 0.9mm (20AWG)

(*) Minimum 100µF if V_i is a preregulated offline SMPS output or 1000µF if a 50Hz transformer plus rectifiers is used.

Figure 27: P.C. Board and Component Layout of the Circuit of fig. 26 (Powerdip Package) (1:1 scale).

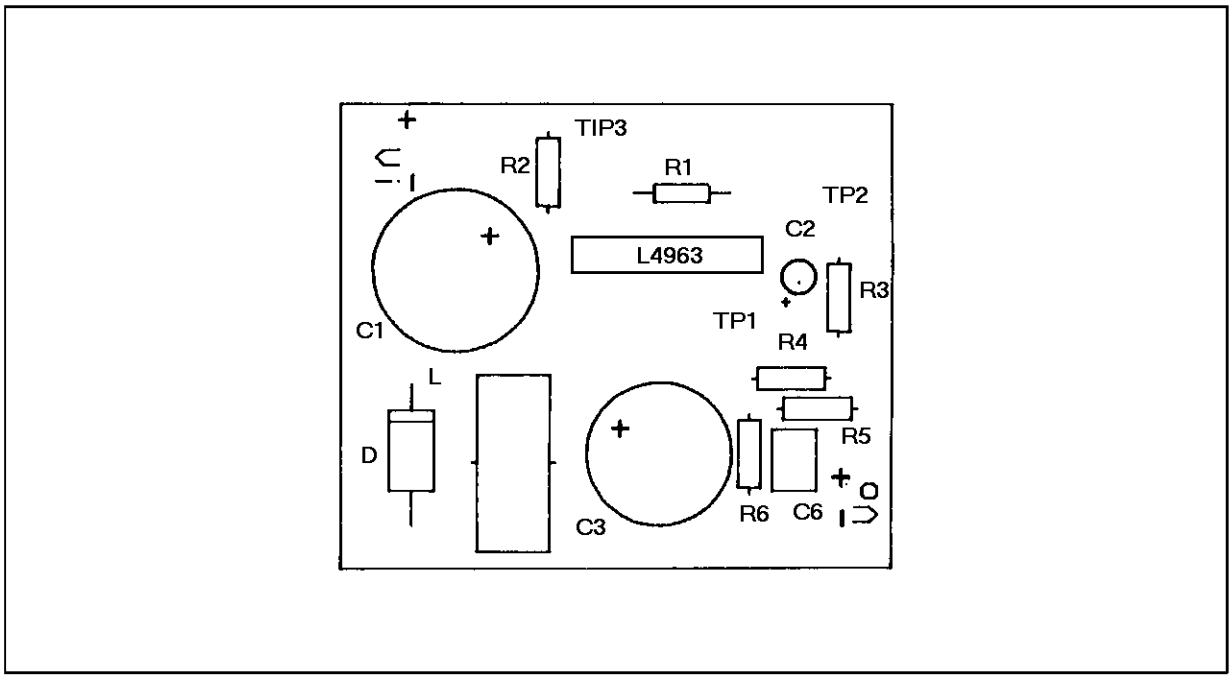


Figure 28: Thermal Characteristics

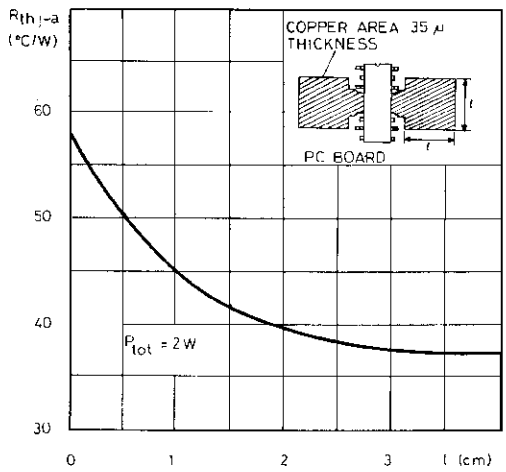


Figure 29: Junction to Ambient Thermal Resistance vs. Area on Board Heatsink (SO20)

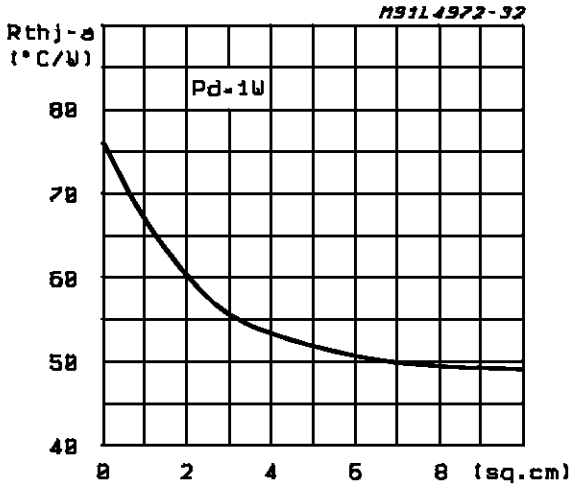


Figure 30: A Minimal 5.1 Fixed Regulator — Very Few Components are Required

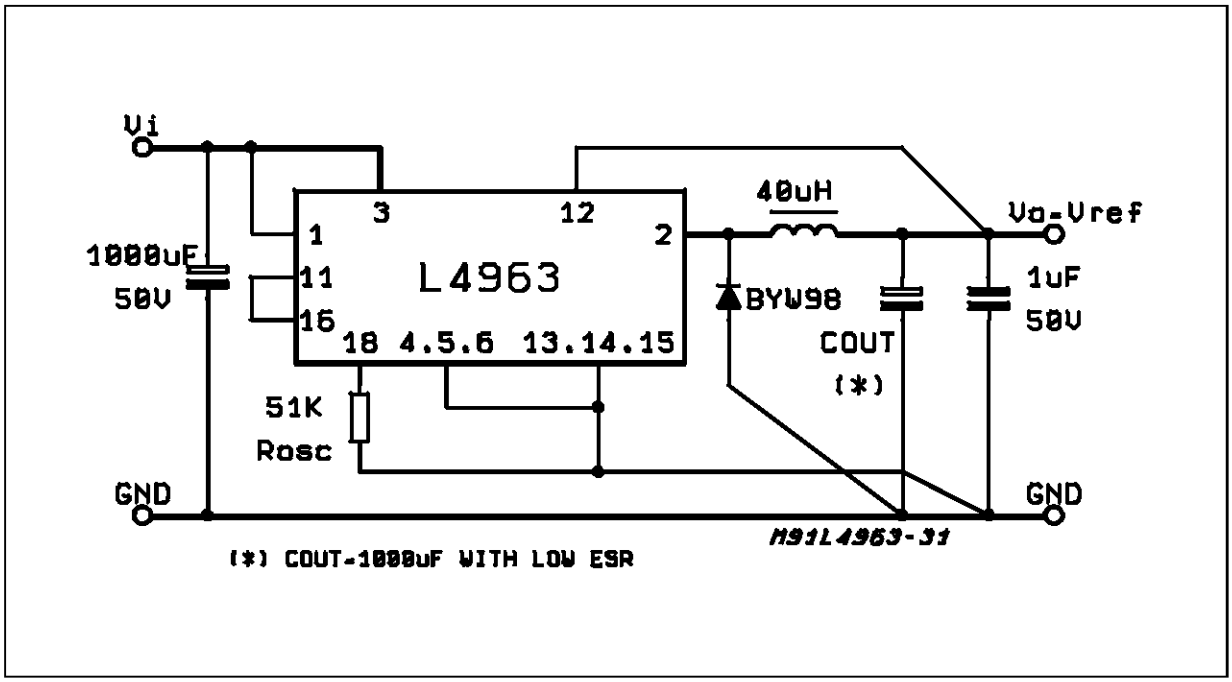
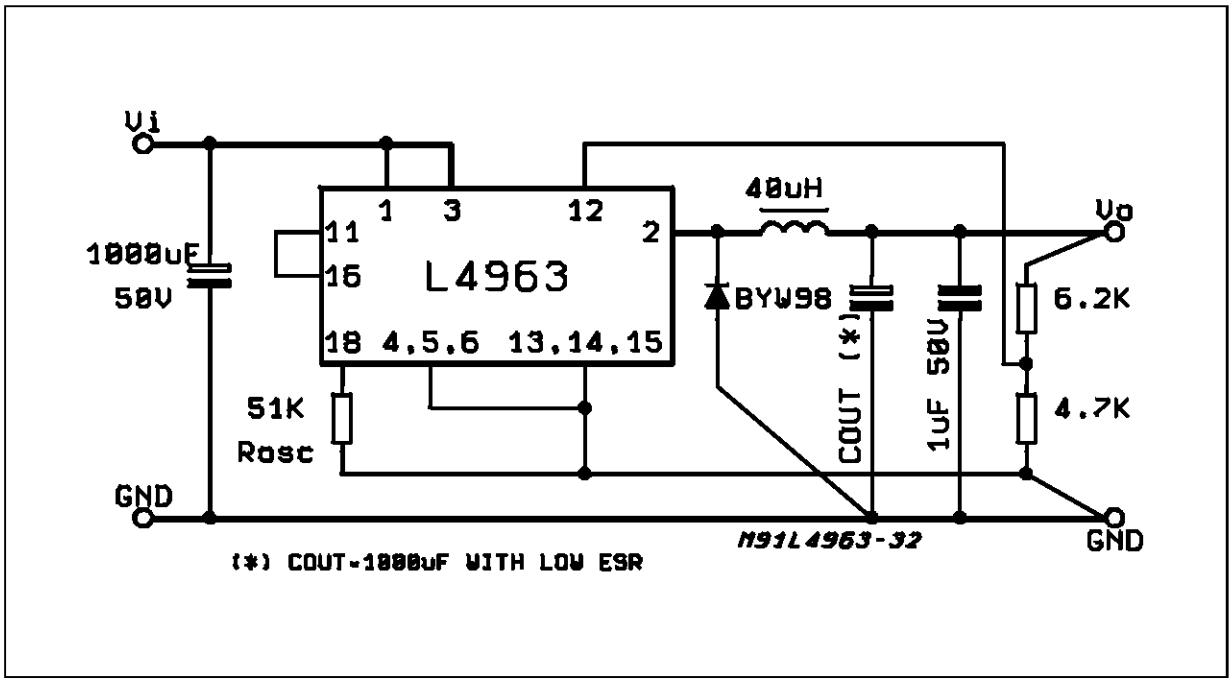
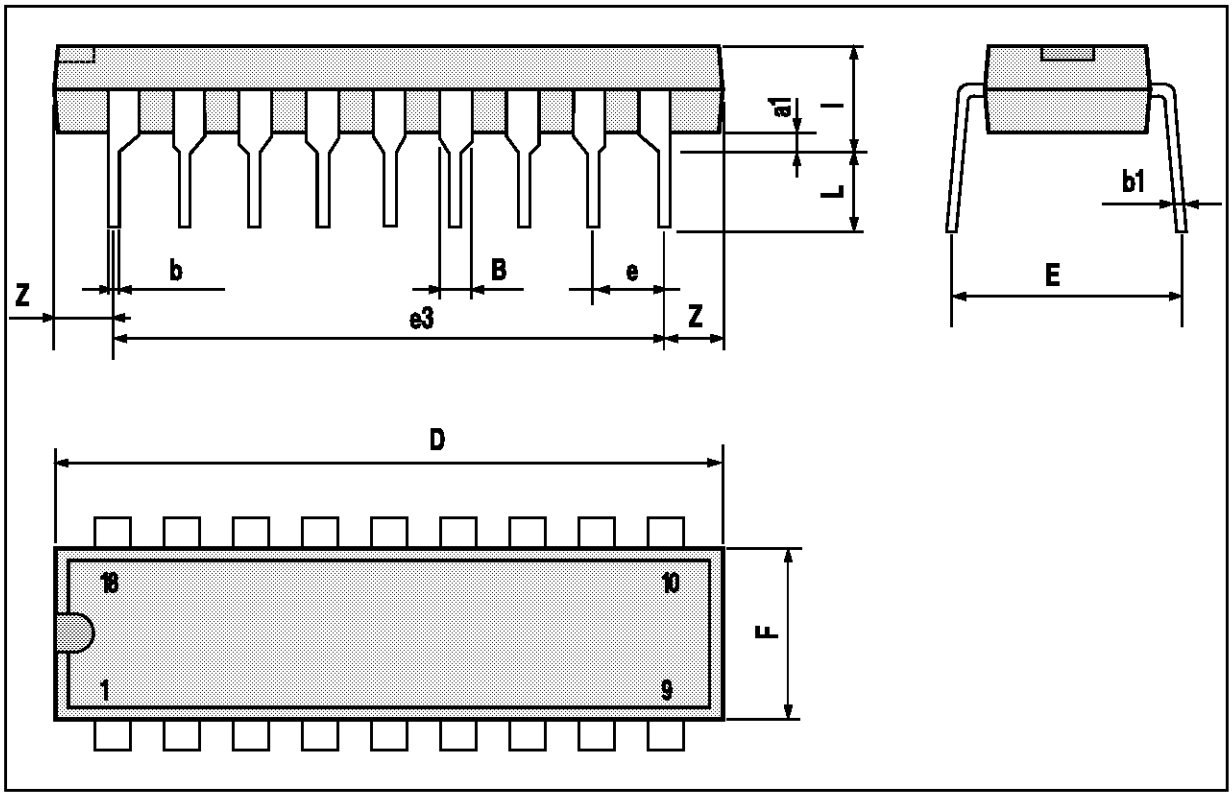


Figure 31: A Minimal Components count for V_O = 12V



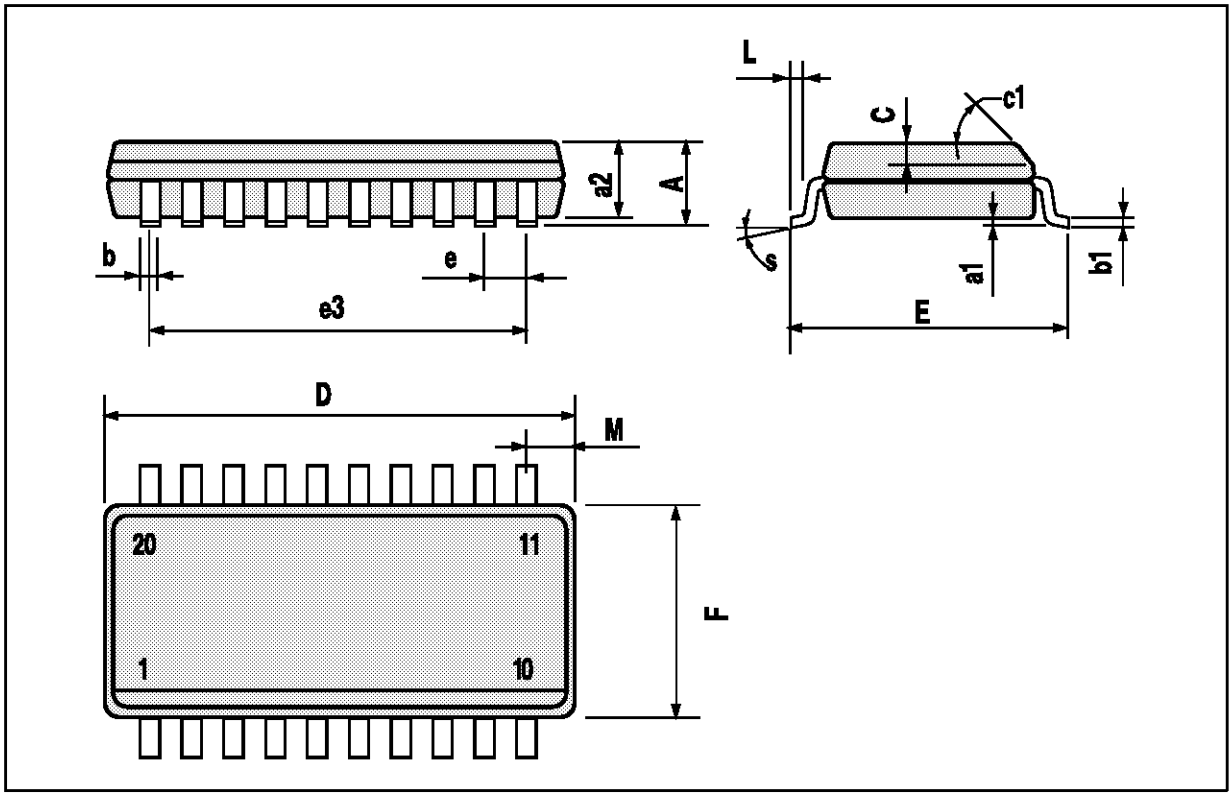
POWERDIP18 PACKAGE MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
a1	0.51			0.020		
B	0.85		1.40	0.033		0.055
b		0.50			0.020	
b1	0.38		0.50	0.015		0.020
D			24.80			0.976
E		8.80			0.346	
e		2.54			0.100	
e3		20.32			0.800	
F			7.10			0.280
I			5.10			0.201
L		3.30			0.130	
Z			2.54			0.100



SO20 PACKAGE MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			2.65			0.104
a1	0.1		0.3	0.004		0.012
a2			2.45			0.096
b	0.35		0.49	0.014		0.019
b1	0.23		0.32	0.009		0.013
C		0.5			0.020	
c1	45 (typ.)					
D	12.6		13.0	0.496		0.512
E	10		10.65	0.394		0.419
e		1.27			0.050	
e3		11.43			0.450	
F	7.4		7.6	0.291		0.299
L	0.5		1.27	0.020		0.050
M			0.75			0.030
S	8 (max.)					



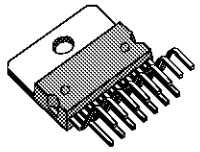
SGS-THOMSON MICROELECTRONICS

L4970A

10A SWITCHING REGULATOR

- 10A OUTPUT CURRENT
- 5.1V TO 40V OUTPUT VOLTAGE RANGE
- 0 TO 90% DUTY CYCLE RANGE
- INTERNAL FEED-FORWARD LINE REGULATION
- INTERNAL CURRENT LIMITING
- PRECISE 5.1V ± 2% ON CHIP REFERENCE
- RESET AND POWER FAIL FUNCTIONS
- SOFT START
- INPUT/OUTPUT SYNC PIN
- UNDER VOLTAGE LOCK OUT WITH HYSTERETIC TURN-ON
- PWM LATCH FOR SINGLE PULSE PER PERIOD
- VERY HIGH EFFICIENCY
- SWITCHING FREQUENCY UP TO 500KHz
- THERMAL SHUTDOWN
- CONTINUOUS MODE OPERATION

MULTIPOWER BCD TECHNOLOGY



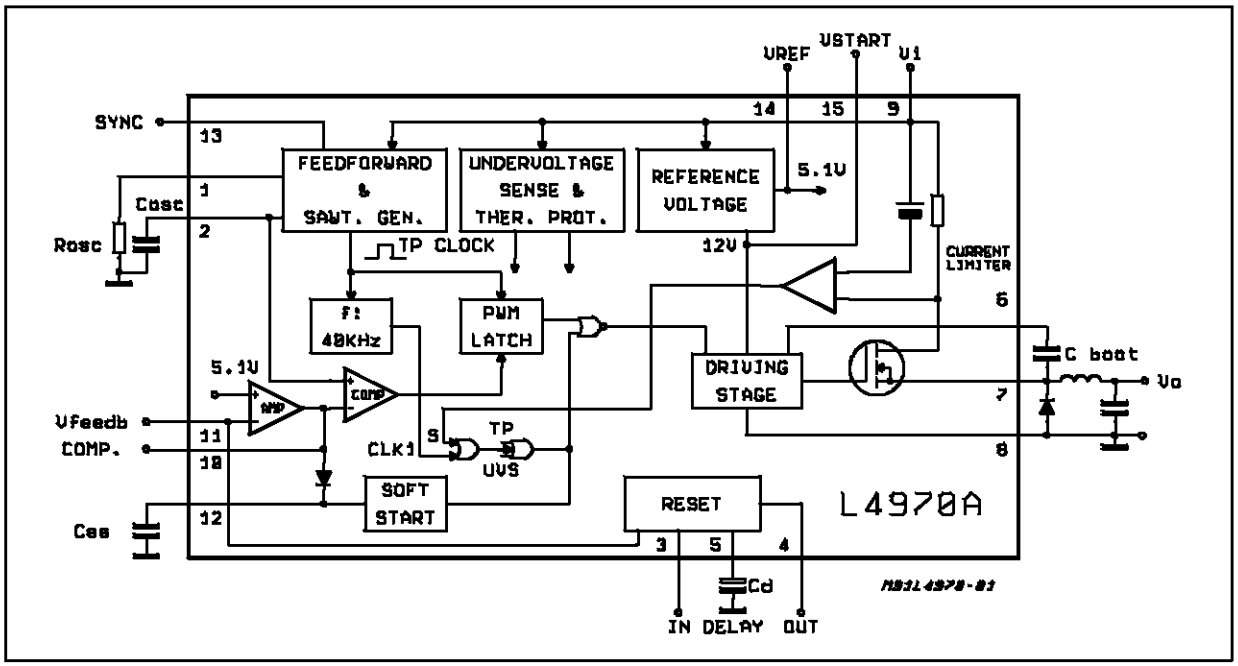
Multiwatt15V
ORDERING NUMBER: L4970A

DESCRIPTION

The L4970A is a stepdown monolithic power switching regulator delivering 10A at a voltage variable from 5.1 to 40V.

Realized with BCD mixed technology, the device uses a DMOS output transistor to obtain very high efficiency and very fast switching times. Features of the L4970A include reset and power fail for microprocessors, feed forward line regulation, soft start, limiting current and thermal protection. The device is mounted in a 15-lead multiwatt plastic power package and requires few external components. Efficient operation at switching frequencies up to 500KHz allows reduction in the size and cost of external filter components.

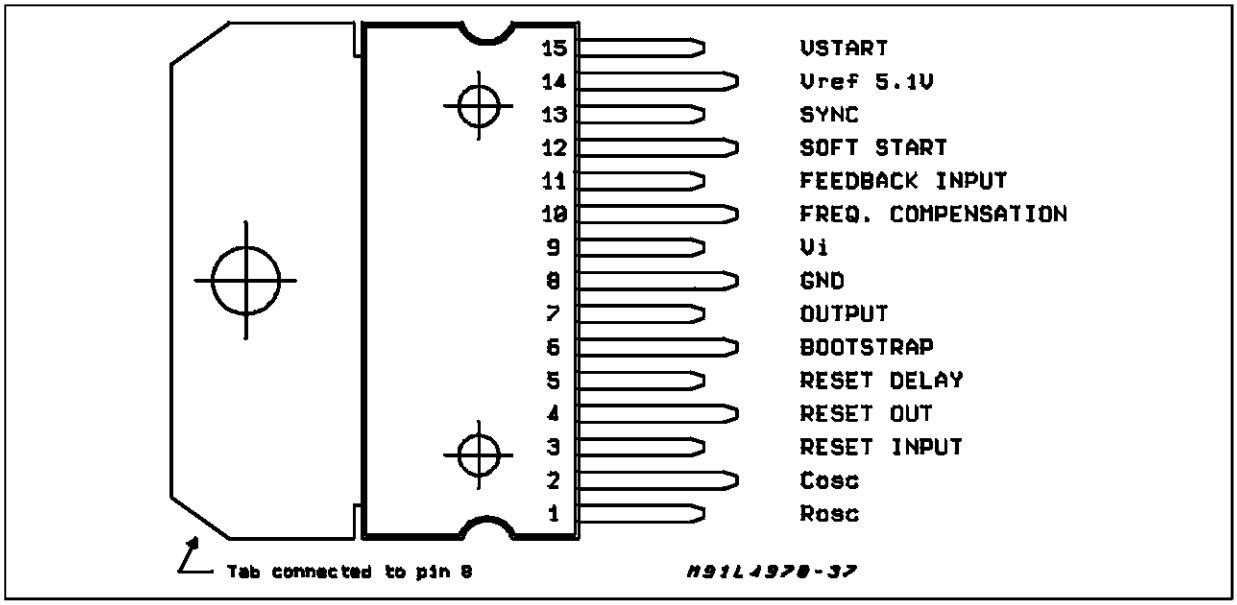
BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_9	Input Voltage	55	V
V_9	Input Operating Voltage	50	V
V_7	Output DC Voltage Output Peak Voltage at t = 0.1µs f = 200KHz	-1 -7	V V
I_7	Maximum Output Current	Internally Limited	
V_6	Bootstrap Voltage Bootstrap Operating Voltage	65 V_9 + 15	V V
V_3, V_{12}	Input Voltage at Pins 3, 12	12	V
V_4	Reset Output Voltage	50	V
I_4	Reset Output Sink Current	50	mA
V_5, V_{10}, V_{11}, V_{13}	Input Voltage at Pin 5, 10, 11, 13	7	V
I_5	Reset Delay Sink Current	30	mA
I_{10}	Error Amplifier Output Sink Current	1	A
I_{12}	Soft Start Sink Current	30	mA
P_{tot}	Total Power Dissipation at T_{case} < 120°C	30	W
T_j, T_{stg}	Junction and Storage Temperature	-40 to 150	°C

PIN CONNECTION (Top view)



THERMAL DATA

Symbol	Parameter		Value	Unit
$R_{th\ j\text{-}case}$	Thermal Resistance Junction-case	max	1	°C/W
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient	max	35	°C/W

PIN FUNCTIONS

N°	Name	Function
1	OSCILLATOR	R_{osc}. External resistor connected to ground determines the constant charging current of C_{osc}.
2	OSCILLATOR	C_{osc}. External capacitor connected to ground determines (with R_{osc}) the switching frequency.
3	RESET INPUT	Input of Power Fail Circuit. The threshold is 5.1V. It may be connected via a divider to the input for power fail function. It must be connected to the pin 14 an external 30KΩ resistor when power fail signal not required.
4	RESET OUT	Open Collector Reset/power Fail Signal Output. This output is high when the supply and the output voltages are safe.
5	RESET DELAY	A C_d capacitor connected between this terminal and ground determines the reset signal delay time.
6	BOOTSTRAP	A C_{boot} capacitor connected between this terminal and the output allows to drive properly the internal D-MOS transistor.
7	OUTPUT	Regulator Output.
8	GROUND	Common Ground Terminal
9	SUPPLY VOLTAGE	Unregulated Input Voltage.
10	FREQUENCY COMPENSATION	A series RC network connected between this terminal and ground determines the regulation loop gain characteristics.
11	FEEDBACK INPUT	The Feedback Terminal of the Regulation Loop. The output is connected directly to this terminal for 5.1V operation; It is connected via a divider for higher voltages.
12	SOFT START	Soft Start Time Constant. A capacitor is connected between thi sterminal and ground to define the soft start time constant.
13	SYNC INPUT	Multiple L4970A are synchronized by connecting pin 13 inputs together or via an external syncr. pulse.
14	V_{ref}	5.1V V_{ref} Device Reference Voltage.
15	V_{start}	Internal Start-up Circuit to Drive the Power Stage.

CIRCUIT OPERATION (refer to the block diagram)

The L4970A is a 10A monolithic stepdown switching regulator working in continuous mode realized in the new BCD Technology. This technology allows the integration of isolated vertical DMOS power transistors plus mixed CMOS/Bipolar transistors.

The device can deliver 10A at an output voltage adjustable from 5.1V to 40V, and contains diagnostic and control functions that make it particularly suitable for microprocessor based systems.

BLOCK DIAGRAM

The block diagram shows the DMOS power transistor and the PWM control loop. Integrated functions include a reference voltage trimmed to 5.1V ± 2%, soft start, undervoltage lockout, oscillator with feedforward control, pulse by pulse current limit, thermal shutdown and finally the reset and power fail circuit. The reset and power fail circuit provides an output signal for a microprocessor indicating the status of the system.

Device turn on is around 11V with a typical 1V hysteresis, this threshold provides a correct voltage for the driving stage of the DMOS gate and the hysteresis prevents instabilities.

An external bootstrap capacitor charged to 12V by an internal voltage reference is needed to provide correct gate drive to the power DMOS. The driving circuit is able to source and sink peak currents of around 0.5A to the gate of the DMOS transistor. A typical switching time of the current in the DMOS transistor is 50ns. Due to the fast commutation switching frequencies up to 500kHz are possible.

The PWM control loop consists of a sawtooth oscillator, error amplifier, comparator, latch and the output stage. An error signal is produced by comparing the output voltage with the precise 5.1V ± 2% on chip reference. This error signal is then compared with the sawtooth oscillator, in order to generate a fixed frequency pulse width modulated drive for the output stage. A PWM latch is included to eliminate multiple pulsing within a period even in noisy environments. The gain and

Figure 1: Feedforward Waveform

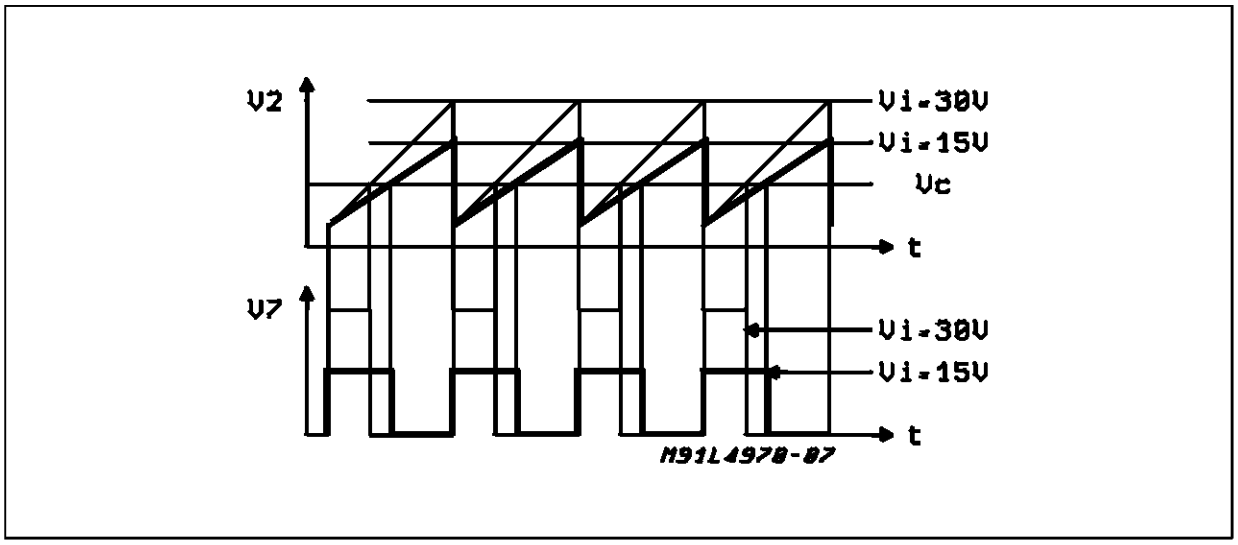


Figure 2: Soft Start Function

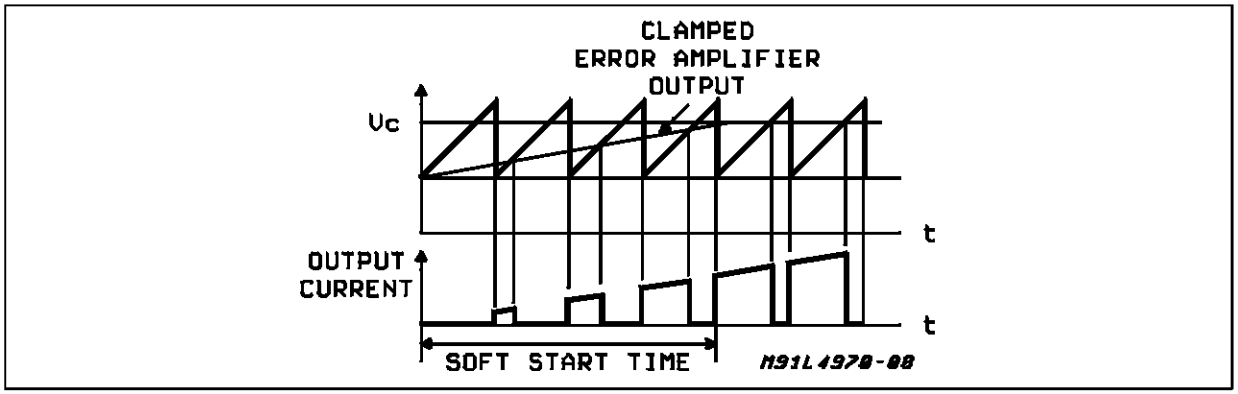
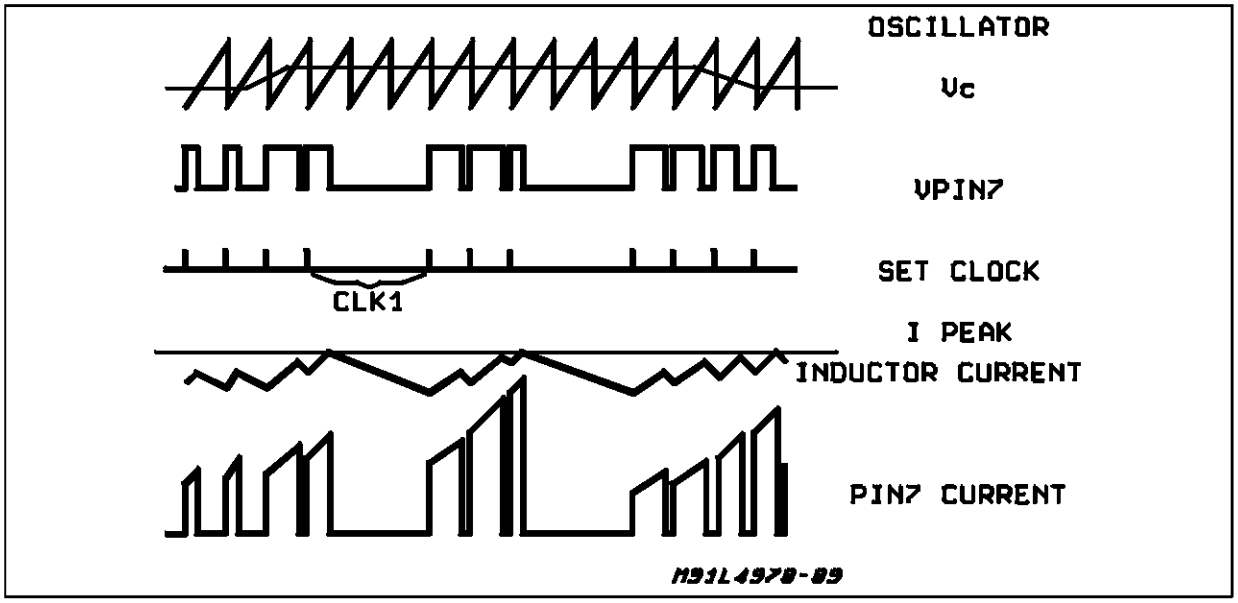


Figure 3: Limiting Current Function



stability of the loop can be adjusted by an external RC network connected to the output of the error amplifier. A voltage feedforward control has been added to the oscillator, this maintains superior line regulation over a wide input voltage range. Closing the loop directly gives an output voltage of 5.1V, higher voltages are obtained by inserting a voltage divider.

At turn on output overcurrents are prevented by the soft start function (fig. 2). The error amplifier is initially clamped by an external capacitor Css and allowed to rise linearly under the charge of an internal constant current source.

Output overload protection is provided by a current limit circuit (fig. 3). The load current is sensed by an internal metal resistor connected to a comparator. When the load current exceeds a preset threshold the output of the comparator sets a flip flop which turns off the power DMOS. The next clock pulse, from an internal 40kHz oscillator will reset the flip flop and the power DMOS will again conduct. This current protection method, ensures a constant current output when the system is overloaded or short circuited and limits the switching frequency, in this condition, to 40kHz.

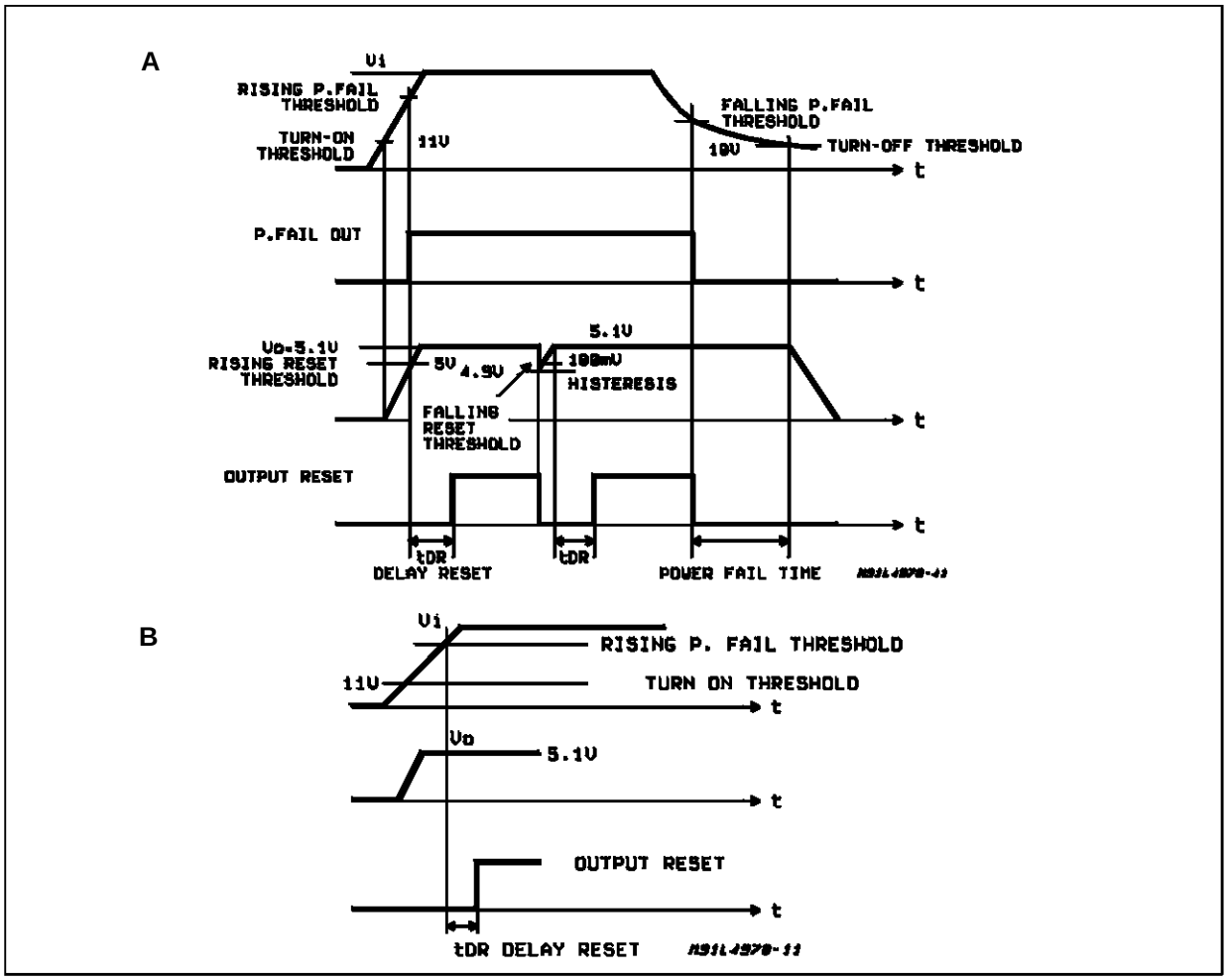
The Reset and Power fail circuitry (fig 4) generates an output signal when the supply voltage exceeds a threshold programmed by an external voltage divider. The reset signal, is generated with a delay time programmed by an external capacitor on the delay pin. When the supply voltage falls below the threshold or the output voltage goes below 5V the reset output goes low immediately. The reset output is an open collector-drain.

Fig 4A shows the case when the supply voltage is higher than the threshold, but the output voltage is not yet 5V.

Fig 4B shows the case when the output is 5.1V but the supply voltage is not yet higher than the fixed threshold.

The thermal protection disables circuit operation when the junction temperature reaches about 150°C and has an hysterysis to prevent unstable conditions.

Figure 4: Reset and Power Fail Functions.



ELECTRICAL CHARACTERISTICS (Refer to the test circuit, T_j = 25°C, V_i = 35V, R_4 = 16KΩ, C_9 = 2.2nF, f_{SW} = 200KHz typ, unless otherwise specified)

DYNAMIC CHARACTERISTICS

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit	Fig.
V_i	input Voltage Range (pin 9)	V_o = V_{ref} to 40V I_o = 10A	15		50	V	5
V_o	Output Votage	V_i = 15V to 50V I_o = 5A; V_o = V_{ref}	5	5.1	5.2	V	5
ΔV_o	Line Regulation	V_i = 15V to 50V I_o = 5A; V_o = V_{ref}		12	30	mV	5
ΔV_o	Load Regulation	V_o = V_{ref} I_o = 3A to 6A I_o = 2A to 10A		 10 20	 30 50	 mV mV	5
V_d	Dropout Voltage Between Pin 9 and 7	I_o = 5A I_o = 10A		0.55 1.1	0.8 1.6	V V	5
I_{7L}	Max. Limiting Current	V_i = 15 to 50V	11	13	15	A	5
η	Efficiency	I_o = 5A V_o = V_{ref} V_o = 12V	80	 85 92		 % %	5
		I_o = 10A V_o = V_{ref} V_o = 12V	75	 80 87		 % %	5
SVR	Supply Voltage Ripple Reject.	V_i = 2VRMS; I_o = 5A f = 100Hz; V_o = V_{ref}	56	60		dB	5
f	Switching Frequency		180	200	220	KHz	5
$\frac{\Delta f}{\Delta V_i}$	Voltage Stability of Swiching Frequency	V_i = 15V to 45V		2	6	%	5
$\frac{\Delta f}{T_j}$	Temperature Stability of Swiching Frequency	T_j = 0 to 125°C		1		%	5
f_{max}	Maximum Operating Switching Frequency	V_o = V_{ref}; R_4 = 10KΩ I_o = 10A; C_9 = 1nF	500			KHz	5

V_{ref} SECTION (pin 14)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit	Fig.
V_{14}	Reference Voltage		5	5.1	5.2	V	7
ΔV_{14}	Line Regulation	V_i = 15V to 50V		10	25	mV	7
ΔV_{14}	Load Regulation	I_{14} = 0 to 1mA		20	40	mV	7
$\frac{\Delta V_{14}}{\Delta T}$	Average Temperature Coefficient Reference Voltage	T_j = 0°C to 125°C		0.4		mV/°C	7
$I_{14\ short}$	Short Circuit Current Limit	V_{14} = 0		70		mA	7

V_{START} SECTION (pin 15)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit	Fig.
V_{15}	Reference Voltage		11.4	12	12.6	V	7
ΔV_{15}	Line Regulation	V_i = 15 to 50V		0.6	1.4	V	7
ΔV_{15}	Load Regulation	I_{15} = 0 to 1mA		50	200	mV	7
$I_{15\ short}$	Short Circuit Current Limit	V_{15} = 0V		80		mA	7

ELECTRICAL CHARACTERISTICS (continued)

DC CHARACTERISTICS

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit	Fig.
V_{9on}	Turn-on Threshold		10	11	12	V	7A
$V_{9\ Hyst}$	Turn-off Hysteresys			1		V	7A
I_{9Q}	Quiescent Current	V_{12} = 0; S1 = D		13	19	mA	7A
I_{9OQ}	Operating Supply Current	V_{12} = 0; S1 = C; S2 = B		16	23	mA	7A
I_{7L}	Out Leak Current	V_i = 55V; S3 = A; V_{12} = 0			2	mA	7A

SOFT START

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit	Fig.
I_{12}	Soft Start Source Current	V_{12} = 3V; V_{11} = 0V	70	100	130	µA	7B
V_{12}	Output Saturation Voltage	I_{12} = 20mA; V_9 = 10V			1	V	7B
		I_{12} = 200µA; V_9 = 10V			0.7	V	7B

ERROR AMPLIFIER

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit	Fig.
V_{10H}	High Level Out Voltage	I_{10} = -100µA; S1 = C V_{11} = 4.7V	6			V	7C
V_{10L}	Low Level Out Voltage	I_{10} = +100µA; S1 = C V_{11} = 5.3V;			1.2	V	7C
I_{10H}	Source Output Current	V_{10} = 1V; S1 = E V_{11} = 4.7V	100	150		µA	7C
I_{10L}	Sink Output Current	V_{10} = 6V; S1 = D V_{11} = 5.3V	100	150		µA	7C
I_{11}	Input Bias Current	R_S = 10KΩ		0.4	3	µA	–
G_V	DC Open Loop Gain	V_{VCM} = 4V; R_S = 10Ω	60			dB	–
SVR	Supply Voltage Rejection	15 < V_i < 50V; R_S = 10Ω	60	80		dB	–
V_{OS}	Input Offset Voltage	R_S = 50Ω		2	10	mV	–

RAMP GENERATOR (pin 2)

Symbol	Parameter	Test Condition		Min.	Typ.	Max.	Unit	Fig.
V_2	Ramp Valley	S1 = C; S2 = B		1.2	1.5		V	7A
V_2	Ramp Peak	S1 = C;	V_i = 15V		2.5		V	7A
		S2 = B;	V_i = 45V		5.5		V	7A
I_2	Min. Ramp Current	S1 = A; I_1 = 100µA			270	300	µA	7A
I_2	Max. Ramp Current	S1 = A; I1 = 1mA		2.4	2.7		mA	7A

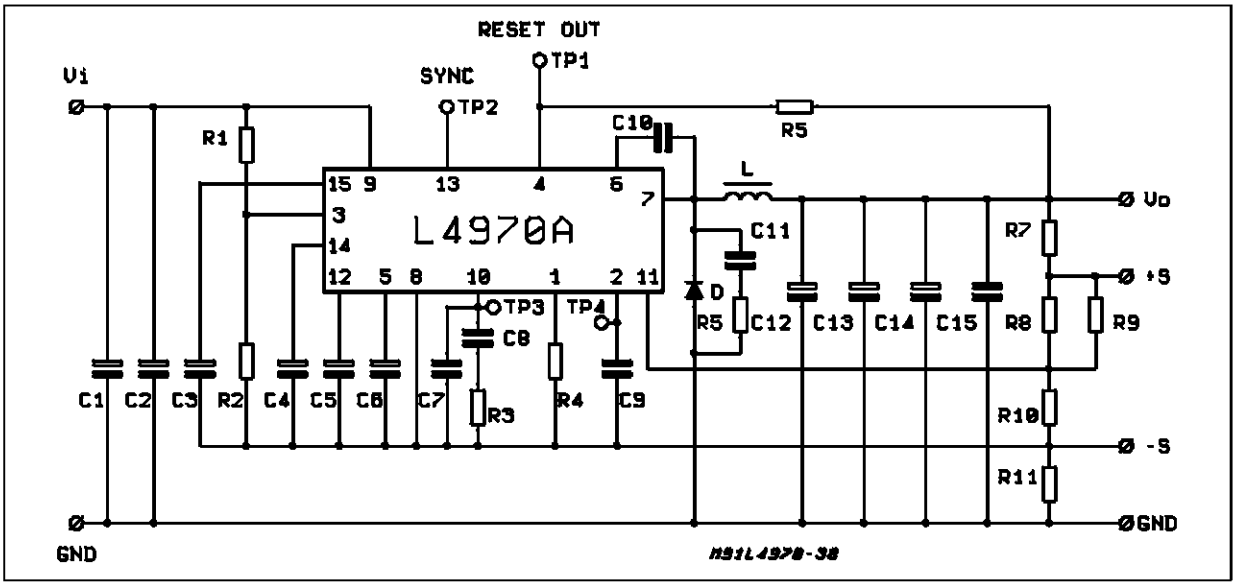
SYNC FUNCTION (pin 13)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit	Fig.
V_{13}	Low Input Voltage	V_i = 15V to 50V; V_{12} = 0; S1 = C; S2 = B; S4 = B	–0.3		0.9	V	7A
V_{13}	High Input voltage	V_{12} = 0; S1 = C; S2 = B; S4 = B	3.5		5.5	V	7A
I_{13L}	Sync Input Current with Low Input Voltage	V_{13} = V_2 = 0.9V; S4 = A; S1 = C; S2 = B			0.4	mA	7A
I_{13H}	Input Current with High Input Voltage	V_{13} = 3.5V; S4 = A; S1 = C; S2 = B			1.5	mA	7A
V_{13}	Output Amplitude		4	5		V	–
t_W	Output Pulse Width	V_{thr} = 2.5V	0.3	0.5	0.8	µs	–

ELECTRICAL CHARACTERISTICS (continued)
RESET AND POWER FAIL FUNCTIONS

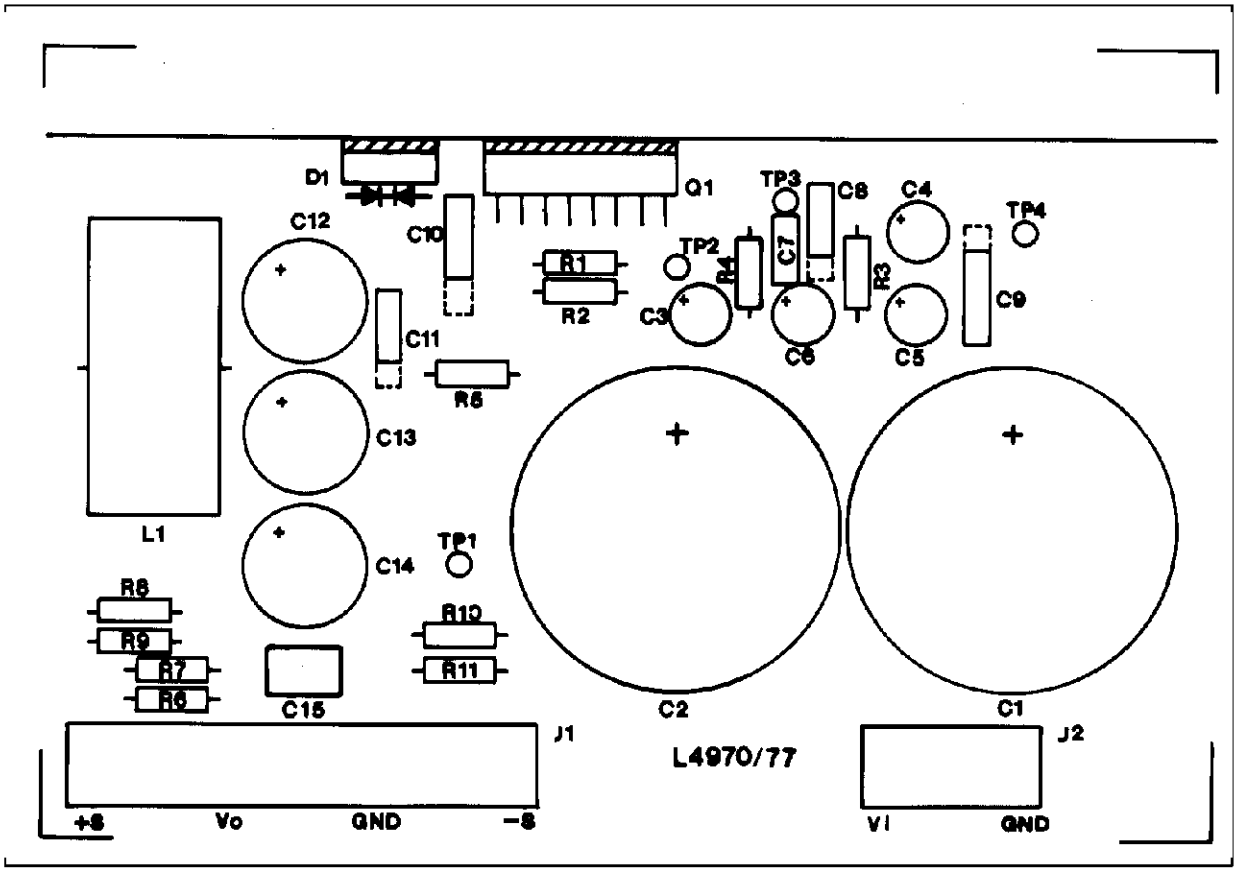
Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit	Fig.
V_{11R}	Rising Threshold Voltage (pin 11)	V_i = 15 to 50V V_3 = 5.3V	V_{ref} –120	V_{ref} –100	V_{ref} –80	V mV	7D
V_{11F}	Falling Threshold Voltage (pin 11)	Vi = 15 to 50V V_3 = 5.3V	4.77	V_{ref} –200	V_{ref} –160	V mV	7D
V_{5H}	Delay High Threshold Voltage	V_i = 15 to 50V V_{14} = V_{11} V_3 = 5.3V	4.95	5.1	5.25	V	7D
V_{5L}	Delay Low Threshold Voltage	Vi = 15 to 50V V_{14} = V_{11} V_3 = 5.3V	1	1.1	1.2	V	7D
$-I_{5SO}$	Delay Source Current	V_3 = 5.3V; V_5 = 3V	40	60	80	µA	7D
I_{5SI}	Delay Sink Current	V_3 = 4.7V; V_5 = 3V	10			mA	7D
V_{4S}	Out Saturation Voltage	I_4 = 15mA; S1 = B V_3 = 4.7V			0.4	V	7D
I_4	Output Leak Current	V_4 = 50V; S1 = A V_3 = 5.3V			100	µA	7D
V_{3R}	Rising Threshold Voltage	V_{11} = V_{14}	4.95	5.1	5.25	V	7D
V_{3H}	Hysteresys		0.4	0.5	0.6	V	7D
I_3	Input Bias Current			1	3	µA	7D

Figure 5: Test and Evaluation Board Circuit



TYPICAL PERFORMANCES (using evaluation board) :
n = 83% (V_i = 35V ; V_o = V_{REF} ; I_o = 10A ; f_{SW} = 200KHz)
$V_{o\ RIPPLE}$ = 30mV (at 10A) with output filter capacitor ESR ≤ 60mΩ
Line regulation = 5mV (V_i = 15 to 50V)
Load regulation = 15mV (I_o = 2 to 10A)
For component values, refer to test circuit part list.

Figure 6a: P.C. Board (components side) and Components Layout of Figure 5 (1:1 scale).



PARTS LIST

R_1 = 30KΩ	C_1, C_2 = 3300µF 63V_L EYF (ROE
R_2 = 10KΩ	C_3, C_4, C_5, C_6 = 2.2µF
R_3 = 15KΩ	C_7 = 390pF Film
R_4 = 16KΩ	C_8 = 22nF MKT 1817 (ERO)
R_5 = 22Ω 0,5W	
R_6 = 4K7	C_9 = 2.2nF KP1830
R_7 = 10Ω	C_{10} = 220nF MKT
R_8 = see tab. A	C_{11} = 2.2nF MP1830
R_9 = OPTION	**C_{12}, C_{13}, C_{14} = 220µF 40V_L EKR
R_{10} = 4K7	C_{15} = 1µF Film
R_{11} = 10Ω	
D1 = MBR 1560CT (or 16A/60V or equivalent)	
L1 = 40µH	core 58071 MAGNETICS 27 TURNS Ø 1,3mm (AWG 16) COGEMA 949178

* 2 capacitors in parallel to increase input RMS current capability
** 3 capacitors in parallel to reduce total output ESR

Table A

V_0	R_9	R_7
12V	4.7kΩ	6.2kW
15V	4.7kΩ	9.1kΩ
18V	4.7kΩ	12kΩ
24V	4.7kΩ	18kΩ

Table B
SUGGESTED BOOTSTRAP CAPACITORS

Operating Frequency	Bootstrap Cap.c10
f = 20KHz	≥680nF
f = 50KHz	≥470nF
f = 100KHz	≥330nF
f = 200KHz	≥220nF
f = 500KHz	≥100nF

Figure 6b: P.C. Board (Back side) and Components Layout of the Circuit of Fig. 5. (1:1 scale)

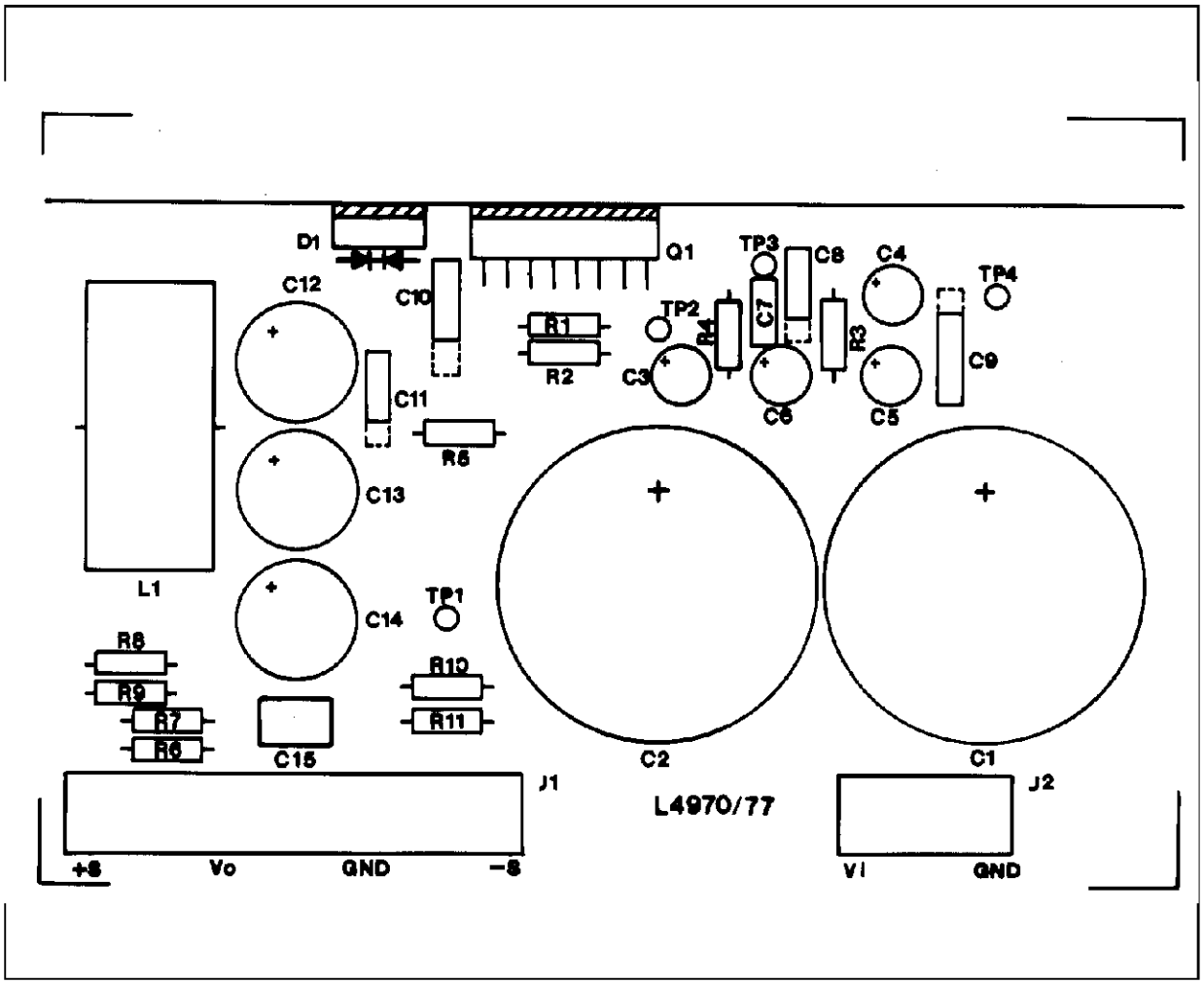


Figure 7: DC Test Circuits

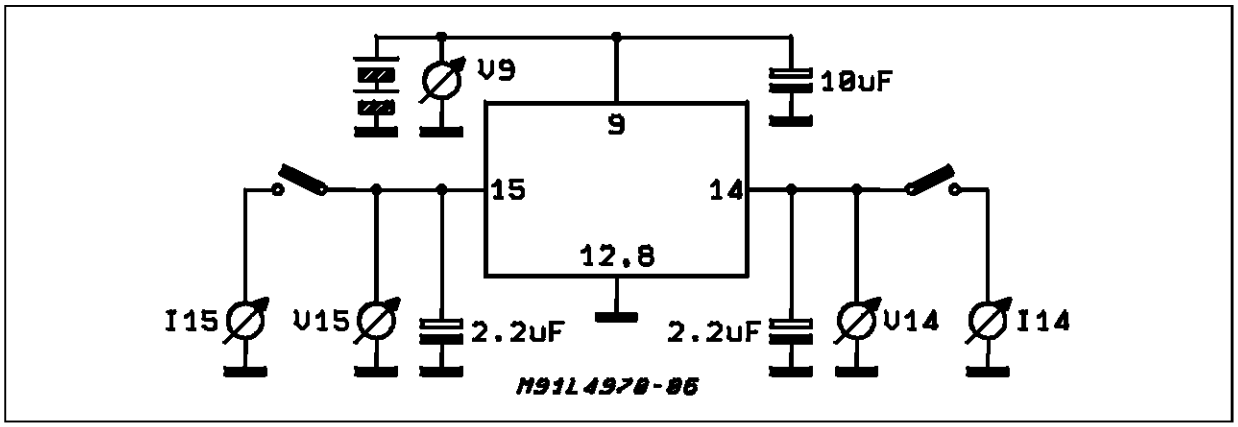


Figure 7A

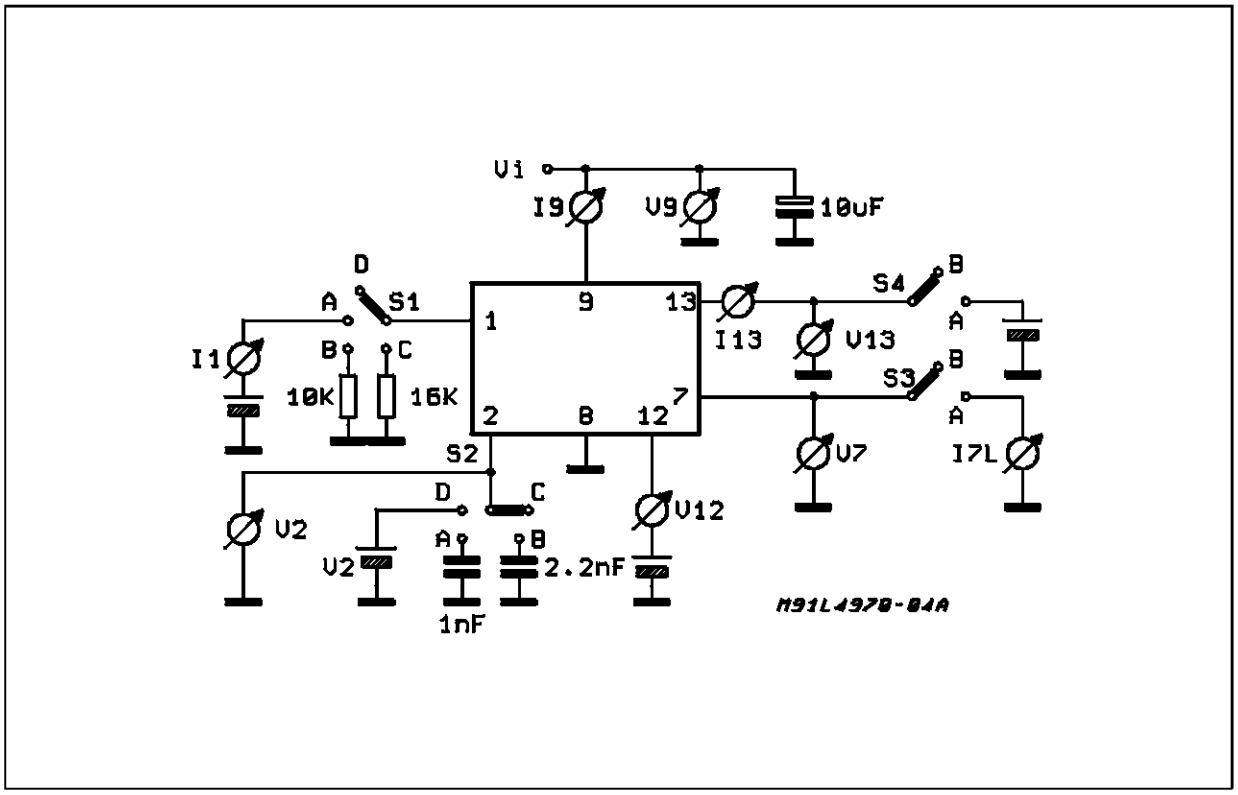


Figure 7B

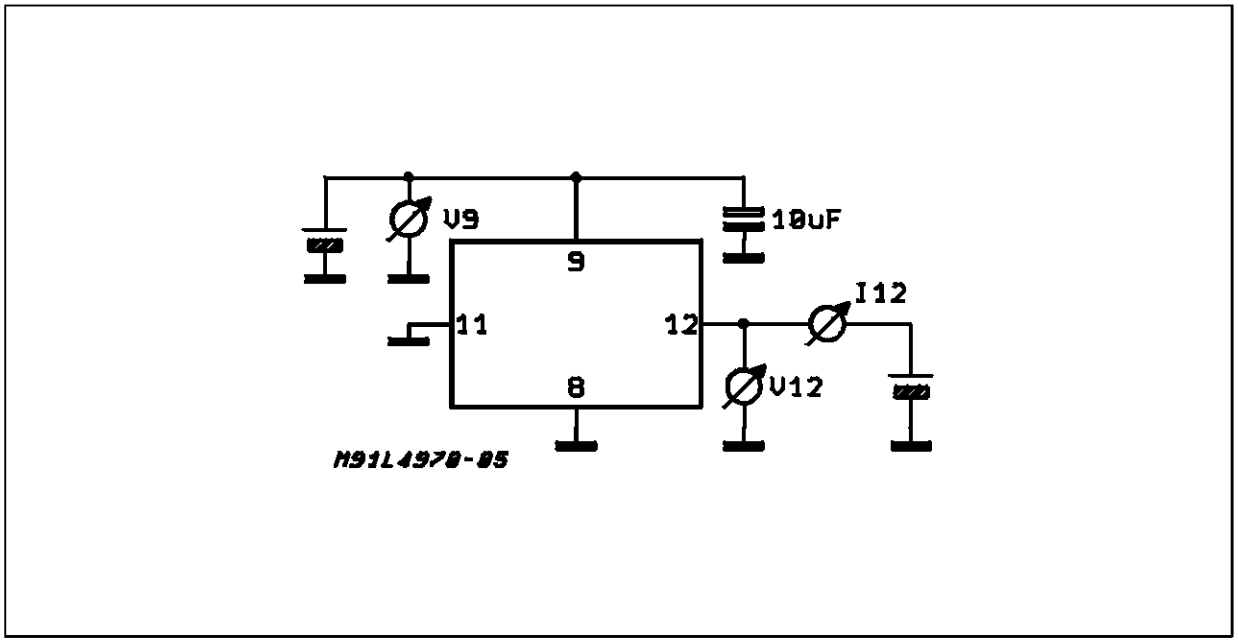


Figure 7D

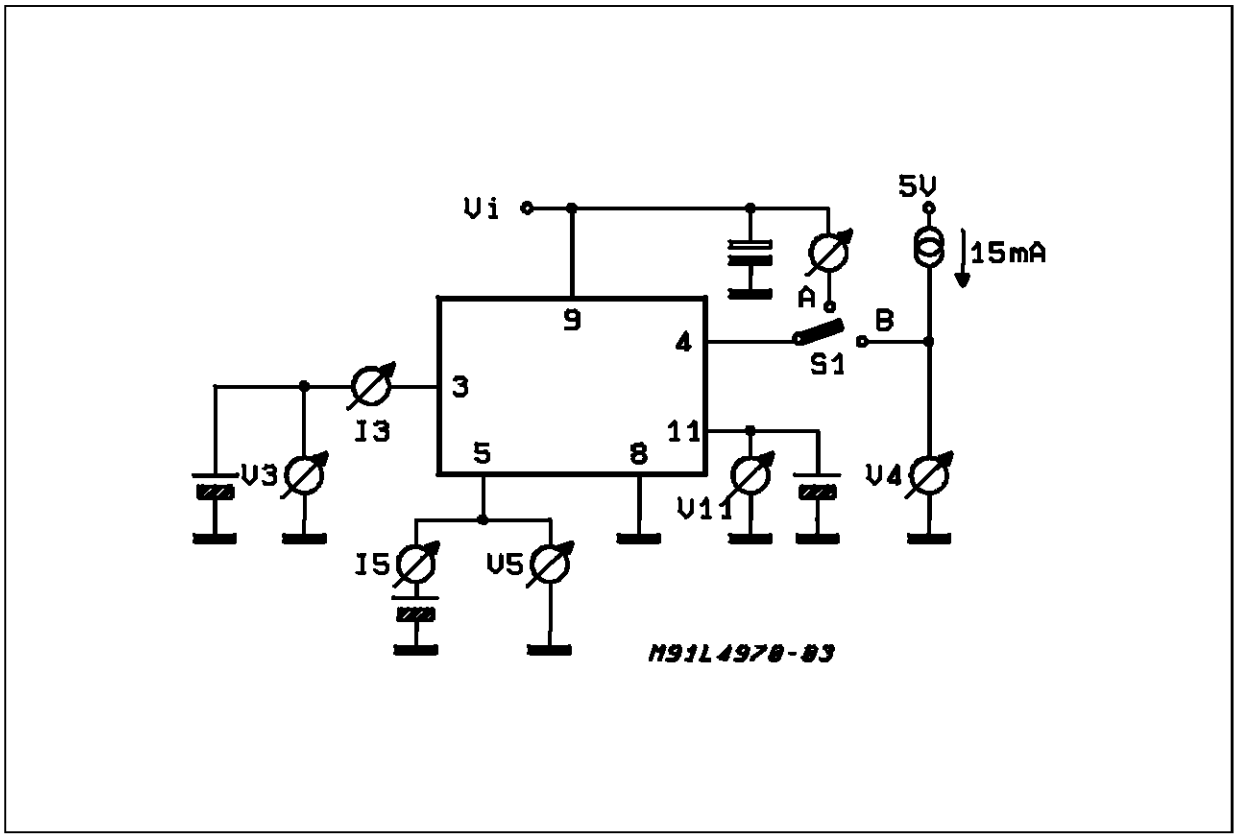


Figure 7C

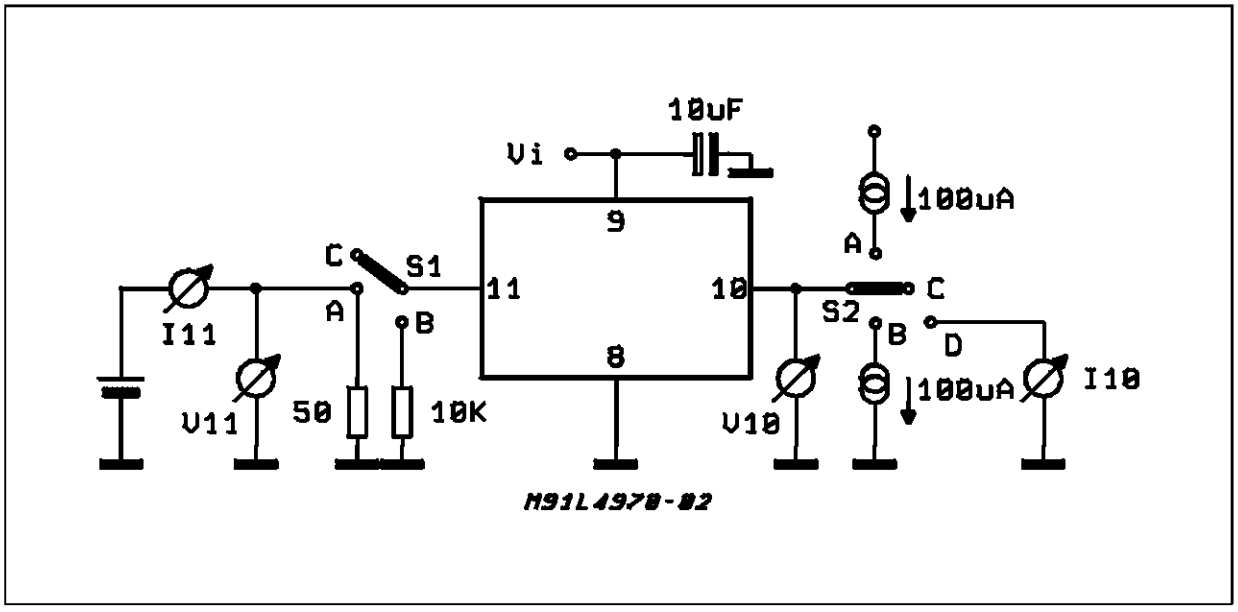


Figure 8: Quiescent Drain Current vs. Supply Voltage (0% duty cycle - see fig. 7A).

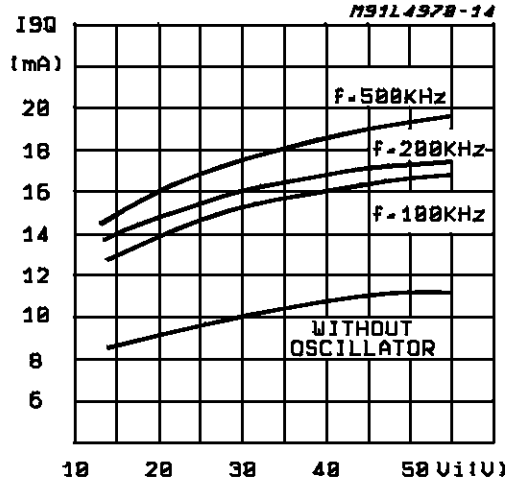


Figure 9: Quiescent Drain Current vs. Junction Temperature (0% duty cycle).

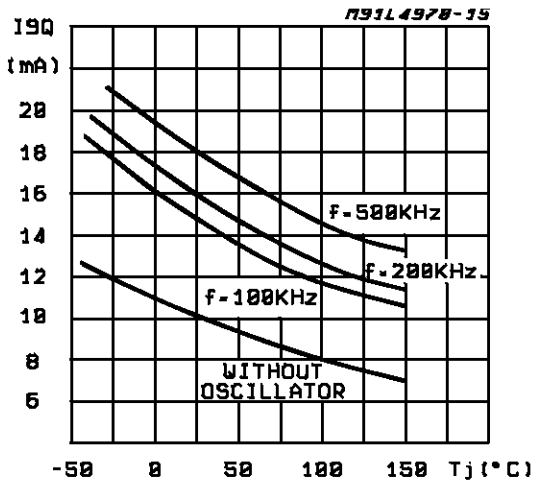


Figure 10: Quiescent Drain Current vs. Duty Cycle

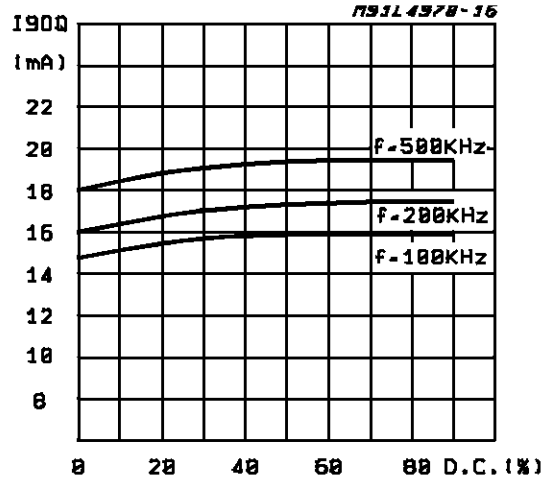


Figure 11: Reference Voltage (pin14) vs. V_i (see fig. 7)

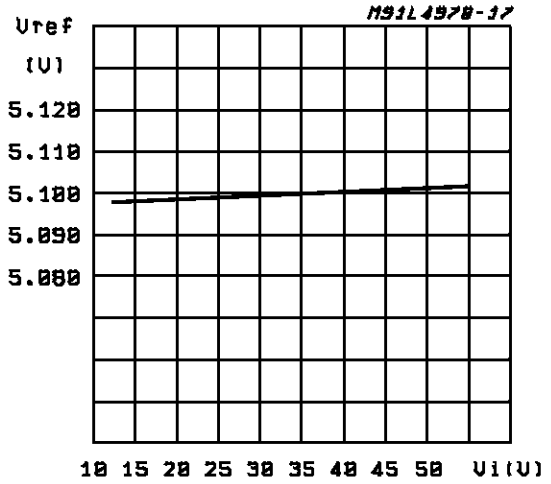


Figure 12: Reference Voltage (pin 14) vs. Junction Temperature (see fig. 7)

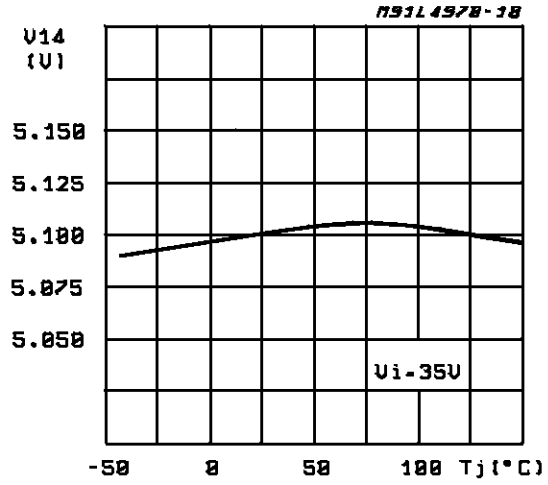


Figure 13: Reference Voltage (pin15) vs. V_i (see fig. 7)

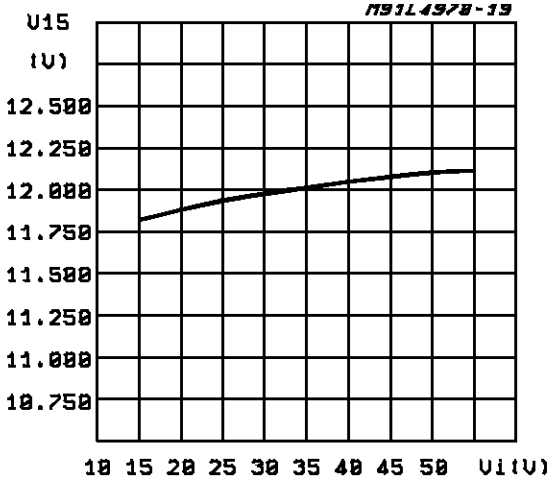


Figure 14: Reference Voltage (pin 15) vs. Junction Temperature (see fig. 7)

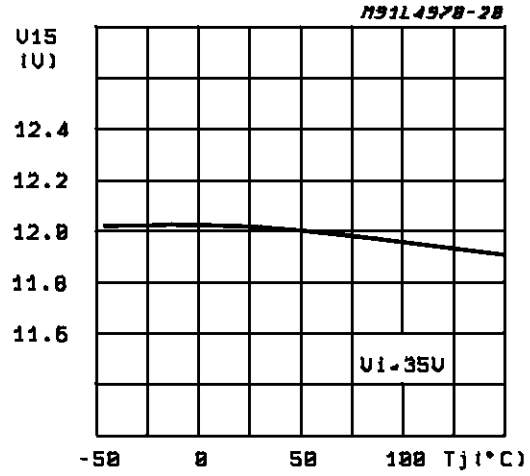


Figure 15: Reference Voltage 5.1V (pin 14) Supply Voltage Ripple Rejection vs. Frequency

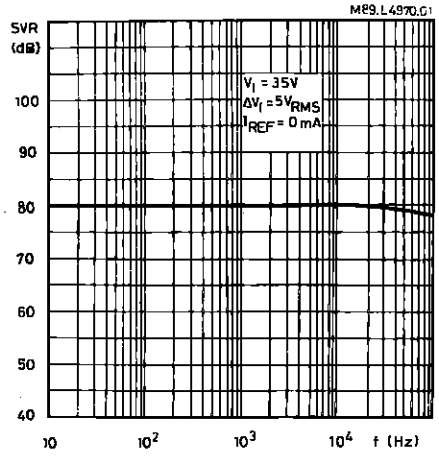


Figure 16: Switching Frequency vs. Input Voltage (see fig. 5)

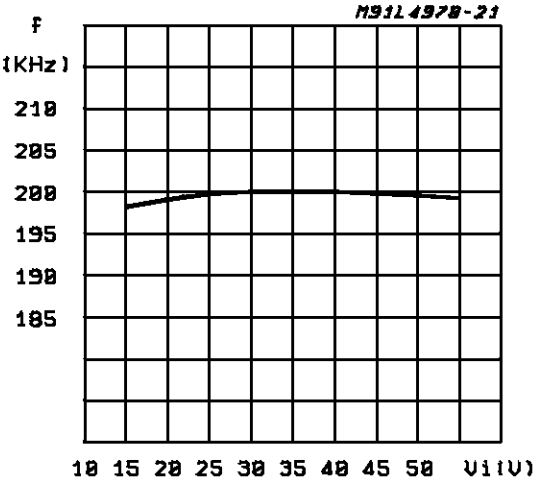


Figure 17: Switching Frequency vs. Junction Temperature (see fig 5)

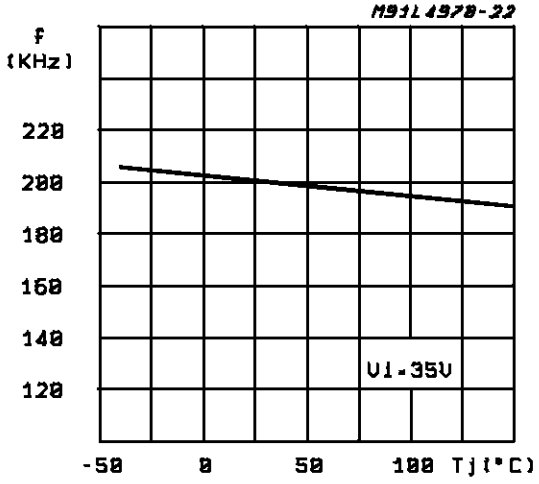


Figure 18: Switching Frequency vs. R4 (see fig. 5)

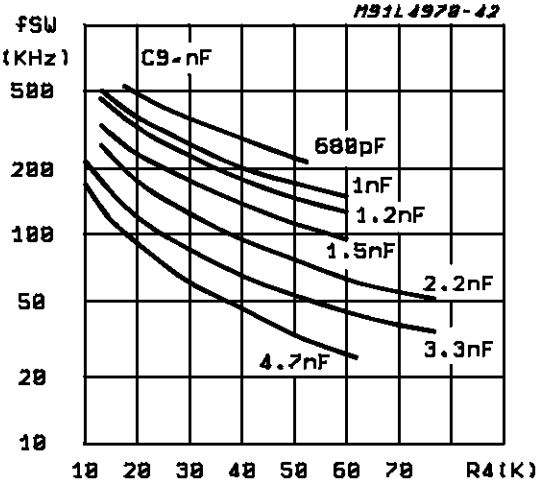


Figure 19: Max. Duty Cycle vs. Frequency

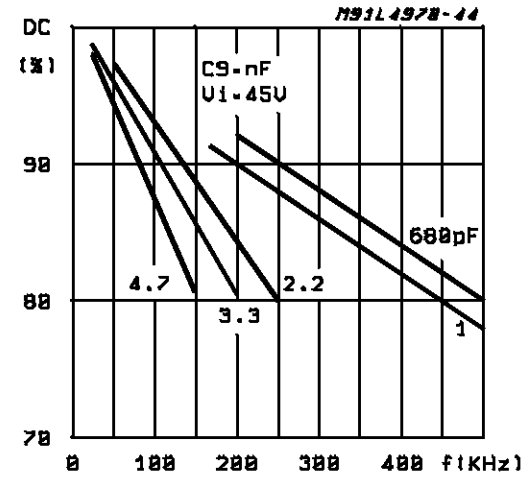


Figure 20: Supply Voltage Ripple Rejection vs. Frequency (see fig. 5)

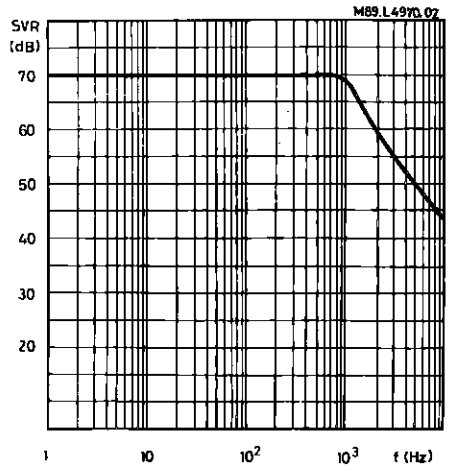


Figure 21: Line Transient Response (see fig. 5)

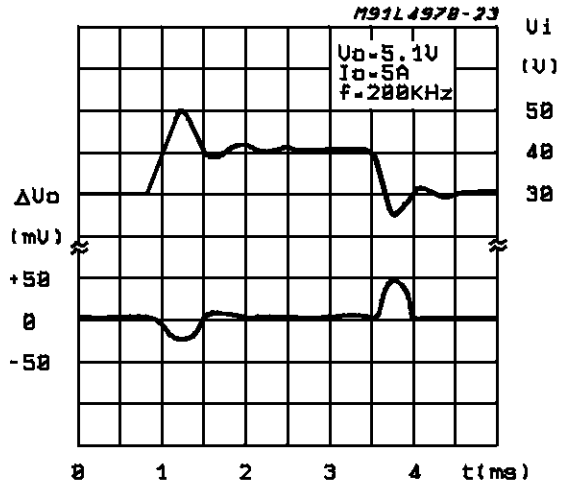


Figure 22: Load Transient Response (see fig. 5)

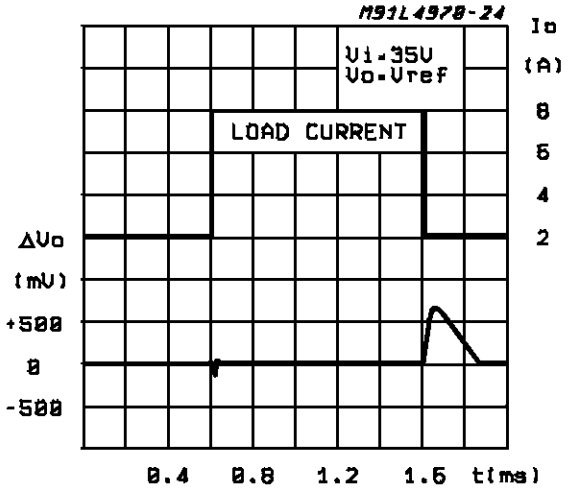


Figure 23: Dropout Voltage Between Pin 9 and Pin 7 vs. Current at Pin 7

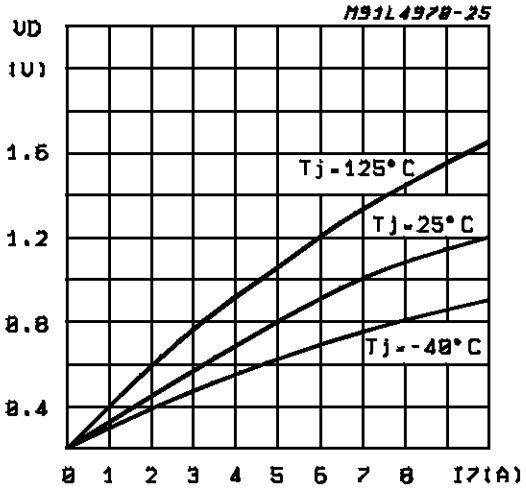


Figure 24: Dropout Voltage Between Pin 9 and Pin 7 vs. Junction Temperature

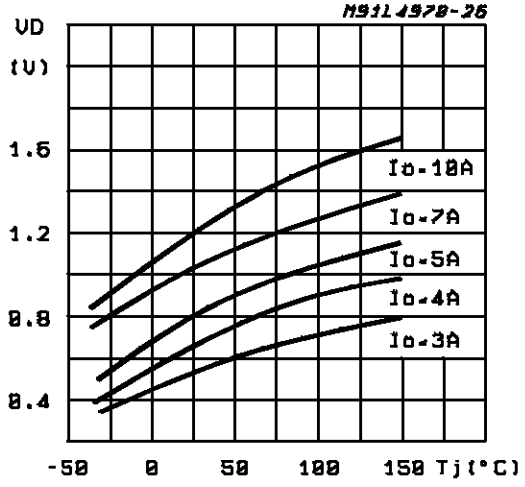


Figure 25: Power Dissipation (device only) vs. Input Voltage

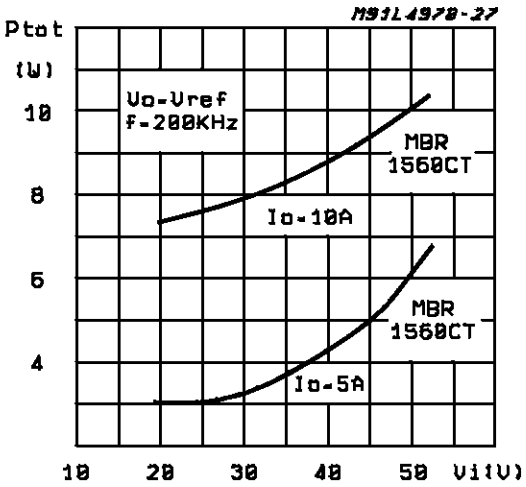


Figure 26: Power Dissipation (device only) vs. Output Voltage

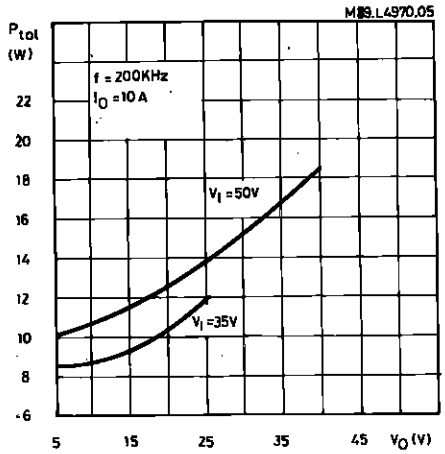


Figure 27: Heatsink Used to Derive the Device's Power Dissipation

$$R_{th}\text{ - Heatsink} = \frac{T_{case} - T_{amb}}{P_d}$$

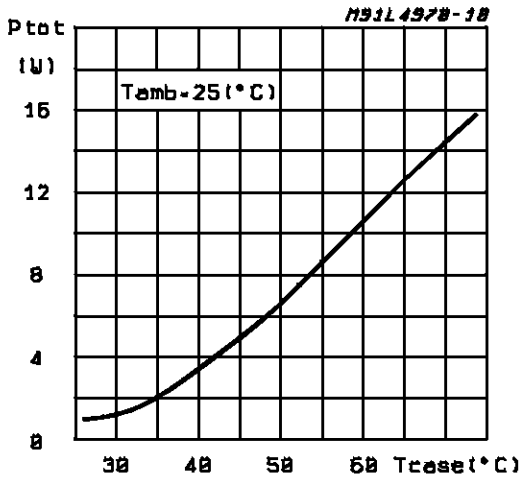


Figure 28: Efficiency vs. Output Current

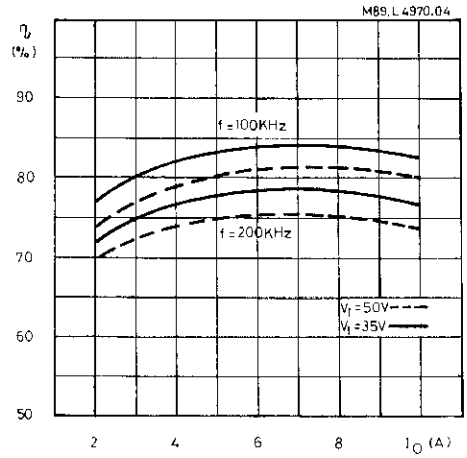


Figure 29: Efficiency vs. Output Voltage

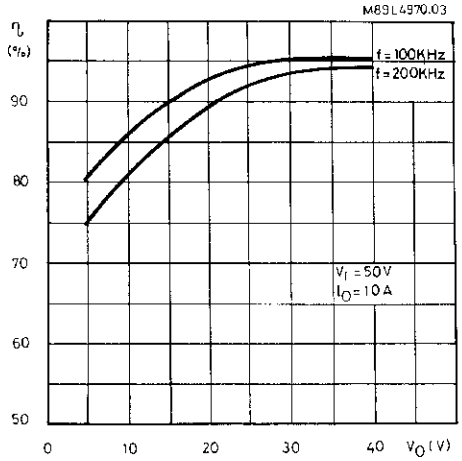


Figure 30: Efficiency vs. Output Voltage

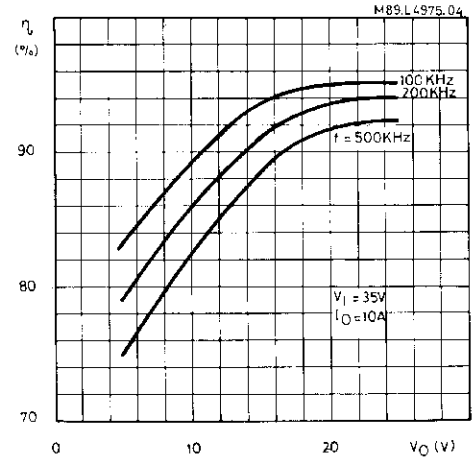


Figure 31: Open Loop Frequency and Phase Response of Error Amplifier (see fig.7C)

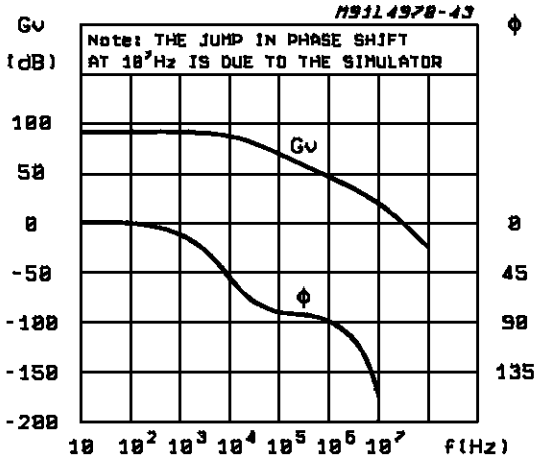


Figure 32: Power Dissipation Derating Curve

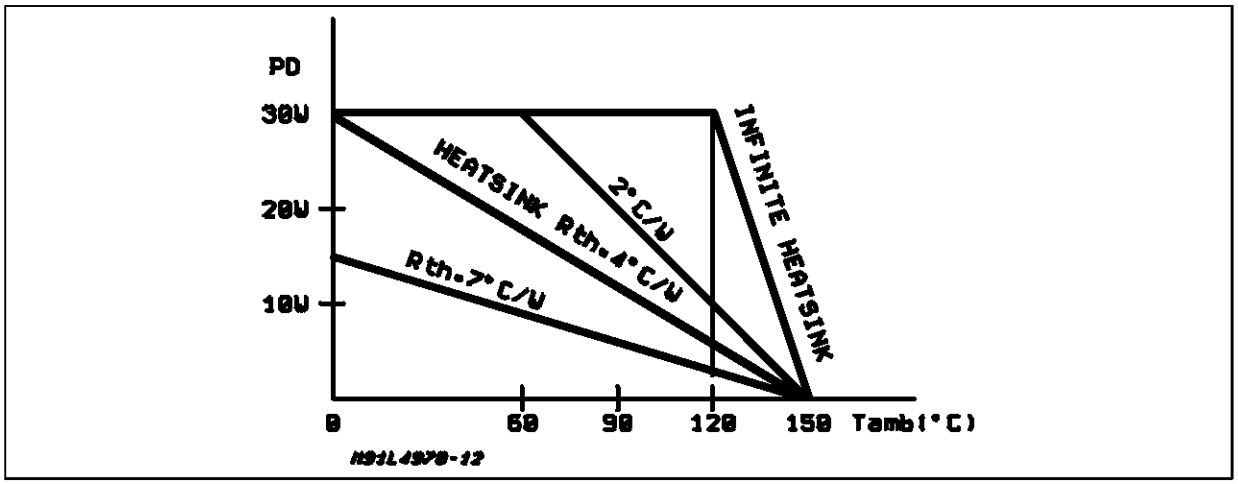


Figure 33: A5.1V/12V Multiple Supply. Note the Synchronization between the L4970A and the L4974A

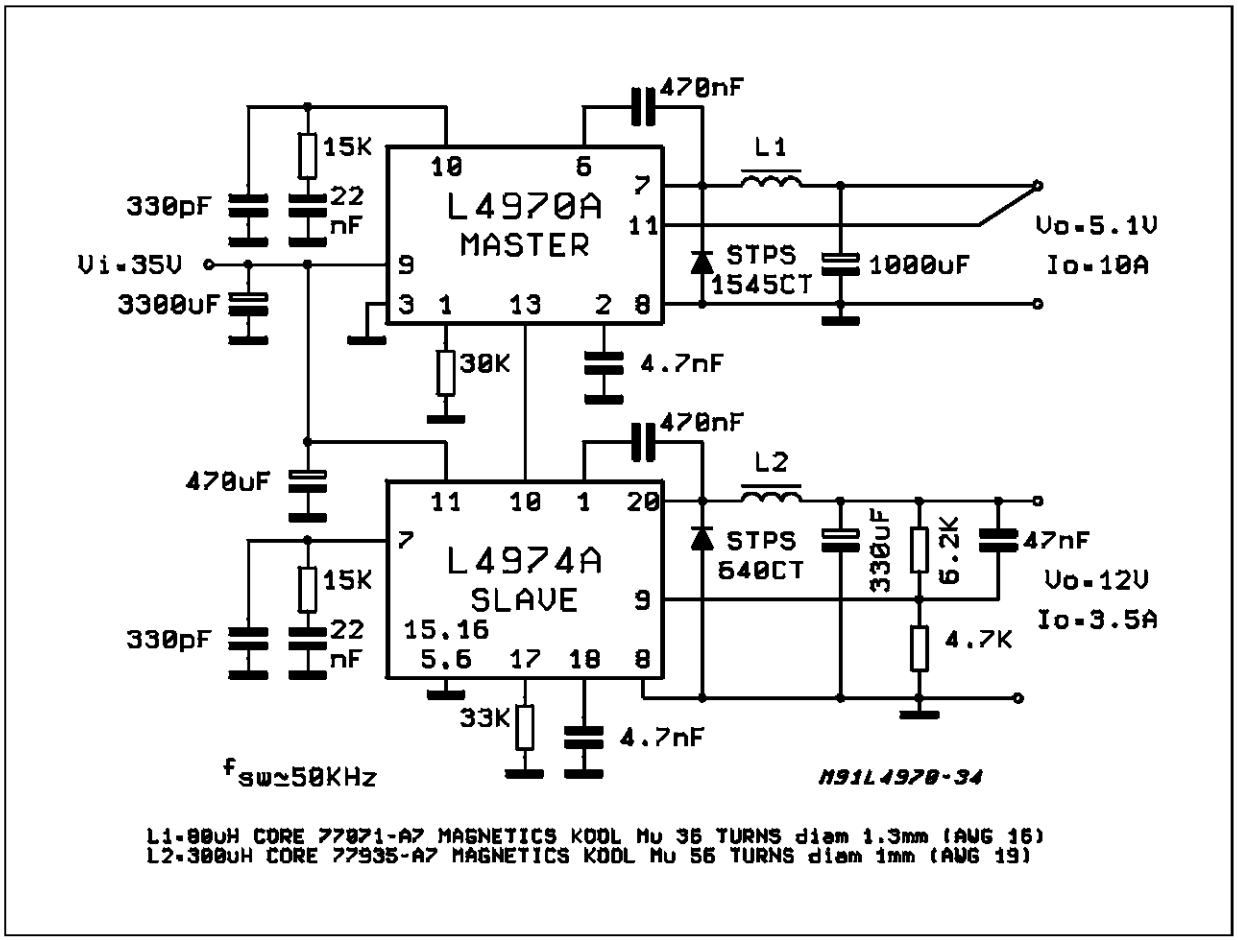


Figure 34: 5.1V / 10A Low Cost Application

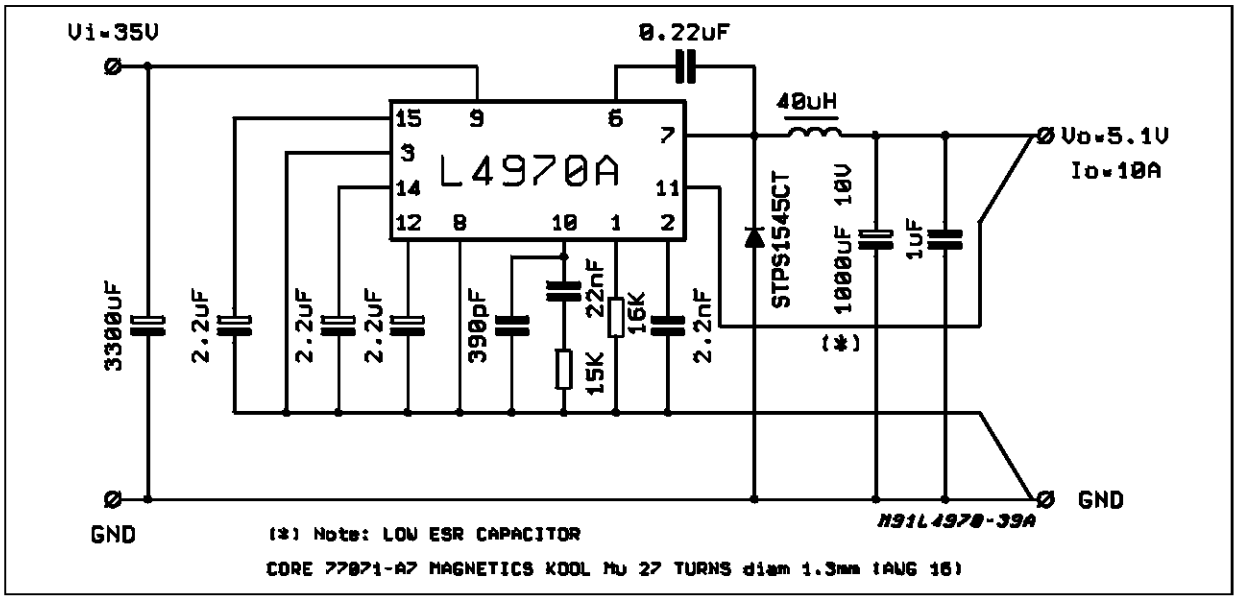


Figure 35: 10A Switching Regulator, Adjustable from 0V to 25V.

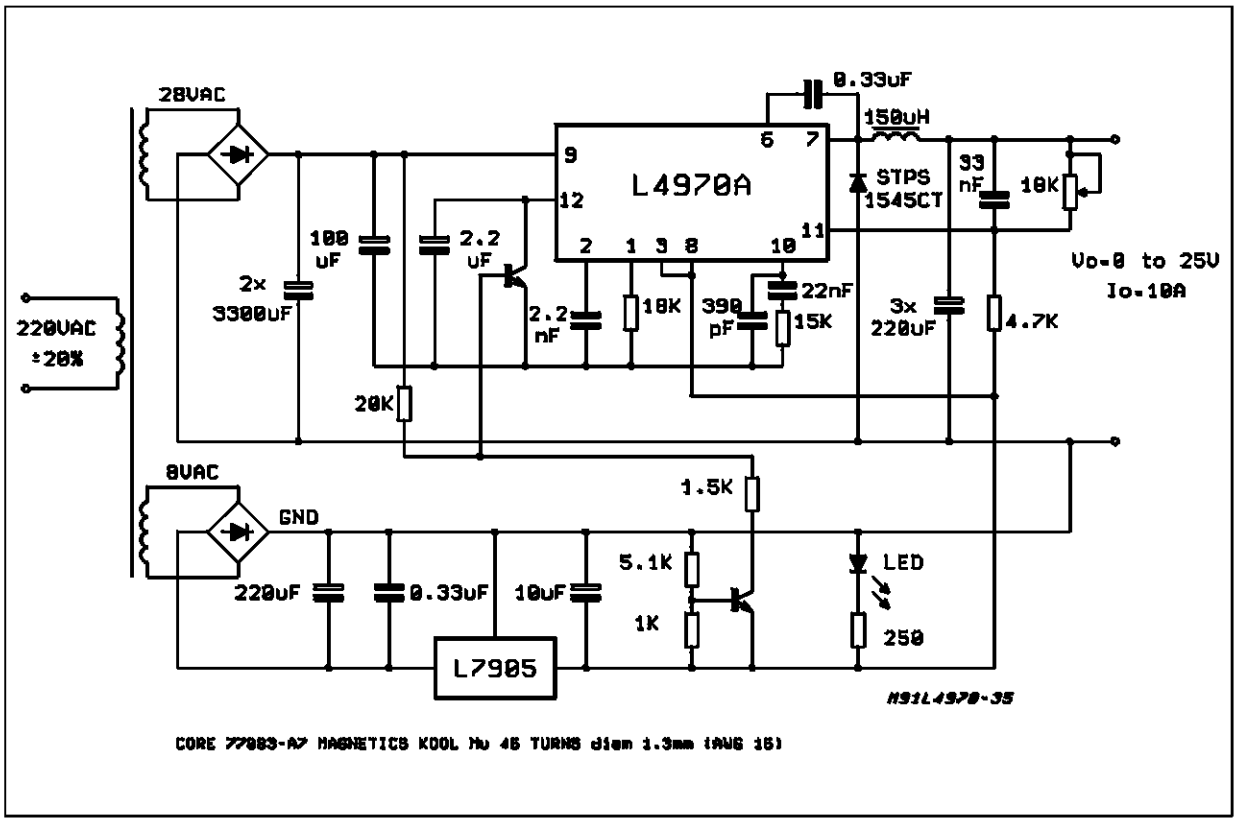
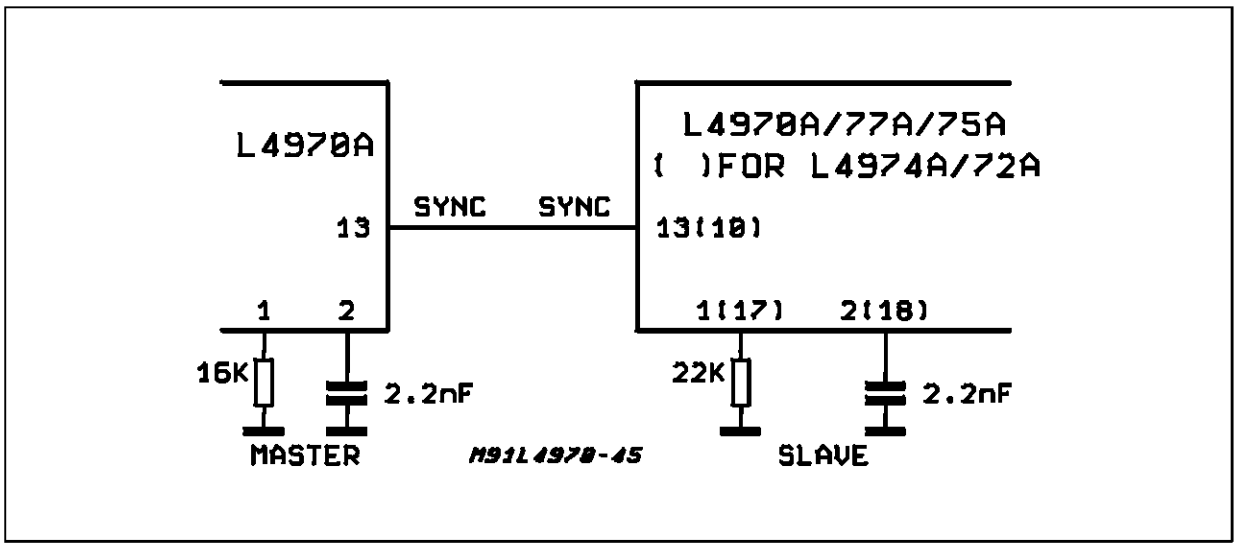
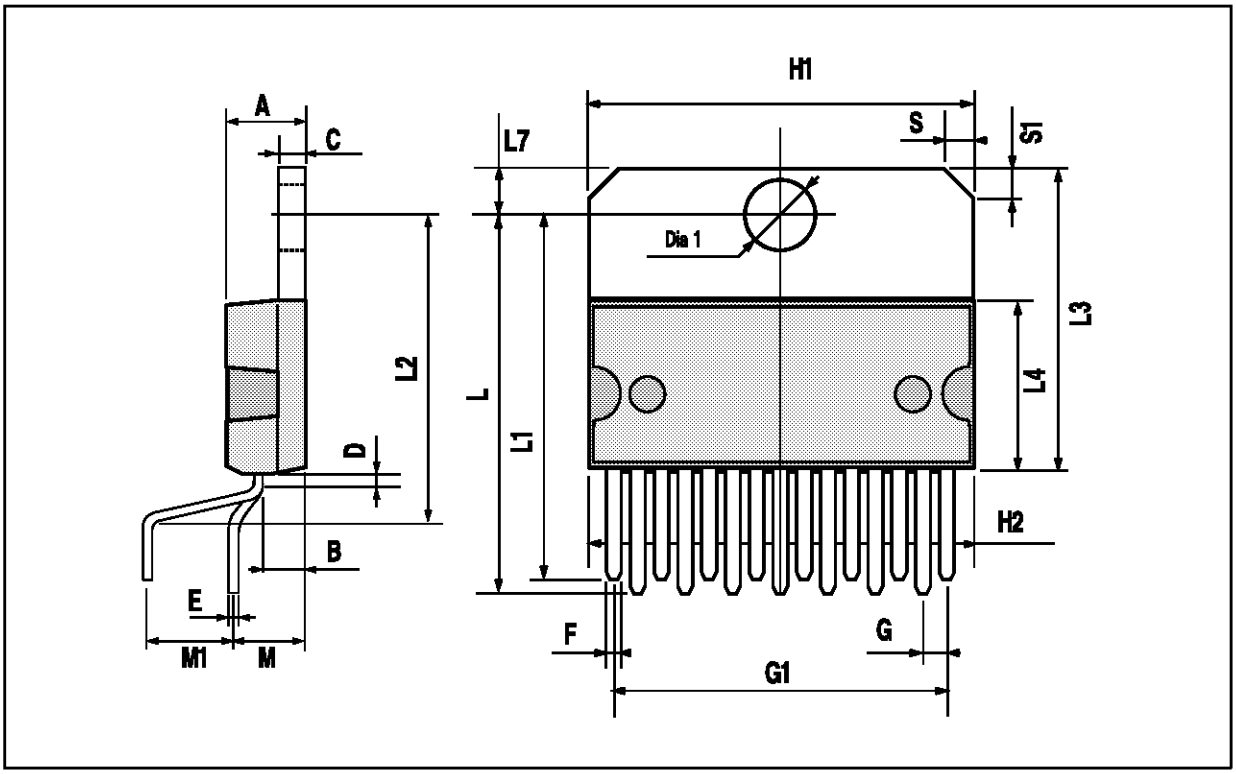


Figure 36: L4970A's Sync. Example



MULTIWATT15 PACKAGE MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			5			0.197
B			2.65			0.104
C			1.6			0.063
D		1			0.039	
E	0.49		0.55	0.019		0.022
F	0.66		0.75	0.026		0.030
G	1.14	1.27	1.4	0.045	0.050	0.055
G1	17.57	17.78	17.91	0.692	0.700	0.705
H1	19.6			0.772		
H2			20.2			0.795
L	22.1		22.6	0.870		0.890
L1	22		22.5	0.866		0.886
L2	17.65		18.1	0.695		0.713
L3	17.25	17.5	17.75	0.679	0.689	0.699
L4	10.3	10.7	10.9	0.406	0.421	0.429
L7	2.65		2.9	0.104		0.114
M	4.2	4.3	4.6	0.165	0.169	0.181
M1	4.5	5.08	5.3	0.177	0.200	0.209
S	1.9		2.6	0.075		0.102
S1	1.9		2.6	0.075		0.102
Dia1	3.65		3.85	0.144		0.152



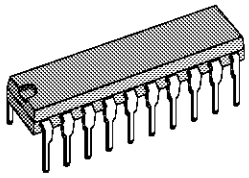
SGS-THOMSON MICROELECTRONICS

L4972A
L4972AD

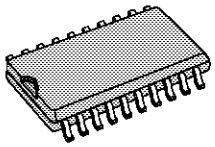
2A SWITCHING REGULATOR

- 2A OUTPUT CURRENT
- 5.1V TO 40V OUTPUT VOLTAGE RANGE
- 0 TO 90% DUTY CYCLE RANGE
- INTERNAL FEED-FORWARD LINE REG.
- INTERNAL CURRENT LIMITING
- PRECISE 5.1V ± 2% ON CHIP REFERENCE
- RESET AND POWER FAIL FUNCTIONS
- INPUT/OUTPUT SYNC PIN
- UNDER VOLTAGE LOCK OUT WITH HYSTERETIC TURN-ON
- PWM LATCH FOR SINGLE PULSE PER PERIOD
- VERY HIGH EFFICIENCY
- SWITCHING FREQUENCY UP TO 200KHz
- THERMAL SHUTDOWN
- CONTINUOUS MODE OPERATION

MULTIPOWER BCD TECHNOLOGY



POWERDIP
(16 + 2 + 2)



SO20

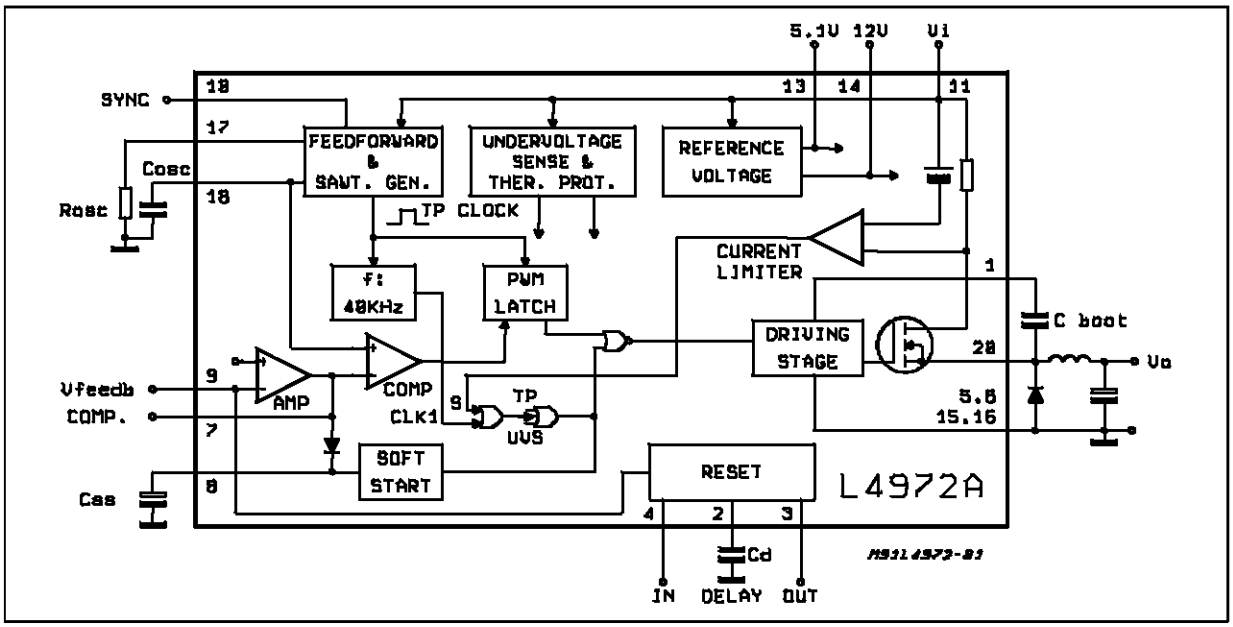
ORDERING NUMBERS : L4972A (Powerdip)
L4972AD (SO20)

DESCRIPTION

The L4972A is a stepdown monolithic power switching regulator delivering 2A at a voltage variable from 5.1 to 40V.

Realized with BCD mixed technology, the device uses a DMOS output transistor to obtain very high efficiency and very fast switching times. Features of the L4972A include reset and power fail for microprocessors, feed forward line regulation, soft start, limiting current and thermal protection. The device is mounted in a Powerdip 16 + 2 + 2 and SO20 large plastic packages and requires few external components. Efficient operation at switching frequencies up to 200KHz allows reduction in the size and cost of external filter component.

BLOCK DIAGRAM

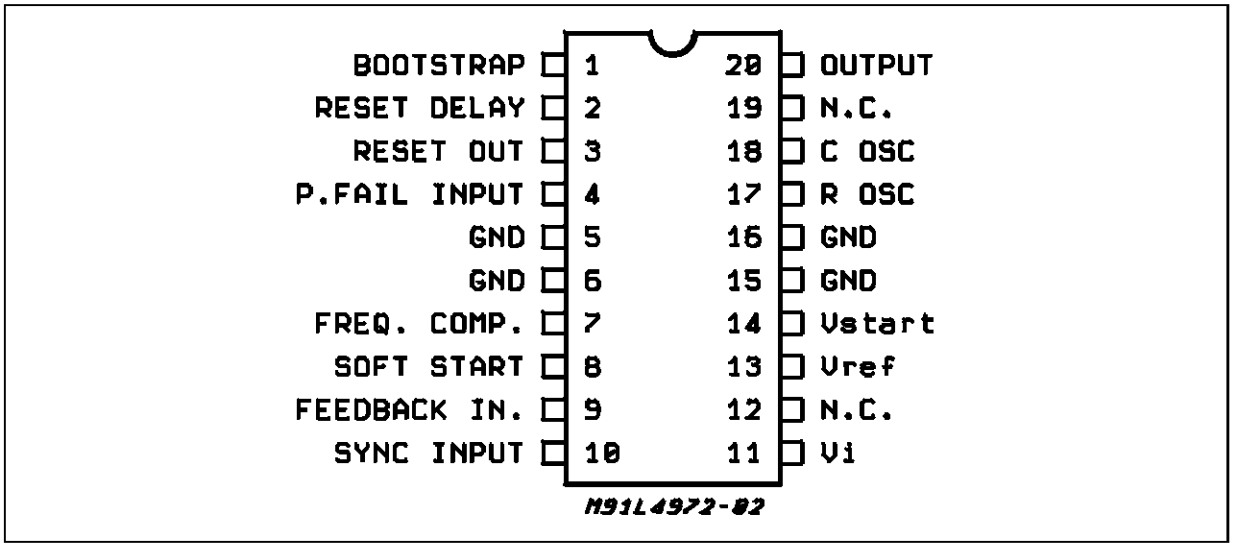


ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{11}	Input Voltage	55	V
V_{11}	Input Operating Voltage	50	V
V_{20}	Output DC Voltage Output Peak Voltage at t = 0.1µs f = 200khz	-1 -5	V V
I_{20}	Maximum Output Current	Internally Limited	
V_I	Boostrap Voltage Boostrap Operating Voltage	65 V_{11} + 15	V V
V_4, V_8	Input Voltage at Pins 4, 12	12	V
V_3	Reset Output Voltage	50	V
I_3	Reset Output Sink Current	50	mA
V_2, V_7, V_9, V_{10}	Input Voltage at Pin 2, 7, 9, 10	7	V
I_2	Reset Delay Sink Current	30	mA
I_7	Error Amplifier Output Sink Current	1	A
I_8	Soft Start Sink Current	30	mA
P_{tot}	Total Power Dissipation at $T_{PINS} \leq 90°C$ at T_{amb} = 70°C (No copper area on PCB)	5 / 3.75(*) 1.3/1 (*)	W W
T_J, T_{stg}	Junction and Storage Temperature	-40 to 150	°C

(*) SO-20

PIN CONNECTION (top view)



THERMAL DATA

Symbol	Parameter		Powerdip	SO-20
$R_{th\ j\text{-}pins}$	Thermal Resistance Junction-Pins	max	12°C/W	16°C/W
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient	max	60°C/W	80°C/W

PIN FUNCTIONS

N°	Name	Function
1	BOOTSTRAP	A C_{boot} capacitor connected between this terminal and the output allows to drive properly the internal D-MOS transistor.
2	RESET DELAY	A C_d capacitor connected between this terminal and ground determines the reset signal delay time.
3	RESET OUT	Open Collector Reset/power Fail Signal Output. This output is high when the supply and the output voltages are safe.
4	RESET INPUT	Input of Power Fail Circuit. The threshold is 5.1V. It may be connected via a divider to the input for power fail function. It must be connected to the pin 14 an external 30KΩ resistor when power fail signal not required.
5, 6 15, 16	GROUND	Common Ground Terminal
7	FREQUENCY COMPENSATION	A series RC network connected between this terminal and ground determines the regulation loop gain characteristics.
8	SOFT START	Soft Start Time Constant. A capacitor is connected between thi sterminal and ground to define the soft start time constant.
9	FEEDBACK INPUT	The Feedback Terminal of the Regulation Loop. The output is connected directly to this terminal for 5.1V operation; It is connected via a divider for higher voltages.
10	SYNC INPUT	Multiple L4972A's are synchronized by connecting pin 10 inputs together or via an external syncr. pulse.
11	SUPPLY VOLTAGE	Unregulated Input Voltage.
12, 19	N.C.	Not Connected.
13	V_{ref}	5.1V V_{ref} Device Reference Voltage.
14	V_{start}	Internal Start-up Circuit to Drive the Power Stage.
17	OSCILLATOR	R_{osc}. External resistor connected to ground determines the constant charging current of C_{osc}.
18	OSCILLATOR	C_{osc}. External capacitor connected to ground determines (with R_{osc}) the switching frequency.
20	OUTPUT	Regulator Output.

CIRCUIT OPERATION

The L4972A is a 2A monolithic stepdown switching regulator working in continuous mode realized in the new BCD Technology. This technology allows the integration of isolated vertical DMOS power transistors plus mixed CMOS/Bipolar transistors.

The device can deliver 2A at an output voltage adjustable from 5.1V to 40V and contains diagnostic and control functions that make it particularly suitable for microprocessor based systems.

BLOCK DIAGRAM

The block diagram shows the DMOS power transistors and the PWM control loop. Integrated functions include a reference voltage trimmed to 5.1V ± 2%, soft start, undervoltage lockout, oscillator with feedforward control, pulse by pulse current limit, thermal shutdown and finally the reset and power fail circuit. The reset and power fail circuit provides an output signal for a microprocessor indicating the status of the system.

Device turn on is around 11V with a typical 1V hysterysis, this threshold porvides a correct voltage for the driving stage of the DMOS gate and the hysterysis prevents instabilities.

An external bootstrap capacitor charge to 12V by an internal voltage reference is needed to provide correct gate drive to the power DMOS. The driving circuit is able to source and sink peak currents of around 0.5A to the gate of the DMOS transistor. A typical switching time of the current in the DMOS transistor is 50ns. Due to the fast commutation switching frequencies up to 200kHz are possible.

The PWM control loop consists of a sawtooth oscillator, error amplifier, comparator, latch and the output stage. An error signal is produced by comparing the output voltage with the precise 5.1V ± 2% on chip reference. This error signal is then compared with the sawtooth oscillator in order to generate frixed frequency pulse width modulated drive for the output stage. A PWM latch is included to eliminate multiple pulsing within a period even in noisy environments.

The gain and stability of the loop can be adjusted by an external RC network connected to the output of the error amplifier. A voltage feedforward control has been added to the oscillator, this maintains superior line regulation over a wide input voltage range. Closing the loop directly gives an output vol-tage of 5.1V, higher voltages are obtained by inserting a voltage divider.

At turn on, output overcurrents are prevented by the soft start function (fig. 2). The error amplifier is initially clamped by an external capacitor, Css, and allowed to rise linearly under the charge of an internal constant current source.

Output overload protection is provided by a current limit circuit. The load current is sensed by a internal metal resistor connected to a comparator. When the load current exceeds a preset threshold, the output of the comparator sets a flip flop which turns off the power DMOS. The next clock pulse, from an internal 40kHz oscillator, will reset the flip flop and the power DMOS will again conduct. This current protection method, ensures a constant current output when the system is overloaded or short circuited and limits the switching frequency, in this condition, to 40kHz. The Reset and Power fail circuit (fig. 4), generates an output signal when the supply voltage exceeds a threshold programmed by an external voltage divider. The reset signal, is generated with a delay time programmed by a external capacitor on the delay pin. When the supply voltage falls below the threshold or the output voltage goes below 5V, the reset output goes low immediately. The reset output is an open drain.

Fig. 4A shows the case when the supply voltage is higher than the threshold, but the output voltage is not yet 5V.

Fig. 4B shows the case when the output is 5.1V, but the supply voltage is not yet higher than the fixed threshold.

The thermal protection disables circuit operation when the junction temperature reaches about 150°C and has a hysterysis to prevent unstable conditions.

Figure 1 : Feedforward Waveform.

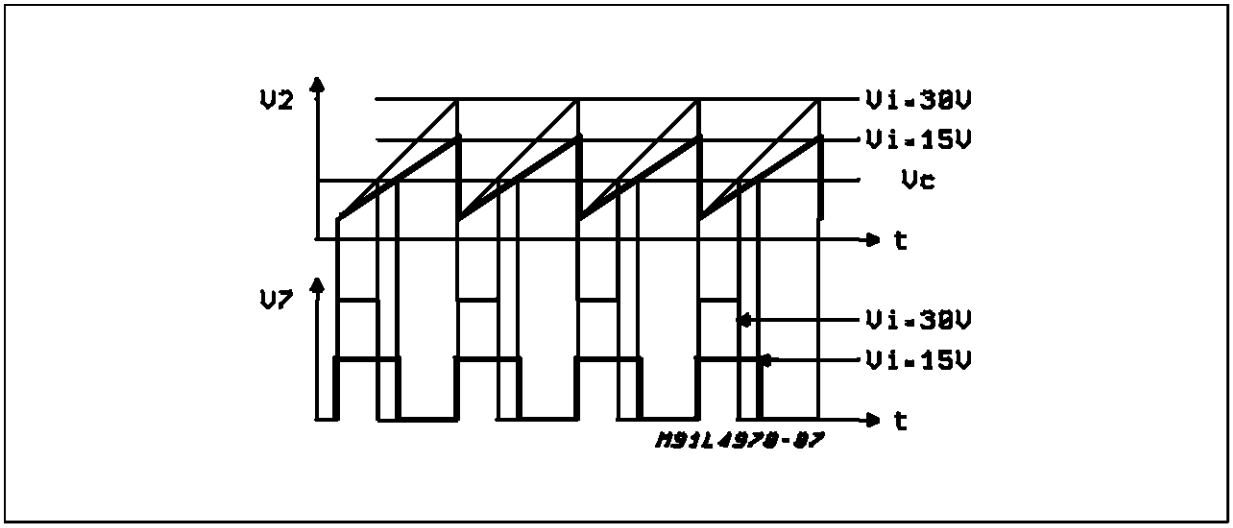


Figure 2 : Soft Start Function.

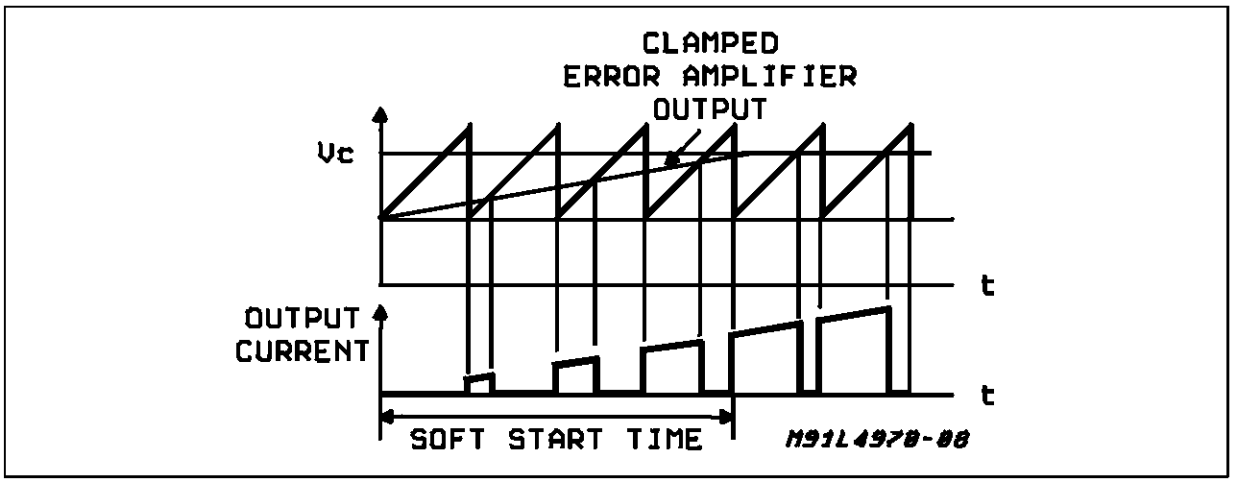


Figure 3 : Limiting Current Function.

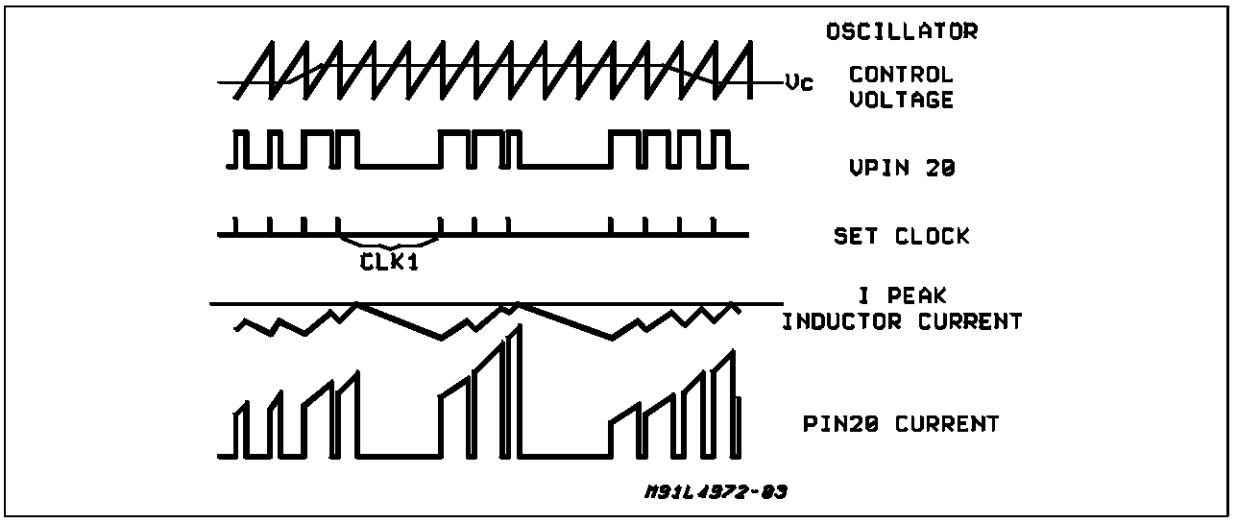
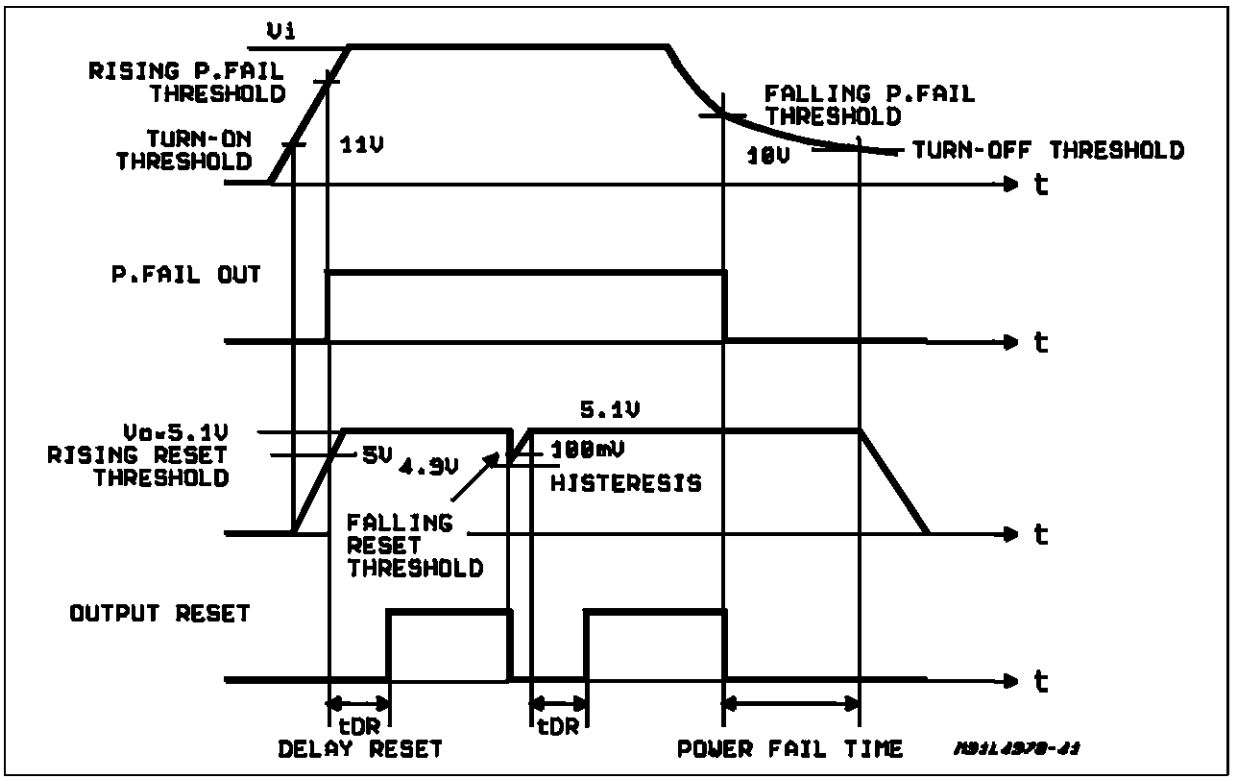
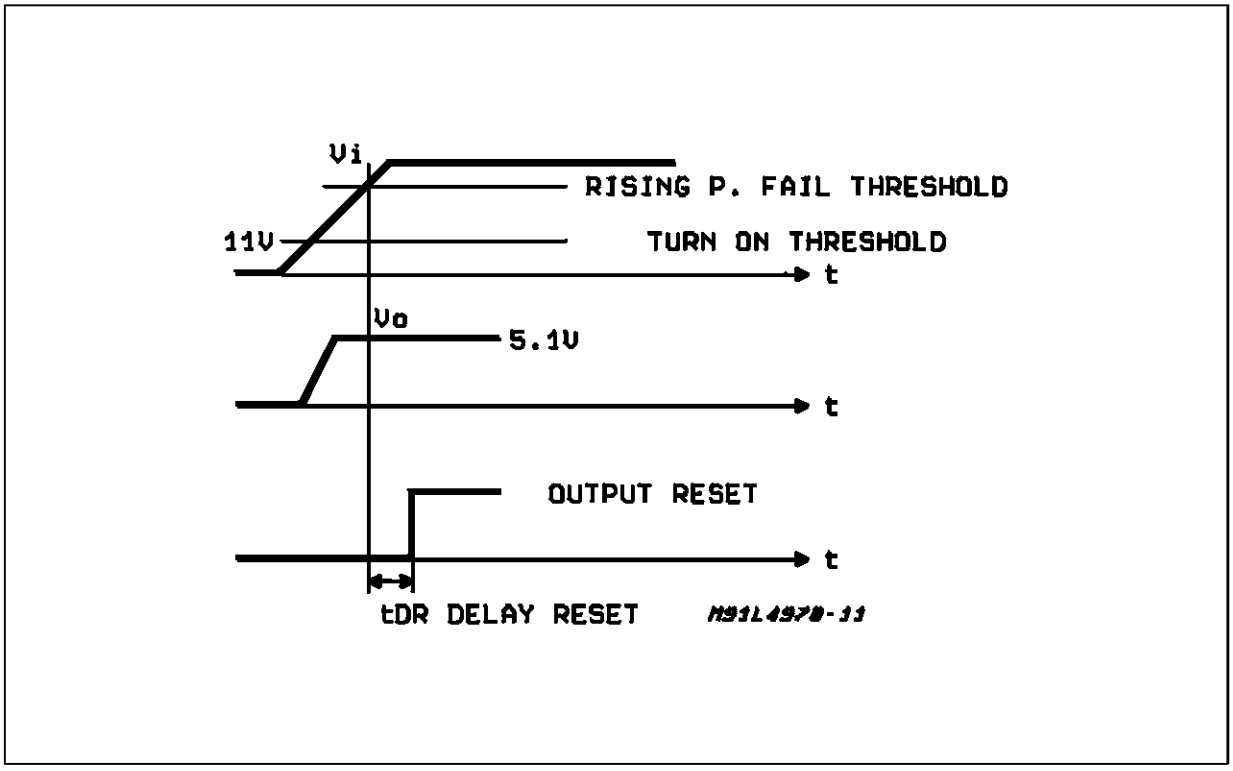


Figure 4 : Reset and Power Fail Functions.

A



B



ELECTRICAL CHARACTERISTICS (refer to the test circuit, T_J = 25°C, V_i = 35V, R_4 = 30KΩ, C_9 = 2.7nF, f_{SW} = 100KHz typ, unless otherwise specified)

DYNAMIC CHARACTERISTICS

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit	Fig.
V_i	Input Volt. Range (pin 11)	V_o = V_{ref} to 40V I_o = 2A (**)	15		50	V	5
V_o	Output Voltage	V_i =15V to 50V I_o = 1A; V_o = V_{ref}	5	5.1	5.2	V	5
ΔV_o	Line Regulation	V_i = 15V to 50V I_o = 0.5A; V_o = V_{ref}		12	30	mV	
ΔV_o	Load Regulation	V_o = V_{ref} I_o = 0.5A to 2A		7	20	mV	
V_d	Dropout Voltage between Pin 11 and 20	I_o = 2A		0.25	0.4	V	
I_{20L}	Max Limiting Current	V_i = 15V to 50V V_o = V_{ref} to 40V	2.5	2.8	3.5	A	
η	Efficiency (*)	I_o = 2A, f = 100KHz V_o = V_{ref} V_o = 12V	75	85 90		% %	
SVR	Supply Voltage Ripple Rejection	V_i = 2VRMS; I_o = 1A f = 100Hz; V_o = V_{ref}	56	60		dB	5
f	Switching Frequency		90	100	110	KHz	5
$\Delta f/\Delta Vi$	Voltage Stability of Switching Frequency	V_i = 15V to 45V		2	6	%	5
$\Delta f/T_j$	Temperature Stability of Switching Frequency	T_j = 0 to 125°C		1		%	5
f_{max}	Maximum Operating Switching Frequency	V_o = V_{ref} R_4 = 15KΩ I_o = 2A C_9 = 2.2nF	200			KHz	5

(*) Only for DIP version (**) Pulse testing with a low duty cycle

V_{ref} SECTION (pin 13)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit	Fig.
V_{13}	Reference Voltage		5	5.1	5.2	V	7
ΔV_{13}	Line Regulation	V_i = 15V to 50V		10	25	mV	7
ΔV_{13}	Load Regulation	I_{13} = 0 to 1mA		20	40	mV	7
$\frac{\Delta V_{13}}{\Delta T}$	Average Temperature Coefficient Reference Voltage	T_j = 0°C to 125°C		0.4		mV/°C	7
$I_{13\ short}$	Short Circuit Current Limit	V_{13} = 0		70		mA	7

V_{START} SECTION (pin 15)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit	Fig.
V_{14}	Reference Voltage		11.4	12	12.6	V	7
ΔV_{14}	Line Regulation	V_i = 15 to 50V		0.6	1.4	V	7
ΔV_{14}	Load Regulation	I_{14} = 0 to 1mA		50	200	mV	7
$I_{14\ short}$	Short Circuit Current Limit	V_{15} = 0V		80		mA	7

ELECTRICAL CHARACTERISTICS (continued)

DC CHARACTERISTICS

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit	Fig.
V_{11on}	Turn-on Threshold		10	11	12	V	7A
$V_{11\ Hyst}$	Turn-off Hysteresys			1		V	7A
I_{11Q}	Quiescent Current	$V_8 = 0$; S1 = D		13	19	mA	7A
I_{11OQ}	Operating Supply Current	$V_8 = 0$; S1 = B; S2 = B		16	23	mA	7A
I_{20L}	Out Leak Current	$V_i = 55V$; S3 = A; $V_8 = 0$			2	mA	7A

SOFT START (pin 8)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit	Fig.
I_8	Soft Start Source Current	$V_8 = 3V$; $V_9 = 0V$	80	115	150	µA	7B
V_8	Output Saturation Voltage	$I_8 = 20mA$; $V_{11} = 10V$ $I_8 = 200µA$; $V_{11} = 10V$			1 0.7	V V	7B 7B

ERROR AMPLIFIER

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit	Fig.
V_{7H}	High Level Out Voltage	$I_7 = 100µA$; S1 = C $V_9 = 4.7V$	6			V	7C
V_{7L}	Low Level Out Voltage	$I_7 = 100µA$; S1 = C $V_9 = 5.3V$;			1.2	V	7C
I_{7H}	Source Output Current	$V_7 = 1V$; $V_7 = 4.7V$	100	150		µA	7C
$-I_{7L}$	Sink Output Current	$V_7 = 6V$; $V_9 = 5.3V$	100	150		µA	7C
I_9	Input Bias Current	S1 = B; $R_S = 10K\Omega$		0.4	3	µA	7C
G_V	DC Open Loop Gain	S1 = A; $R_S = 10\Omega$	60			dB	7C
SVR	Supply Voltage Rejection	$15 < V_i < 50V$	60	80		dB	7C
V_{OS}	Input Offset Voltage	$R_S = 50\Omega$ S1 = A		2	10	mV	7C

RAMP GENERATOR (pin 18)

Symbol	Parameter	Test Condition		Min.	Typ.	Max.	Unit	Fig.
V_{18}	Ramp Valley	S1 = B; S2 = B		1.2	1.5		V	7A
V_{18}	Ramp Peak	S1 = B	$V_i = 15V$		2.5		V	7A
		S2 = B	$V_i = 45V$		5.5		V	7A
I_{18}	Min. Ramp Current	S1 = A; $I_{17} = 100µA$			270	300	µA	7A
I_{18}	Max. Ramp Current	S1 = A; $I_{17} = 1mA$		2.4	2.7		mA	7A

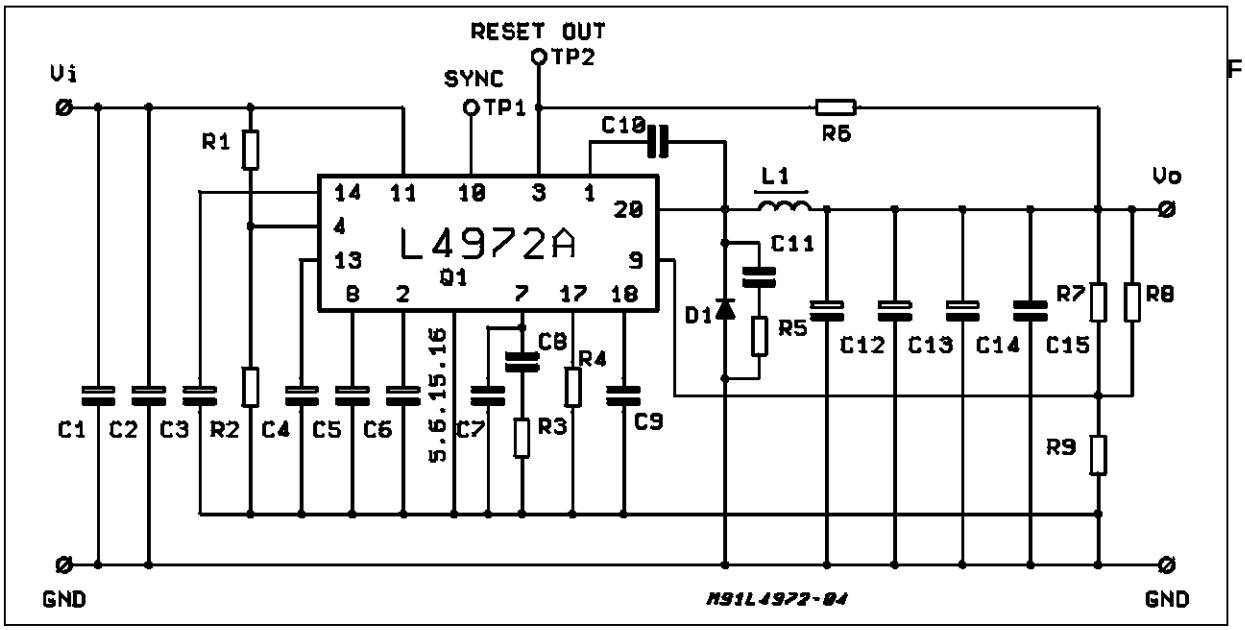
SYNC FUNCTION (pin 10)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit	Fig.
V_{10}	Low Input Voltage	$V_i = 15V$ to 50V; $V_8 = 0$; S1 = B; S2 = B; S4 = B	–0.3		0.9	V	7A
V_{10}	High Input voltage	V8 = 0; S1 = B; S2 = B; S4 = B	2.5		5.5	V	7A
I_{10L}	Sync Input Current with Low Input Voltage	$V_{10} = V_{18} = 0.9V$; S4 = B; S1 = B; S2 = B			0.4	mA	7A
I_{10H}	Input Current with High Input Voltage	$V_{10} = 2.5V$			1.5	mA	7A
V_{10}	Output Amplitude		4	5		V	–
t_W	Output Pulse Width	$V_{thr} = 2.5V$	0.3	0.5	0.8	µs	–

ELECTRICAL CHARACTERISTICS (continued)

RESET AND POWER FAIL FUNCTIONS

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit	Fig.
V_{9R}	Rising Thereshold Voltage (pin 9)	V_i = 15 to 50V V_4 = 5.3V	V_{ref} -130	V_{ref} -100	V_{ref} -80	V mV	7D
V_{9F}	Falling Thereshold Voltage (pin 9)	Vi = 15 to 50V V_4 = 5.3V	4.77	Vref -200	V_{ref} -160	V mV	7D
V_{2H}	Delay High Threshold Volt.	Vi = 15 to 50V V_4 = 5.3V $V_9 = V_{13}$	4.95	5.1	5.25	V	7D
V_{2L}	Delay Low Threshold Volt.	Vi = 15 to 50V V_4 = 4.7V $V_9 = V_{13}$	1	1.1	1.2	V	7D
I_{2SO}	Delay Source Current	V_4 = 5.3V; V_2 = 3V	30	60	80	µA	7D
I_{2SI}	Delay Source Sink Current	V_4 = 4.7V; V_2 = 3V	10			mA	7D
V_{3S}	Output Saturation Voltage	I_3 = 15mA; S1 = B V_4 = 4.7V			0.4	V	7D
I_3	Output Leak Current	V3 = 50V; S1 = A			100	µA	7D
V_{4R}	Rising Threshold Voltage	V9 = V_{13}	4.95	5.1	5.25	V	7D
V_{4H}	Hysteresis		0.4	0.5	0.6	V	7D
I_4	Input Bias Current			1	3	µA	7D



TYPICAL PERFORMANCES (using evaluation board) :

n = 83% (V_i = 35V ; V_o = VREF ; I_o = 2A ; f_{sw} = 100KHz)

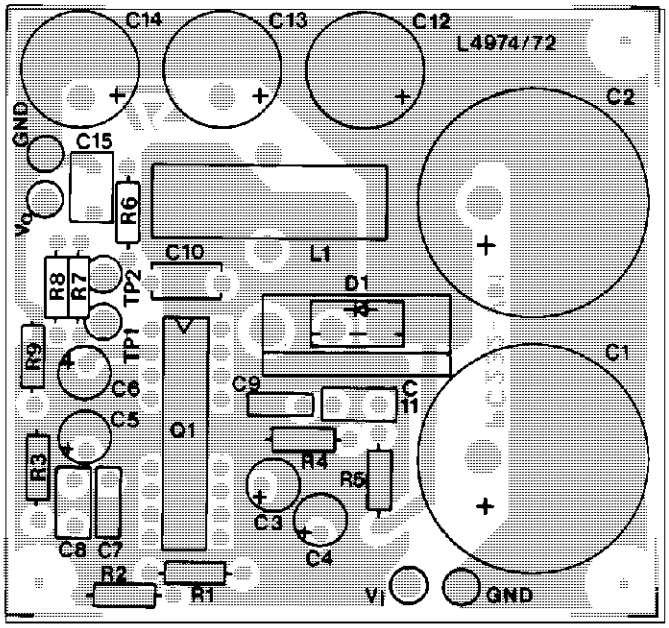
$V_{o\ RIPPLE}$ = 30mV (at 1A)

Line regulation = 12mV (V_i = 15 to 50V)

Load regulation = 7mV (I_o = 0.5 to 2A)

for component values Refer to the fig. 5 (Part list).

Figure 6a : Component Layout of fig.5 (1 : 1 scale). Evaluation Board Available (only for DIP version)



PART LIST

R_1 = 30KΩ
R_2 = 10KΩ
R_3 = 15KΩ
R_4 = 30KΩ
R_5 = 22Ω
R_6 = 4.7KΩ
R_7 = see table A
R_8 = OPTION
R_9 = 4.7KΩ

* C_1 = C_2 = 1000µF 63V EYF (ROE)
C_3 = C_4 = C_5 = C_6 = 2,2µF 50V
C_7 = 390pF Film
C_8 = 22nF MKT 1837 (ERO)
C_9 = 2.7nF KP 1830 (ERO)
C_{10} = 0.33µF Film
C_{11} = 1nF
** C_{12} = C_{13} = C_{14} = 100µF 40V EKR (ROE)
C_{15} = 1µF Film

D1 = SB 560 (OR EQUIVALENT)

L1 = 150µH
core 58310 MAGNETICS
45 TURNS 0.91mm (AWG 19)
COGEMA 949181

* 2 capacitors in parallel to increase input RMS current capability.
* * 3 capacitors in parallel to reduce total output ESR.

Table A

V_0	R_9	R_7
12V	4.7kΩ	6.2kW
15V	4.7kΩ	9.1kΩ
18V	4.7kΩ	12Ω
24V	4.7kΩ	18Ω

Note:
In the Test and Application Circuit for L4972D are not mounted C2, C14 and R8.

Table B
SUGGESTED BOOSTRAP CAPACITORS

Operating Frequency	Boostrap Cap.c10
f = 20KHz	≥680nF
f = 50KHz	≥470nF
f = 100KHz	≥330nF
f = 200KHz	≥220nF
f = 500KHz	≥100nF

Figure 6b: P.C. Board and Component Layout of the Circuit of Fig. 5. (1:1 scale)

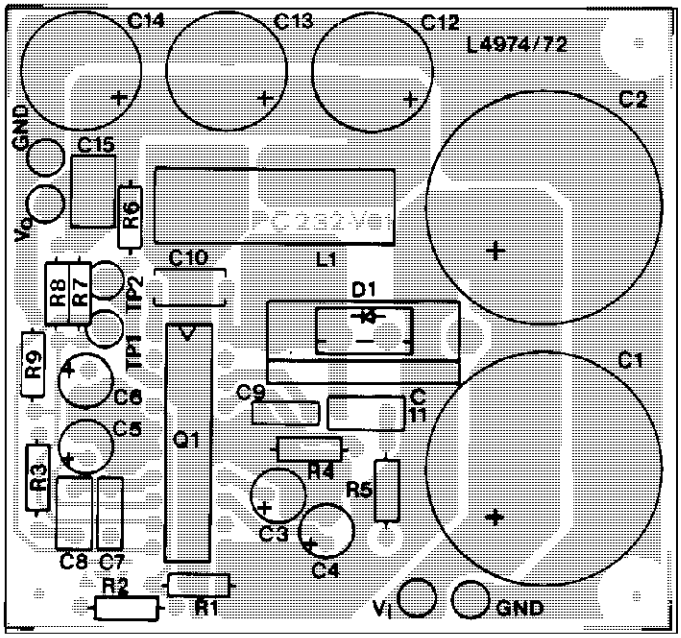


Figure 7 : DC Test Circuits.

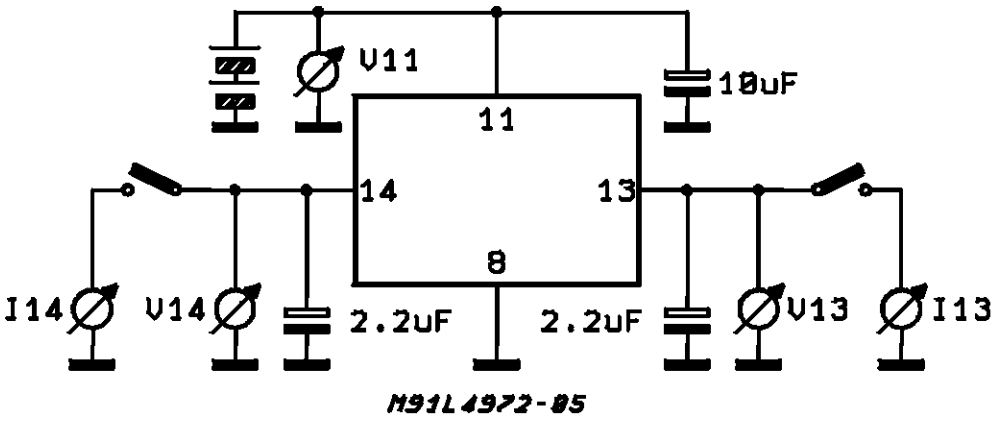


Figure 7A.

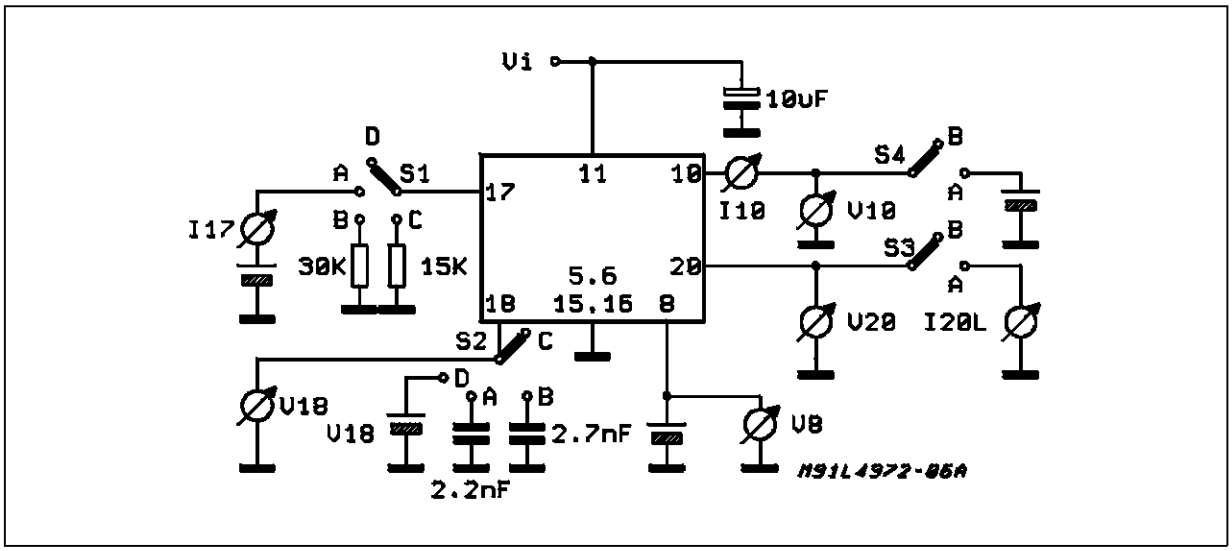


Figure 7B.

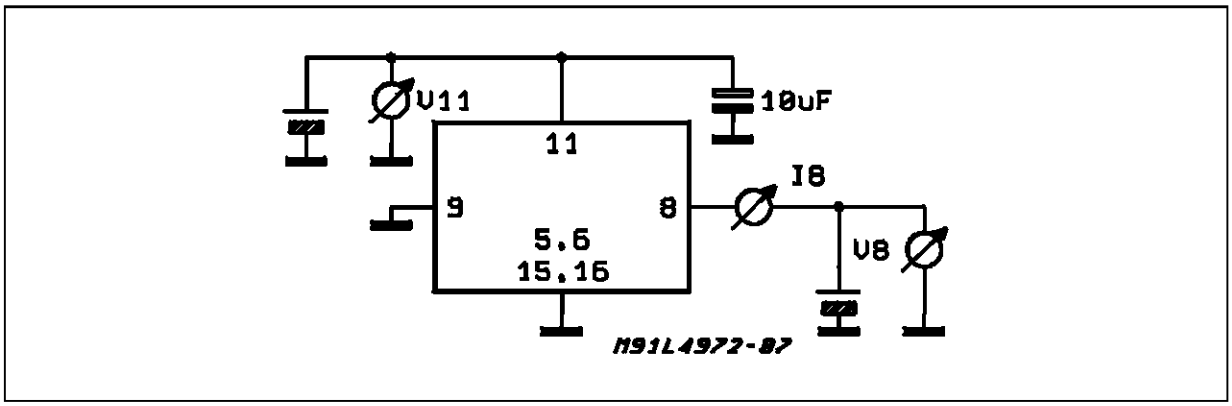


Figure 7C.

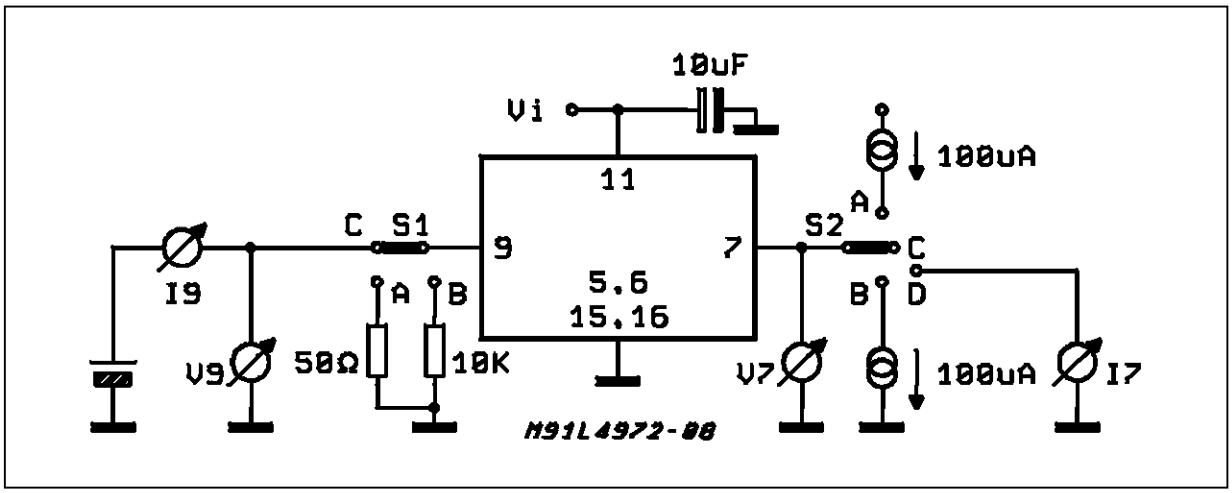


Figure 7D.

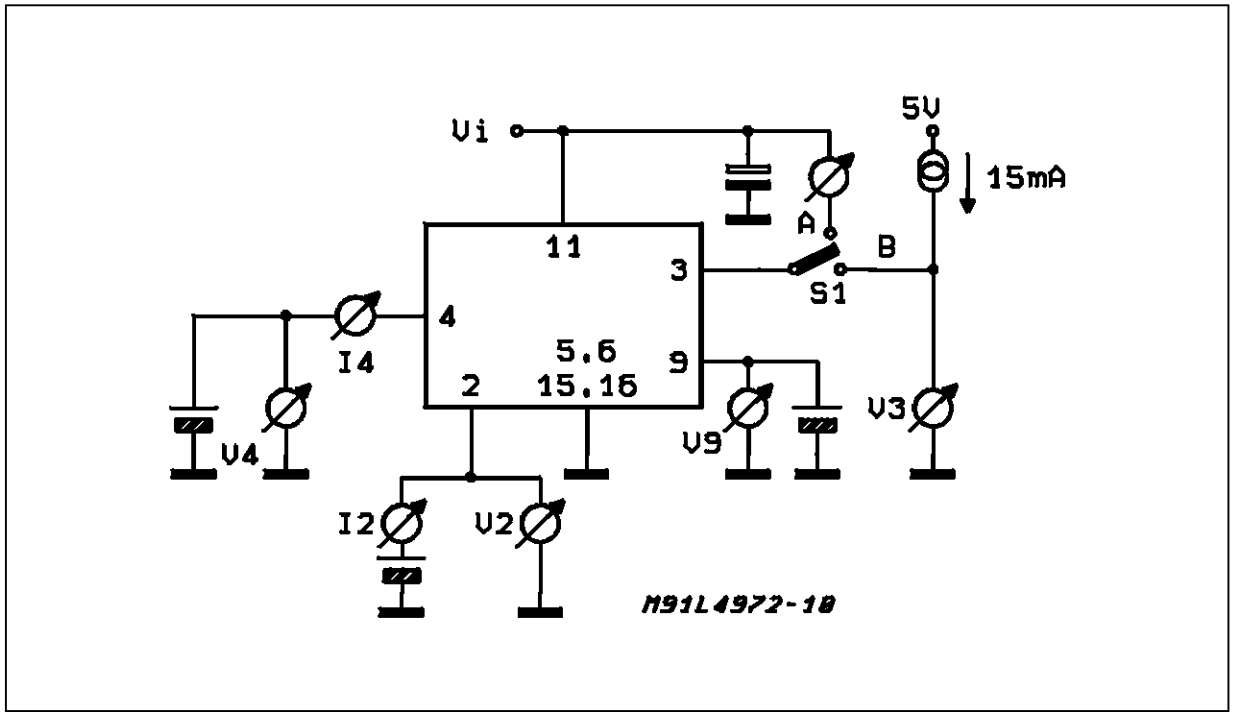


Figure 8 : Quiescent Drain Current vs. Supply Voltage (0% duty cycle - see fig. 7A).

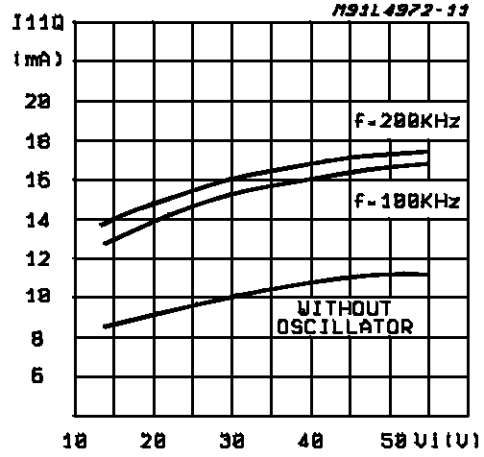


Figure 9 : Quiescent Drain Current vs. Junction Temperature (0% duty cycle).

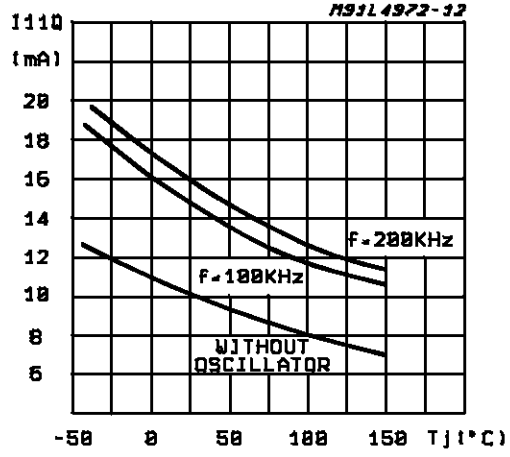


Figure 10 : Quiescent Drain Current vs. Duty Cycle.

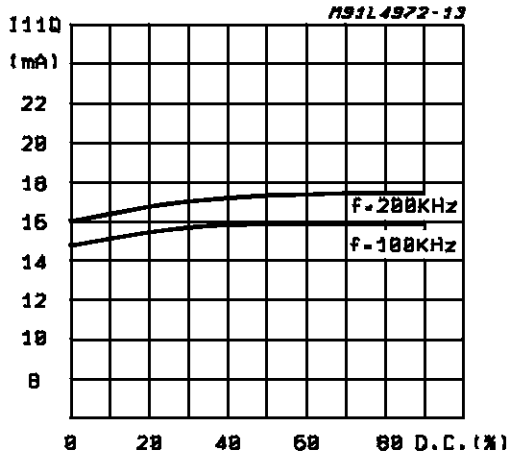


Figure 11 : Reference Voltage (pin 13) vs. Vi (see fig. 7).

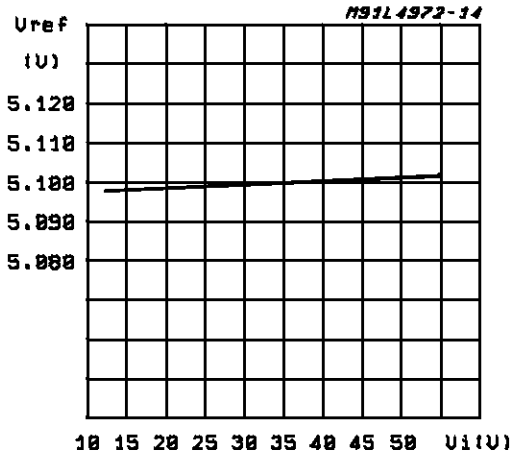


Figure 12 : Reference Voltage (pin 13) vs. Junction Temperature (see fig. 7).

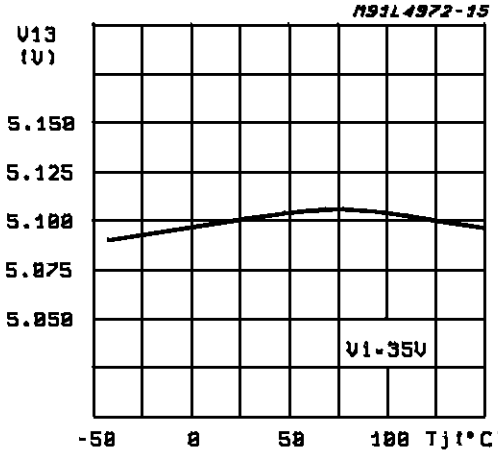


Figure 13 : Reference Voltage (pin 14) vs. Vi (see fig. 7).

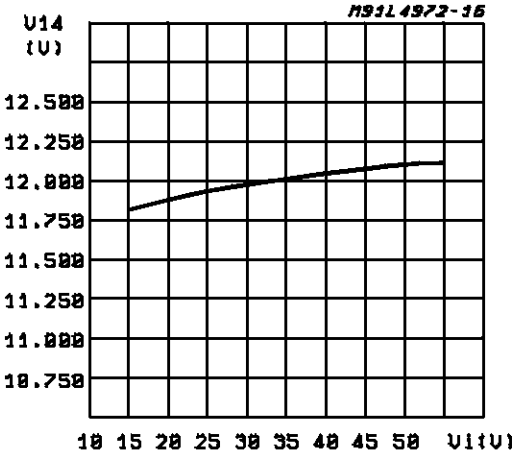


Figure 14 : Reference Voltage (pin 14) vs. Junction Temperature (see fig. 7).

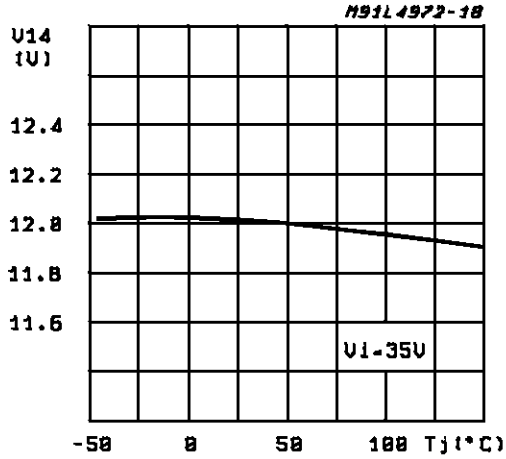


Figure 15 : Reference Voltage 5.1V (pin 13) Supply Voltage Ripple Rejection vs. Fre-

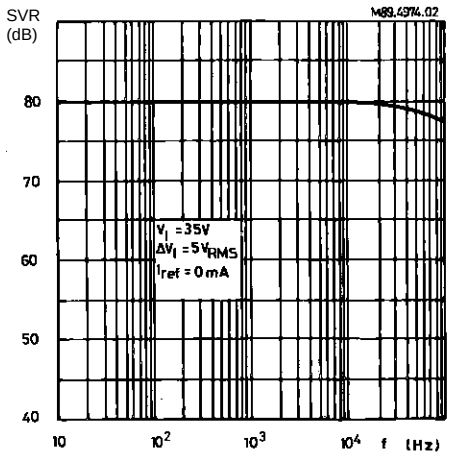


Figure 16 : Switching Frequency vs. Input Voltage (see fig. 5).

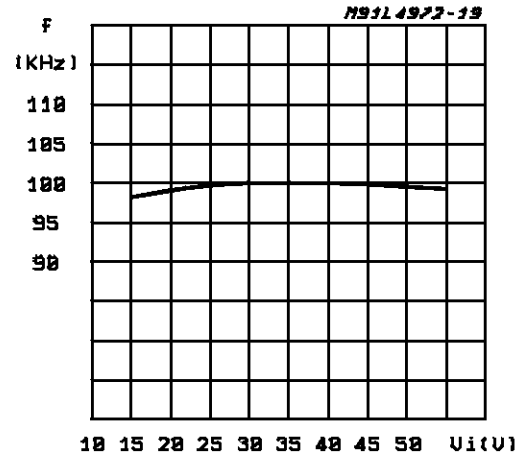


Figure 17 : Switching Frequency vs. Junction Temperature (see fig. 5).

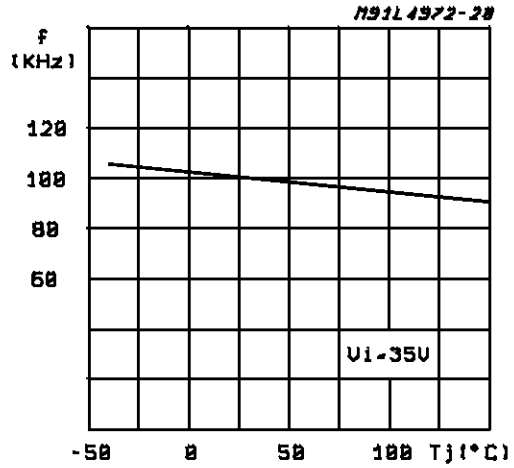


Figure 18 : Switching Frequency vs. R4 (see fig.5).

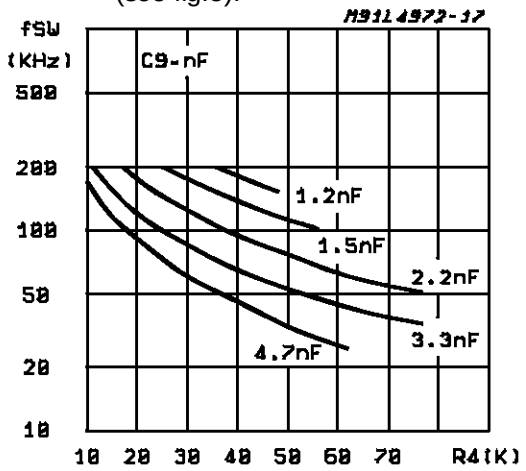


Figure 19 : Maximum Duty Cycle vs. Frequency.

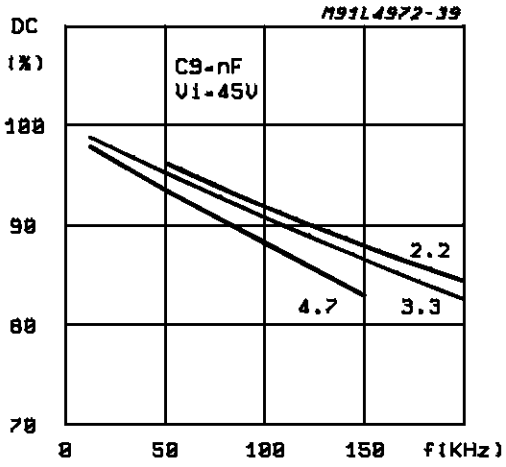


Figure 20 : Supply Voltage Ripple Rejection vs. Frequency (see fig. 5).

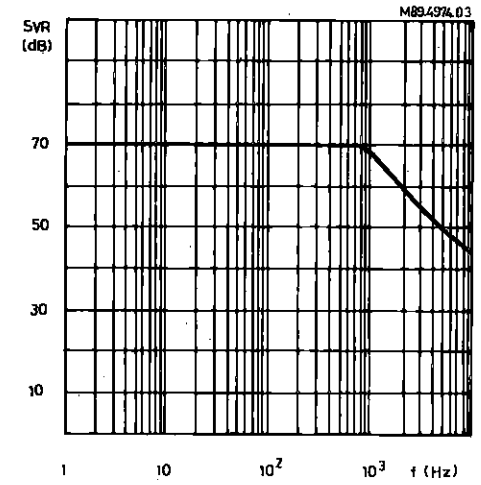


Figure 21 : Efficiency vs. Output Voltage.

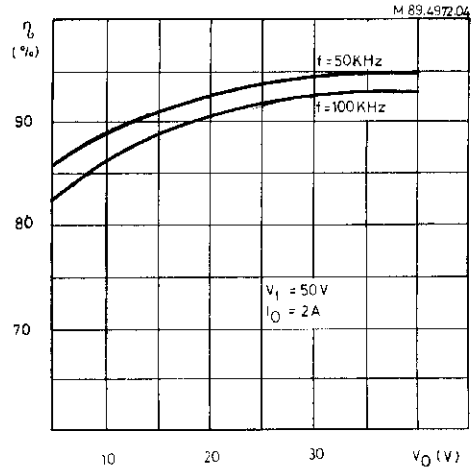


Figure 22 : Line Transient Response (see fig. 5).

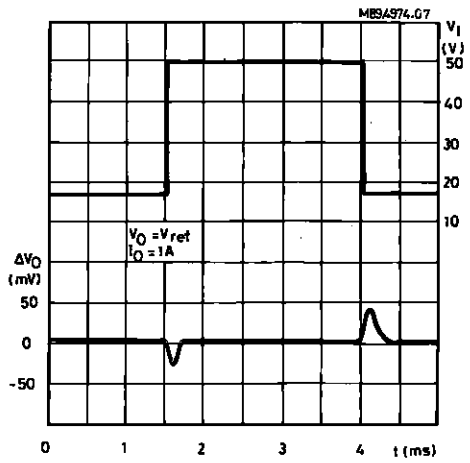


Figure 23 : Load Transient Response (see fig. 5).

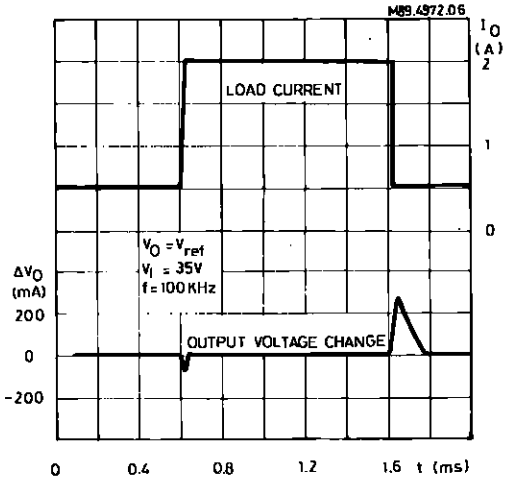


Figure 24 : Dropout Voltage between Pin 11 and Pin 20 vs. Current at Pin 20.

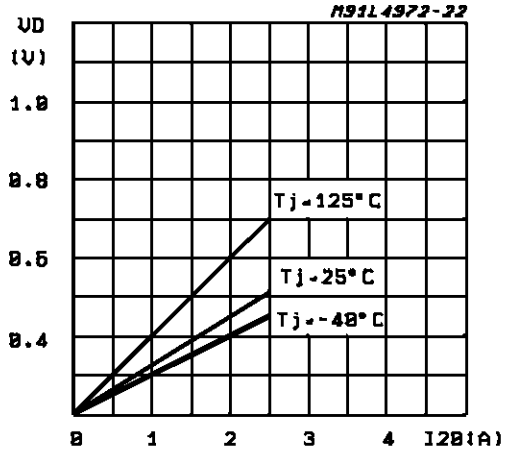


Figure 25 : .Dropout Voltage between Pin 11 and Pin 20 vs. Junction Temperature.

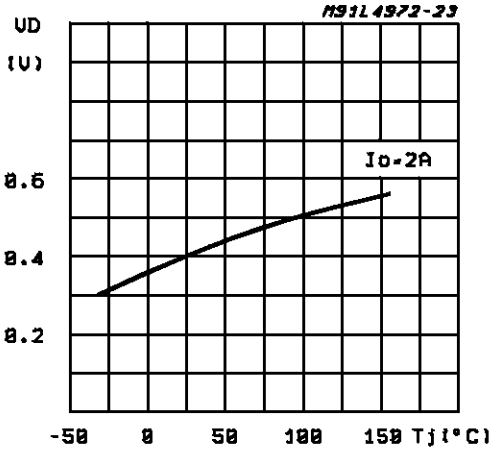


Figure 26 : Power Dissipation (device only) vs. Input Voltage.

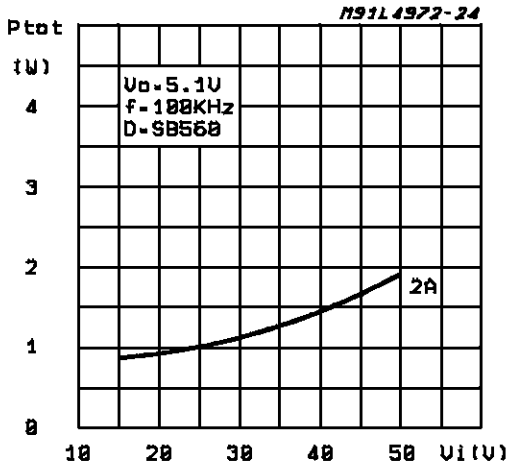


Figure 27 : Power Dissipation (device only) vs. Input Voltage.

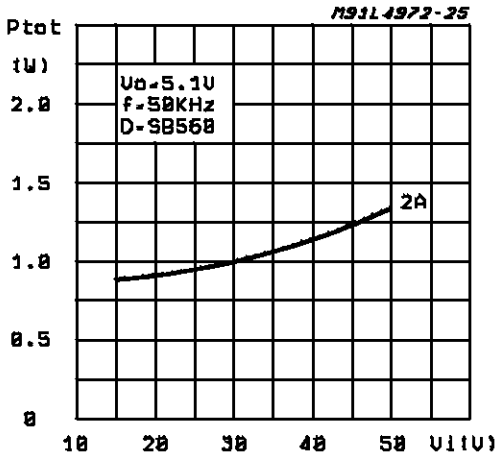


Figure 28 : Power Dissipation (device only) vs. Output Voltage.

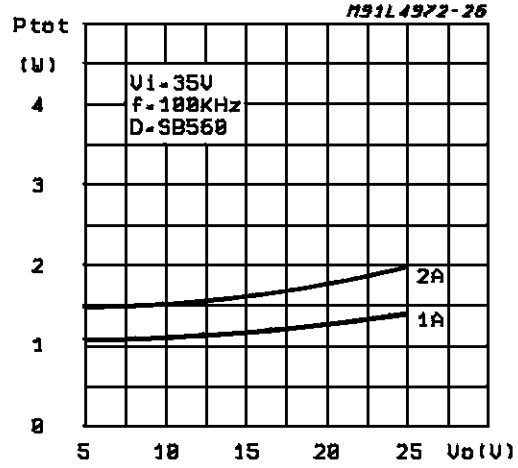


Figure 29 : Power Dissipation (device only) vs. Output Voltage.

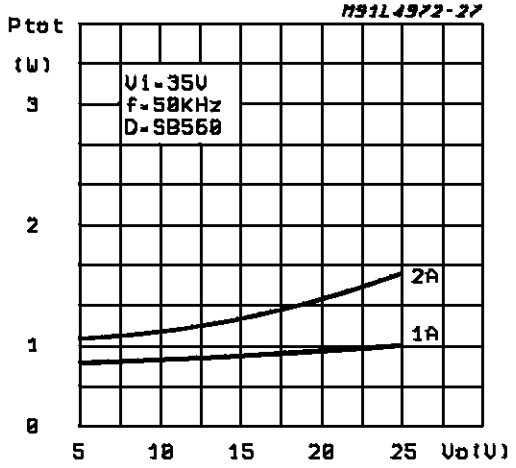


Figure 30 : Power Dissipation (device only) vs. Output Current.

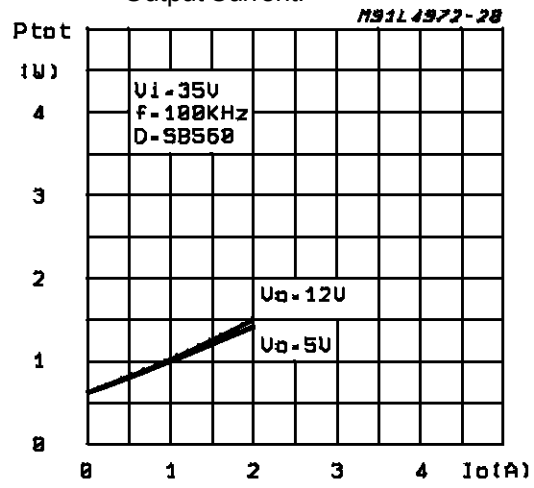


Figure 31 : Power Dissipation (device only) vs. Output Current.

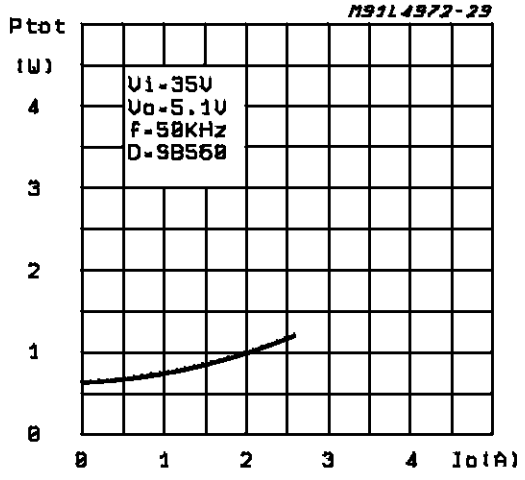


Figure 32 : Efficiency vs. Output Current.

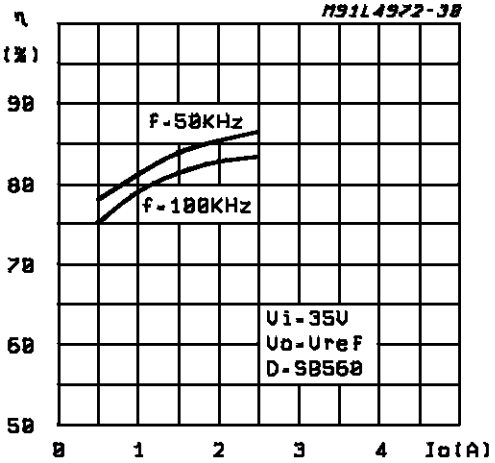


Figure 33 : Test PCB Thermal Characteristic.

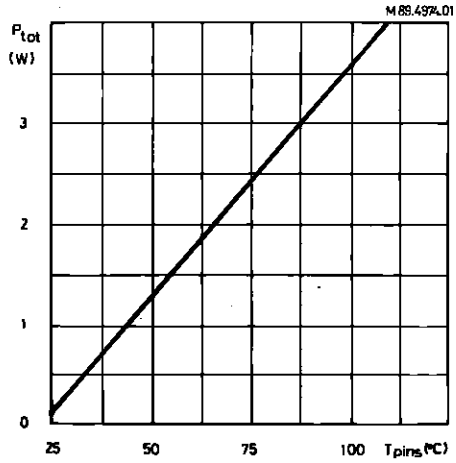


Figure 34 : Junction to Ambient Thermal Resistance vs. Area on Board Heatsink (DIP 16+2+2)

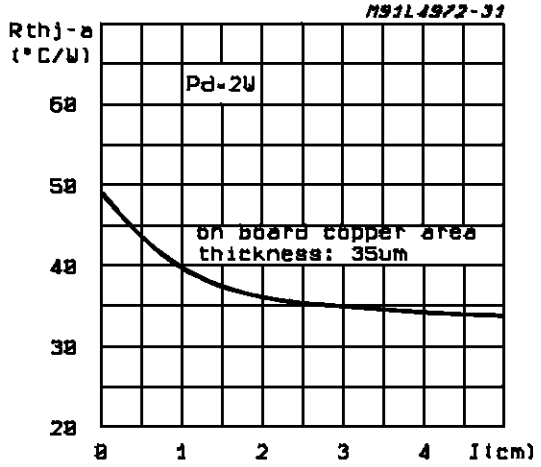


Figure 35: Junction to Ambient Thermal Resistance vs. Area on Board Heatsink (SO20)

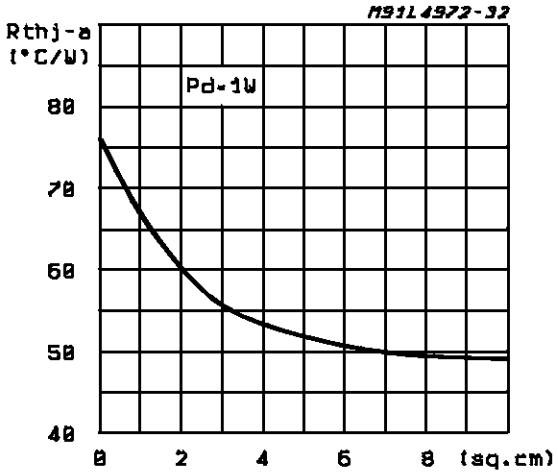


Figure 36: Maximum Allowable Power Dissipation vs. Ambient Temperature (Powerdip)

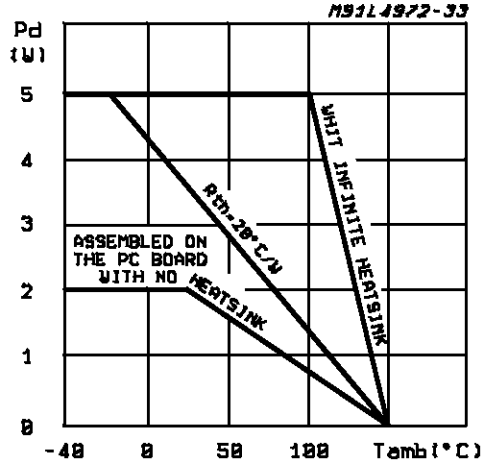


Figure 37: Maximum Allowable Power Dissipation vs. Ambient Temperature (SO20)

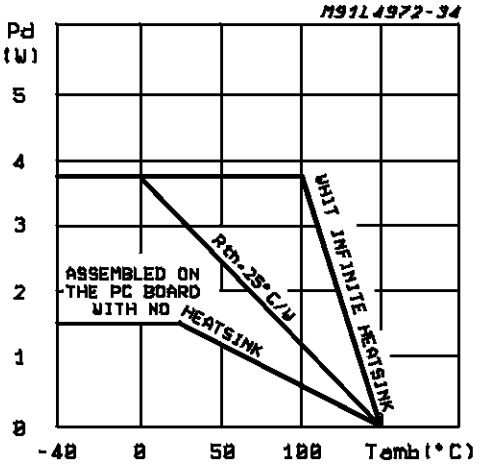


Figure 38: Open Loop Frequency and Phase of Error Amplifier (see fig. 7C).

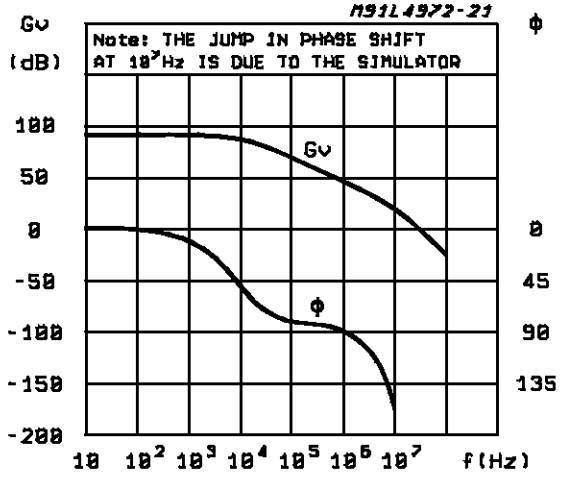


Figure 39 : 2A – 5.1V Low Cost Application Circuit.

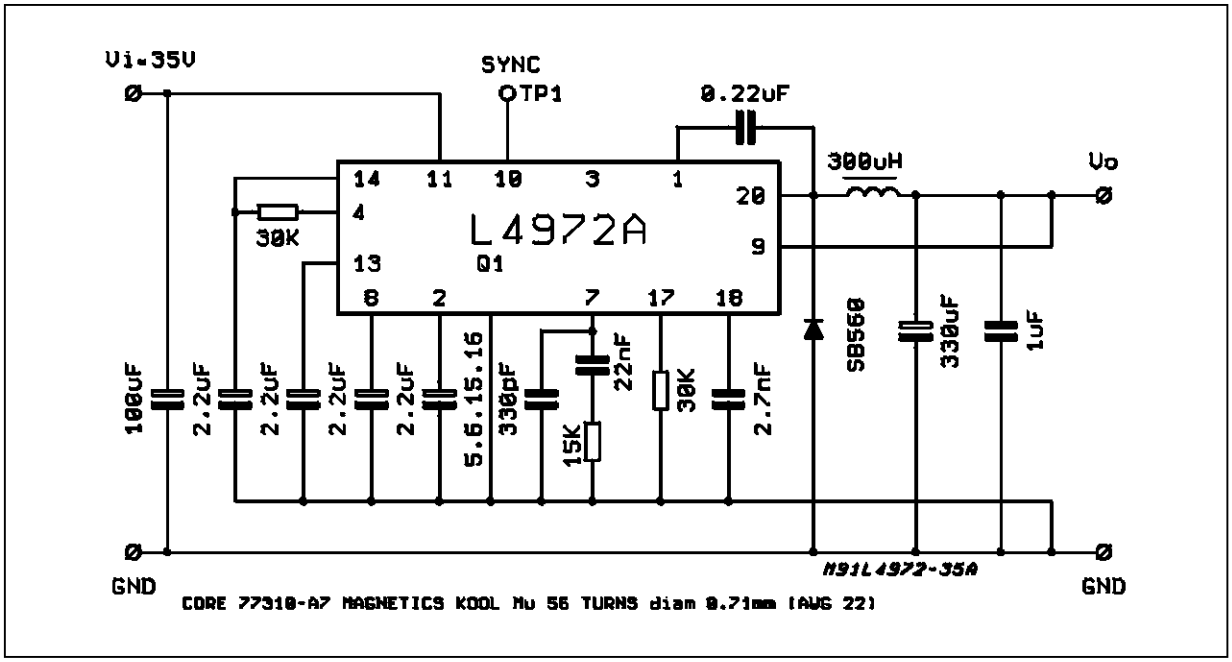


Figure 40 : A 5.1V/12V Multiple Supply. Note the Synchronization between the L4972A and L4970A.

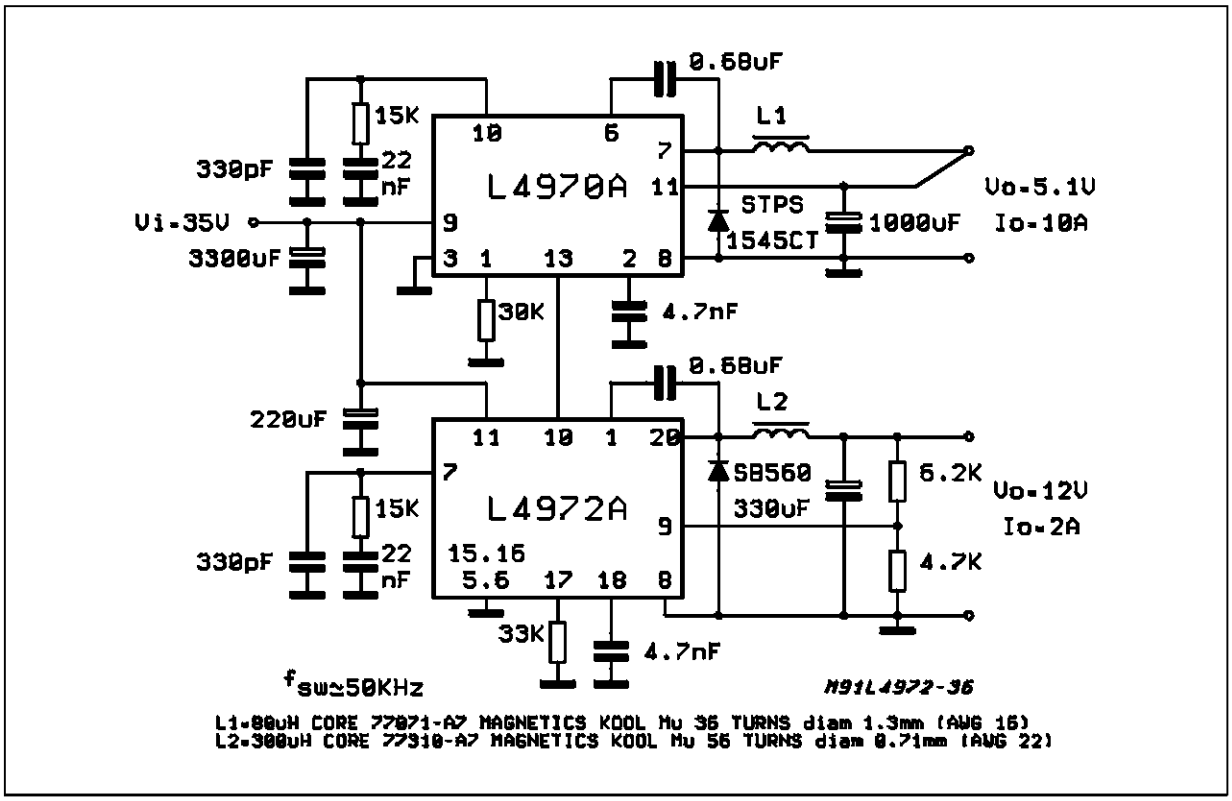


Figure 41 : L4972A's Sync. Example.

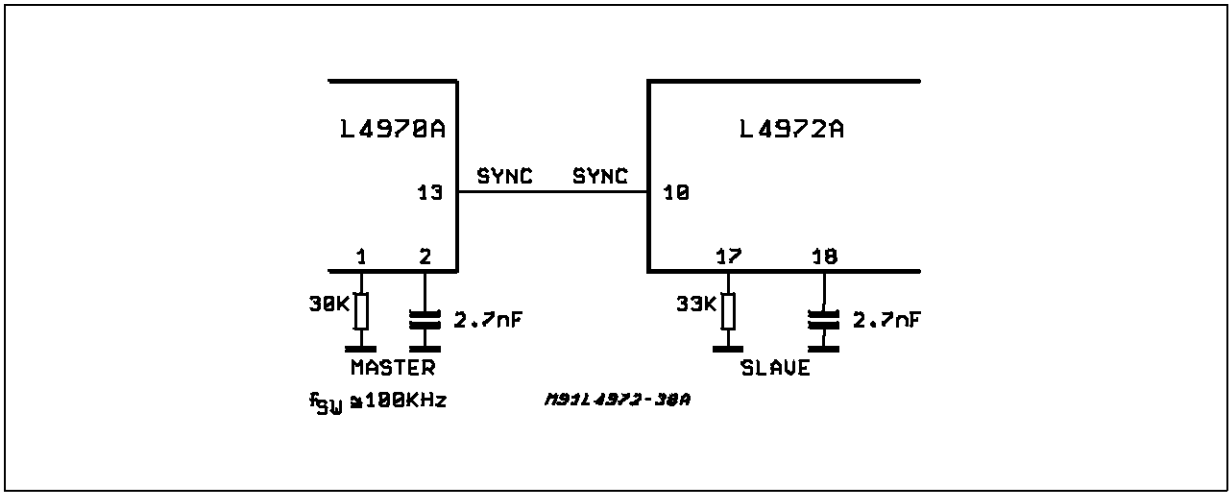
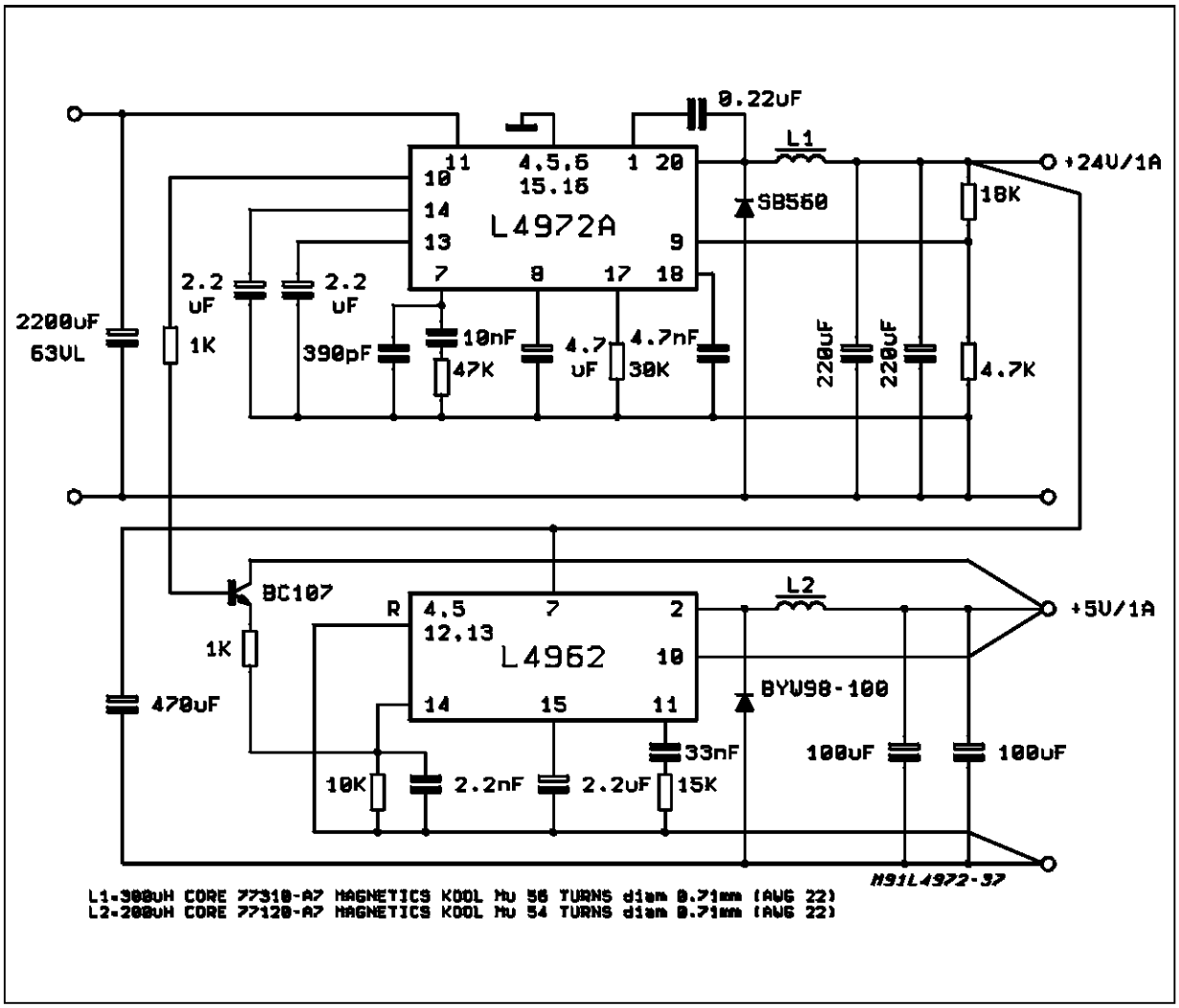
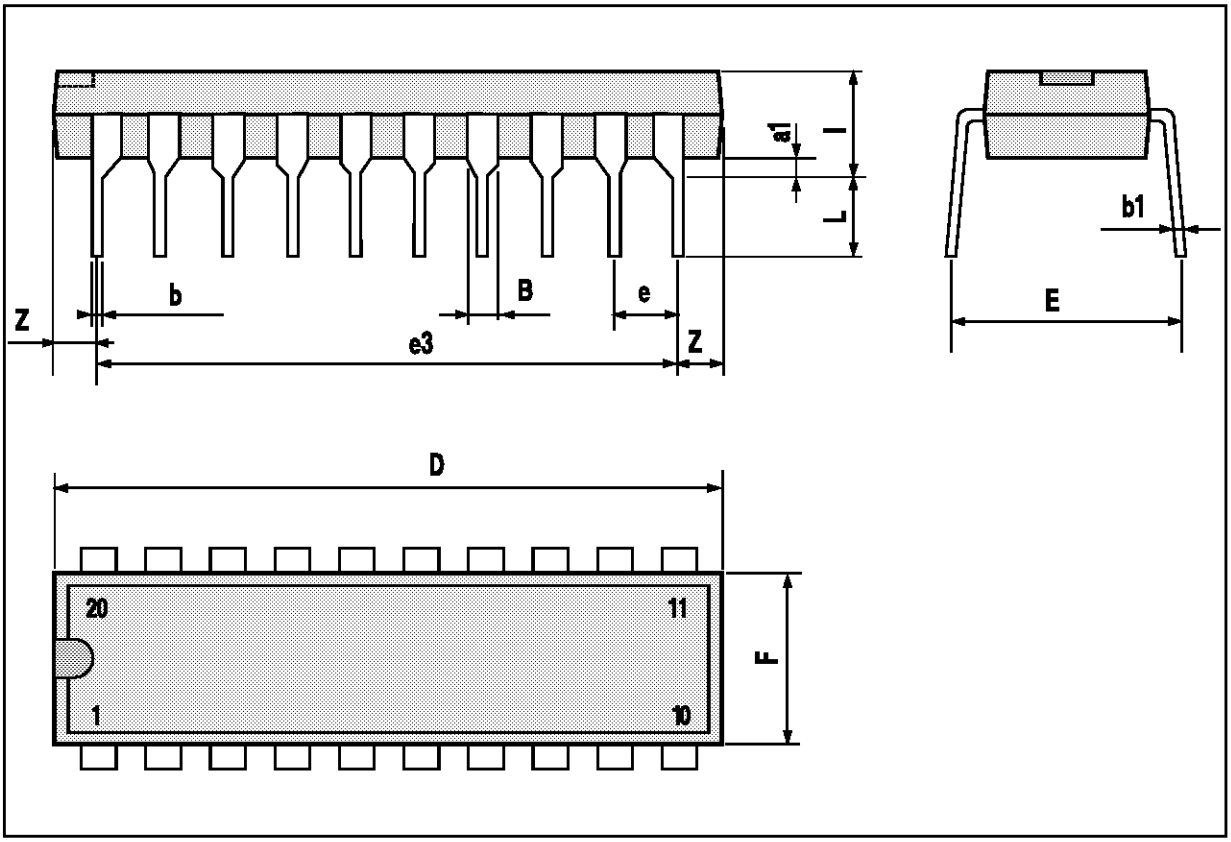


Figure 42: 1A/24V Multiple Supply. Note the synchronization between the L4972A and L4962



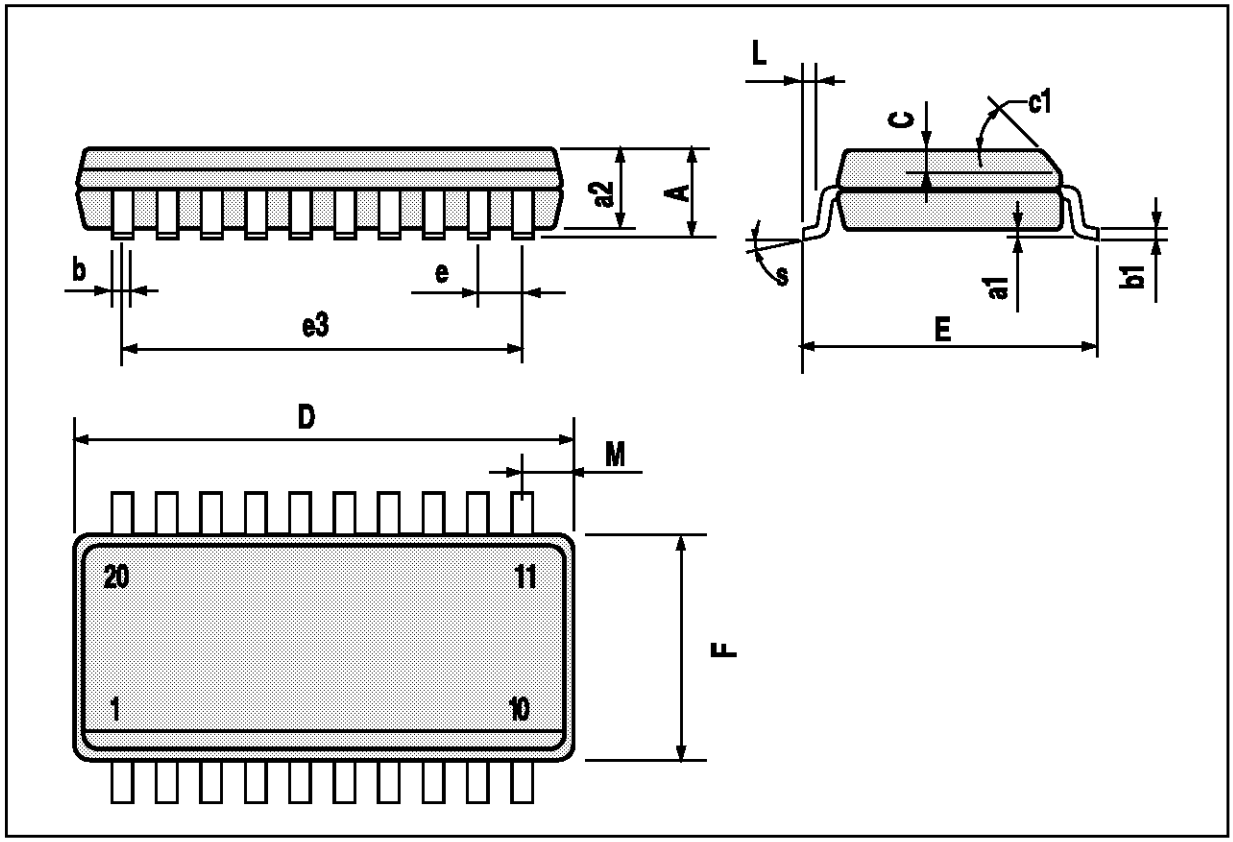
POWERDIP20 PACKAGE MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
a1	0.51			0.020		
B	0.85		1.40	0.033		0.055
b		0.50			0.020	
b1	0.38		0.50	0.015		0.020
D			24.80			0.976
E		8.80			0.346	
e		2.54			0.100	
e3		22.86			0.900	
F			7.10			0.280
I			5.10			0.201
L		3.30			0.130	
Z			1.27			0.050



SO20 PACKAGE MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			2.65			0.104
a1	0.1		0.3	0.004		0.012
a2			2.45			0.096
b	0.35		0.49	0.014		0.019
b1	0.23		0.32	0.009		0.013
C		0.5			0.020	
c1	45 (typ.)					
D	12.6		13.0	0.496		0.512
E	10		10.65	0.394		0.419
e		1.27			0.050	
e3		11.43			0.450	
F	7.4		7.6	0.291		0.299
L	0.5		1.27	0.020		0.050
M			0.75			0.030
S	8 (max.)					



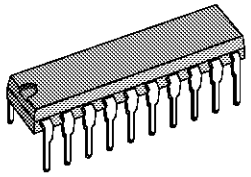
SGS-THOMSON MICROELECTRONICS

L4974A

3.5A SWITCHING REGULATOR

- 3.5A OUTPUT CURRENT
- 5.1V TO 40V OUTPUT VOLTAGE RANGE
- 0 TO 90% DUTY CYCLE RANGE
- INTERNAL FEED-FORWARD LINE REG.
- INTERNAL CURRENT LIMITING
- PRECISE 5.1V ± 2% ON CHIP REFERENCE
- RESET AND POWER FAIL FUNCTIONS
- INPUT/OUTPUT SYNC PIN
- UNDER VOLTAGE LOCK OUT WITH HYSTERETIC TURN-ON
- PWM LATCH FOR SINGLE PULSE PER PERIOD
- VERY HIGH EFFICIENCY
- SWITCHING FREQUENCY UP TO 200KHz
- THERMAL SHUTDOWN
- CONTINUOUS MODE OPERATION

MULTIPOWER BCD TECHNOLOGY



POWERDIP (16 + 2 + 2)

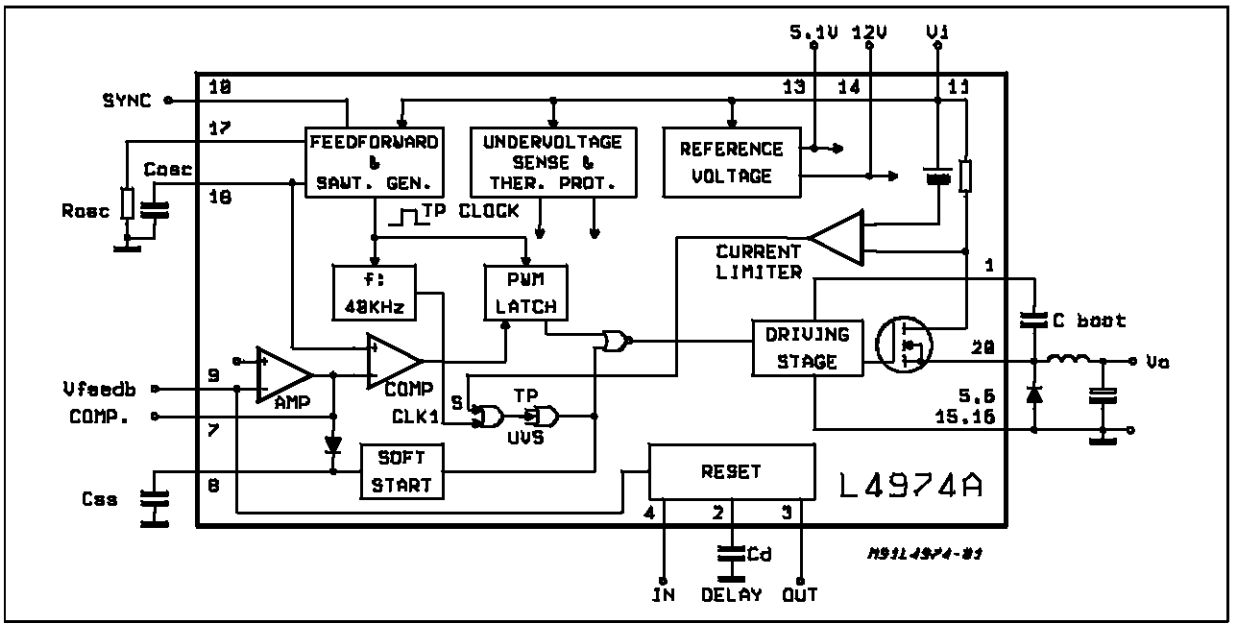
ORDERING NUMBER : L4974A

DESCRIPTION

The L4974A is a stepdown monolithic power switching regulator delivering 3.5A at a voltage variable from 5.1 to 40V.

Realized with BCD mixed technology, the device uses a DMOS output transistor to obtain very high efficiency and very fast switching times. Features of the L4974A include reset and power fail for microprocessors, feed forward line regulation, soft start, limiting current and thermal protection. The device is mounted in a Powerdip 16 + 2 + 2 plastic package and requires few external components. Efficient operation at switching frequencies up to 200KHz allows reduction in the size and cost of external filter component.

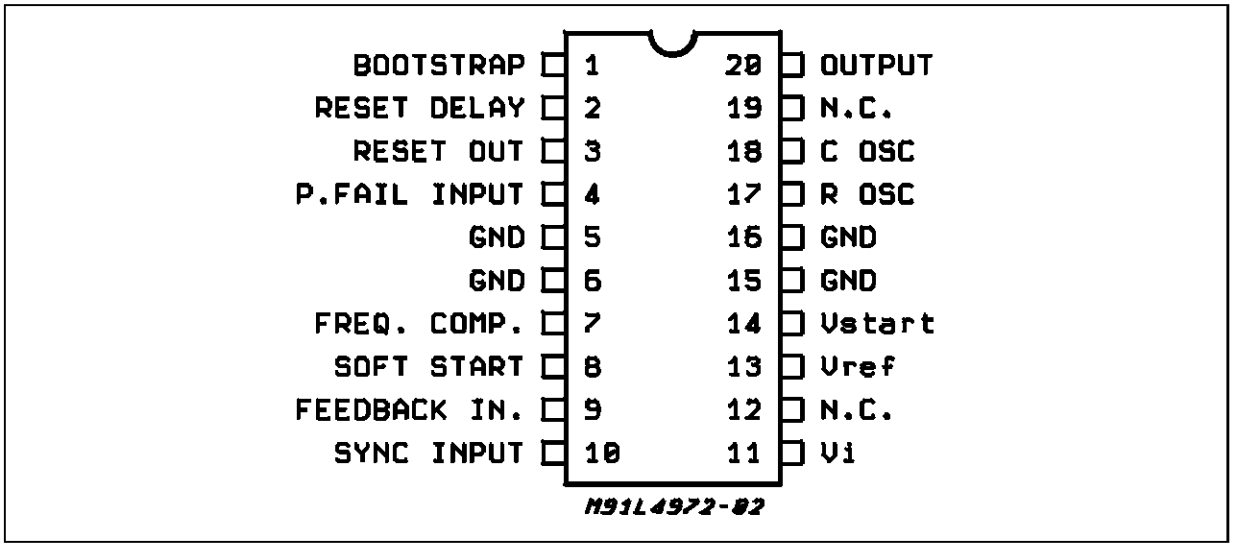
BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{11}	Input Voltage	55	V
V_{11}	Input Operating Voltage	50	V
V_{20}	Output DC Voltage Output Peak Voltage at t = 0.1µs f = 200khz	-1 -5	V V
I_{20}	Maximum Output Current	Internally Limited	
V_I	Boostrap Voltage Boostrap Operating Voltage	65 V_{11} + 15	V V
V_4, V_8	Input Voltage at Pins 4, 12	12	V
V_3	Reset Output Voltage	50	V
I_3	Reset Output Sink Current	50	mA
V_2, V_7, V_9, V_{10}	Input Voltage at Pin 2, 7, 9, 10	7	V
I_2	Reset Delay Sink Current	30	mA
I_7	Error Amplifier Output Sink Current	1	A
I_8	Soft Start Sink Current	30	mA
P_{tot}	Total Power Dissipation at $T_{PINS} \leq 90°C$ at T_{amb} = 70°C (No copper area on PCB)	5 1.3	W W
T_J, T_{stg}	Junction and Storage Temperature	-40 to 150	°C

PIN CONNECTION (top view)



THERMAL DATA

Symbol	Parameter		Value	Unit
$R_{th\ j\text{-}pins}$	Thermal Resistance Junction-Pins	max	12	°C/W
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient	max	60	°C/W

PIN FUNCTIONS

N°	Name	Function
1	BOOTSTRAP	A C_{boot} capacitor connected between this terminal and the output allows to drive properly the internal D-MOS transistor.
2	RESET DELAY	A C_d capacitor connected between this terminal and ground determines the reset signal delay time.
3	RESET OUT	Open Collector Reset/power Fail Signal Output. This output is high when the supply and the output voltages are safe.
4	RESET INPUT	Input of Power Fail Circuit. The threshold is 5.1V. It may be connected via a divider to the input for power fail function. It must be connected to the pin 14 an external 30KΩ resistor when power fail signal not required.
5, 6 15, 16	GROUND	Common Ground Terminal
7	FREQUENCY COMPENSATION	A series RC network connected between this terminal and ground determines the regulation loop gain characteristics.
8	SOFT START	Soft Start Time Constant. A capacitor is connected between thi sterminal and ground to define the soft start time constant.
9	FEEDBACK INPUT	The Feedback Terminal of the Regulation Loop. The output is connected directly to this terminal for 5.1V operation; It is connected via a divider for higher voltages.
10	SYNC INPUT	Multiple L4974A's are synchronized by connecting pin 10 inputs together or via an external syncr. pulse.
11	SUPPLY VOLTAGE	Unregulated Input Voltage.
12, 19	N.C.	Not Connected.
13	V_{ref}	5.1V V_{ref} Device Reference Voltage.
14	V_{start}	Internal Start-up Circuit to Drive the Power Stage.
17	OSCILLATOR	R_{osc}. External resistor connected to ground determines the constant charging current of C_{osc}.
18	OSCILLATOR	C_{osc}. External capacitor connected to ground determines (with R_{osc}) the switching frequency.
20	OUTPUT	Regulator Output.

CIRCUIT OPERATION

The L4974A is a 3.5A monolithic stepdown switching regulator working in continuous mode realized in the new BCD Technology. This technology allows the integration of isolated vertical DMOS power transistors plus mixed CMOS/Bipolar transistors.

The device can deliver 3.5A at an output voltage adjustable from 5.1V to 40V and contains diagnostic and control functions that make it particularly suitable for microprocessor based systems.

BLOCK DIAGRAM

The block diagram shows the DMOS power transistors and the PWM control loop. Integrated functions include a reference voltage trimmed to 5.1V ± 2%, soft start, undervoltage lockout, oscillator with feedforward control, pulse by pulse current limit, thermal shutdown and finally the reset and power fail circuit. The reset and power fail circuit provides an output signal for a microprocessor indicating the status of the system.

Device turn on is around 11V with a typical 1V hysterysis, this threshold porvides a correct voltage for the driving stage of the DMOS gate and the hysterysis prevents instabilities.

An external bootstrap capacitor charge to 12V by an internal voltage reference is needed to provide correct gate drive to the power DMOS. The driving circuit is able to source and sink peak currents of around 0.5A to the gate of the DMOS transistor. A typical switching time of the current in the DMOS transistor is 50ns. Due to the fast commutation switching frequencies up to 200kHz are possible.

The PWM control loop consists of a sawtooth oscillator, error amplifier, comparator, latch and the output stage. An error signal is produced by comparing the output voltage with the precise 5.1V ± 2% on chip reference. This error signal is then compared with the sawtooth oscillator in order to generate frixed frequency pulse width modulated drive for the output stage. A PWM latch is included to eliminate multiple pulsing within a period even in noisy environments.

The gain and stability of the loop can be adjusted by an external RC network connected to the output of the error amplifier. A voltage feedforward control has been added to the oscillator, this maintains superior line regulation over a wide input voltage range. Closing the loop directly gives an output vol-tage of 5.1V, higher voltages are obtained by inserting a voltage divider.

At turn on, output overcurrents are prevented by the soft start function (fig. 2). The error amplifier is initially clamped by an external capacitor, Css, and allowed to rise linearly under the charge of an internal constant current source.

Output overload protection is provided by a current limit circuit. The load current is sensed by a internal metal resistor connected to a comparator. When the load current exceeds a preset threshold, the output of the comparator sets a flip flop which turns off the power DMOS. The next clock pulse, from an internal 40kHz oscillator, will reset the flip flop and the power DMOS will again conduct. This current protection method, ensures a constant current output when the system is overloaded or short circuited and limits the switching frequency, in this condition, to 40kHz. The Reset and Power fail circuit (fig. 4), generates an output signal when the supply voltage exceeds a threshold programmed by an external voltage divider. The reset signal, is generated with a delay time programmed by a external capacitor on the delay pin. When the supply voltage falls below the threshold or the output voltage goes below 5V, the reset output goes low immediately. The reset output is an open drain.

Fig. 4A shows the case when the supply voltage is higher than the threshold, but the output voltage is not yet 5V.

Fig. 4B shows the case when the output is 5.1V, but the supply voltage is not yet higher than the fixed threshold.

The thermal protection disables circuit operation when the junction temperature reaches about 150°C and has a hysterysis to prevent unstable conditions.

Figure 1 : Feedforward Waveform.

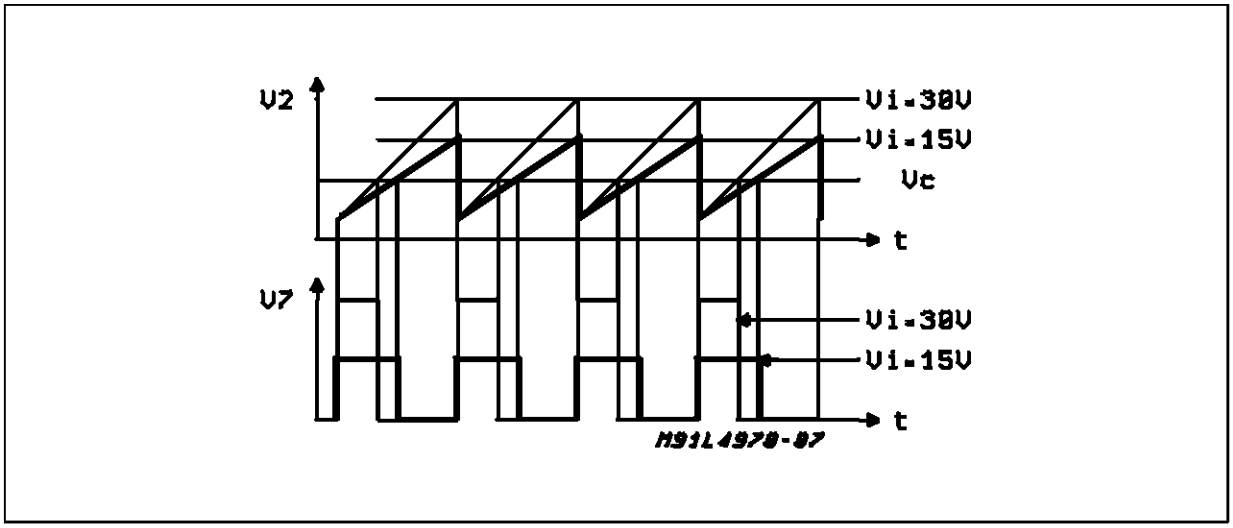


Figure 2 : Soft Start Function.

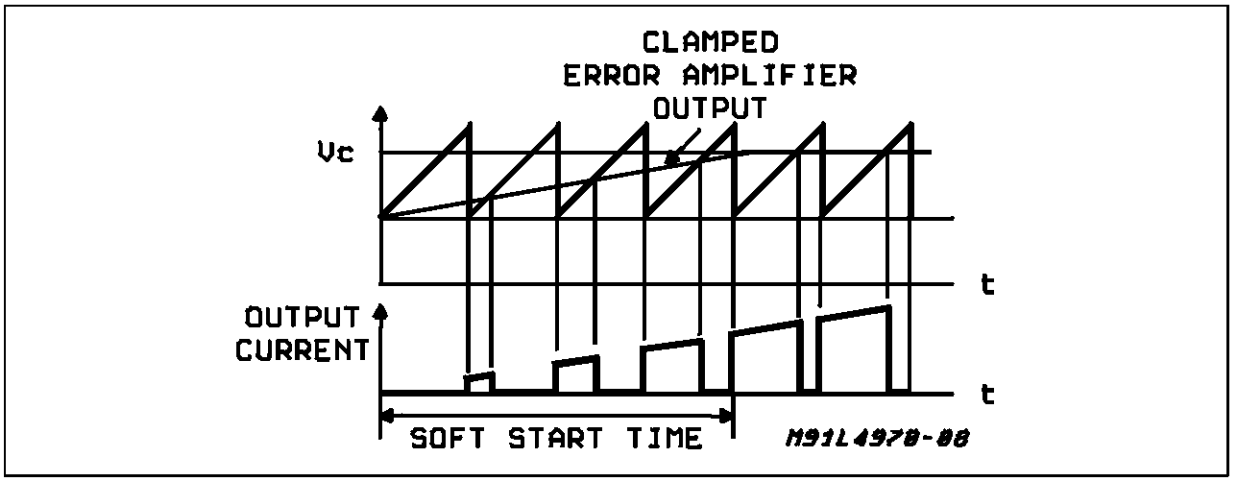


Figure 3 : Limiting Current Function.

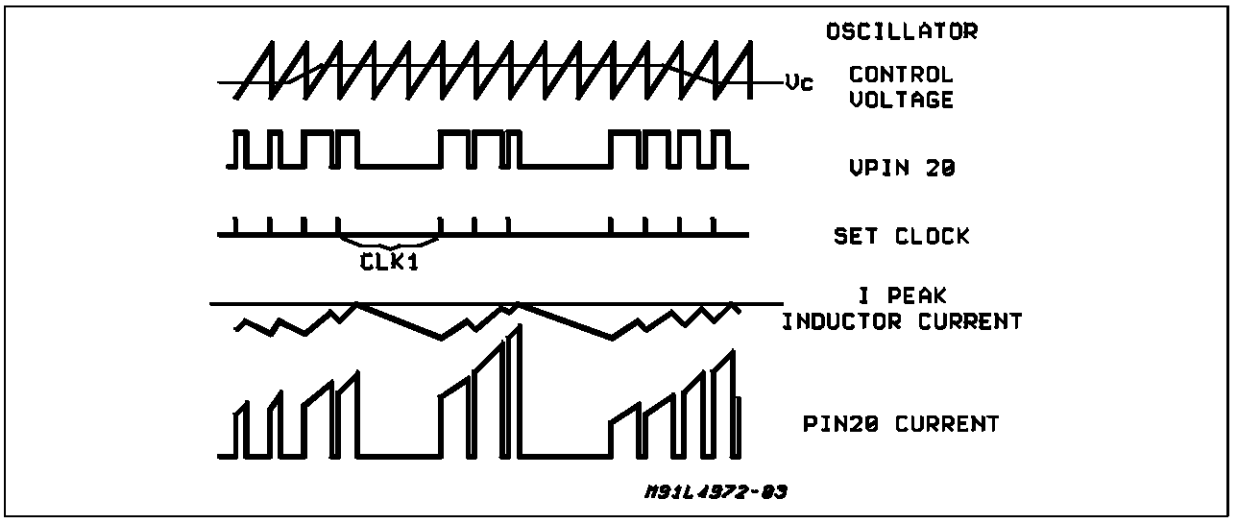
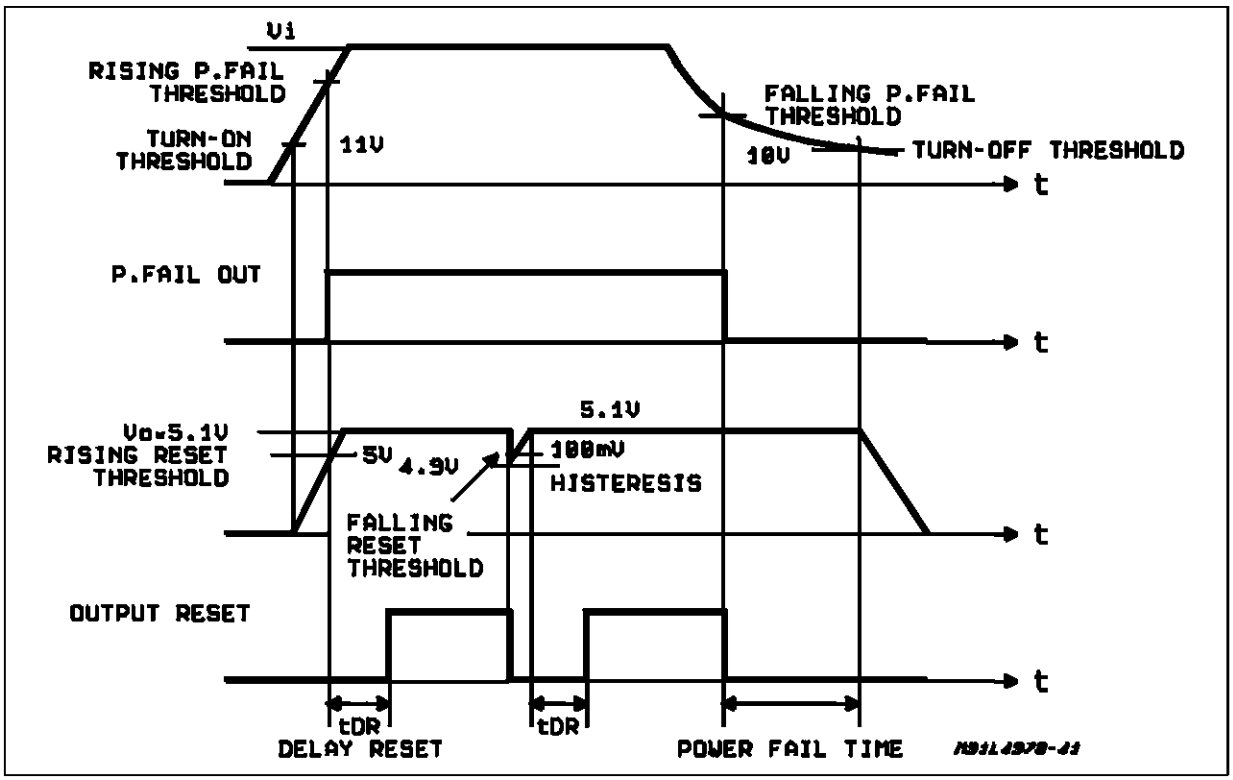
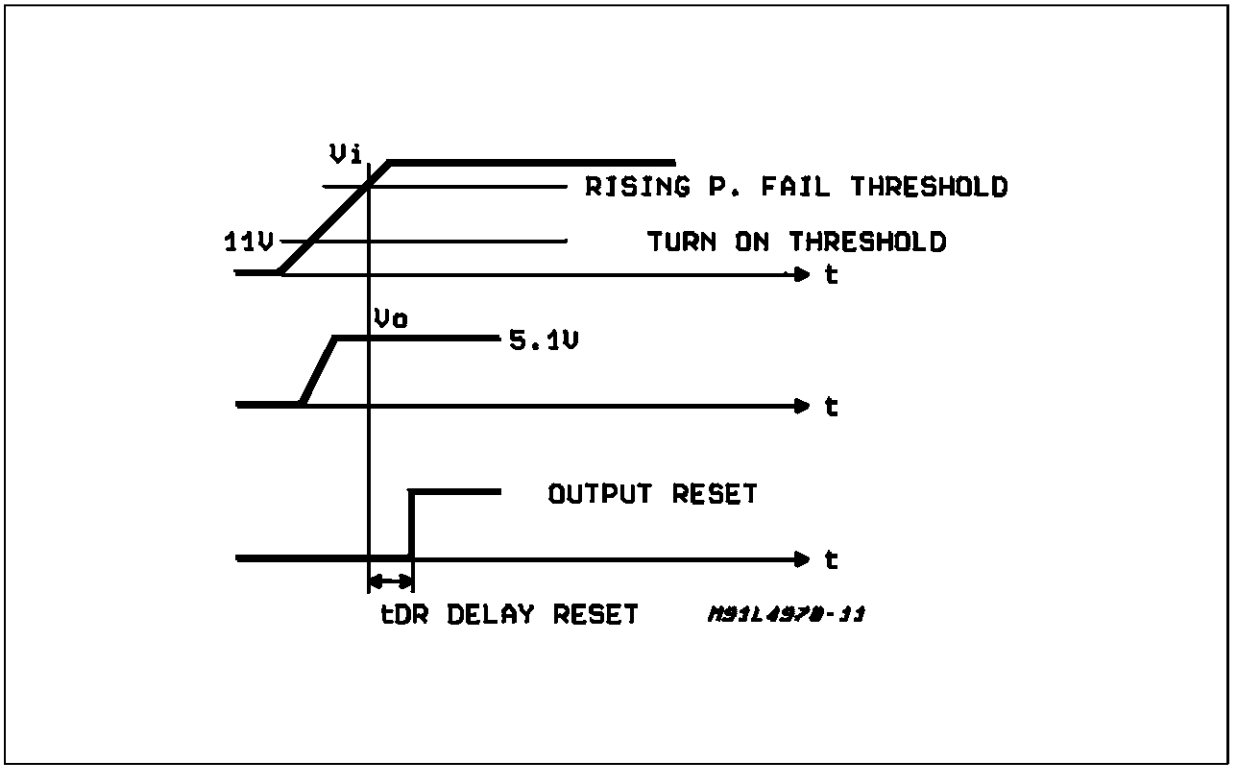


Figure 4 : Reset and Power Fail Functions.

A



B



ELECTRICAL CHARACTERISTICS (refer to the test circuit, T_J = 25°C, V_i = 35V, R_4 = 30KΩ, C_9 = 2.7nF, f_{SW} = 100KHz typ, unless otherwise specified)

DYNAMIC CHARACTERISTICS

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit	Fig.
V_i	Input Volt. Range (pin 11)	V_o = V_{ref} to 40V I_o = 3.5A (*)	15		50	V	5
V_o	Output Voltage	V_i =15V to 50V I_o = 2A; V_o = V_{ref}	5	5.1	5.2	V	5
ΔV_o	Line Regulation	V_I = 15V to 50V I_o = 1A; V_o = V_{ref}		12	30	mV	
ΔV_o	Load Regulation	V_O = V_{ref} I_o = 1A to 3.5A		8	25	mV	
		I_o = 2A to 3A		4	10	mV	
V_d	Dropout Voltage between Pin 11 and 20	I_o = 2A I_o = 3.5A		0.25 0.45	0.4 0.7	V	
I_{20L}	Max Limiting Current	V_i = 15V to 50V V_o = V_{ref} to 40V	4	4.75	5.5	A	
η	Efficiency	I_o = 3.5A, f = 100KHz V_o = V_{ref} V_o = 12V	80	85 90		% %	
SVR	Supply Voltage Ripple Rejection	V_i = 2VRMS; I_o = 5A f = 100Hz; V_o = V_{ref}	56	60		dB	5
f	Switching Frequency		90	100	110	KHz	5
$\Delta f/\Delta Vi$	Voltage Stability of Switching Frequency	V_i = 15V to 45V		2	6	%	5
$\Delta f/T_j$	Temperature Stability of Switching Frequency	T_j = 0 to 125°C		1		%	5
f_{max}	Maximum Operating Switching Frequency	V_o = V_{ref} R_4 = 15KΩ I_o = 3.5A C_9 = 2.2nF	200			KHz	5

(*) Pulse testing with a low duty cycle

V_{ref} SECTION (pin 13)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit	Fig.
V_{13}	Reference Voltage		5	5.1	5.2	V	7
ΔV_{13}	Line Regulation	V_i = 15V to 50V		10	25	mV	7
ΔV_{13}	Load Regulation	I_{13} = 0 to 1mA		20	40	mV	7
$\frac{\Delta V_{13}}{\Delta T}$	Average Temperature Coefficient Reference Voltage	T_j = 0°C to 125°C		0.4		mV/°C	7
$I_{13\ short}$	Short Circuit Current Limit	V_{13} = 0		70		mA	7

V_{START} SECTION (pin 15)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit	Fig.
V_{14}	Reference Voltage		11.4	12	12.6	V	7
ΔV_{14}	Line Regulation	V_i = 15 to 50V		0.6	1.4	V	7
ΔV_{14}	Load Regulation	I_{14} = 0 to 1mA		50	200	mV	7
$I_{14\ short}$	Short Circuit Current Limit	V_{15} = 0V		80		mA	7

ELECTRICAL CHARACTERISTICS (continued)

DC CHARACTERISTICS

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit	Fig.
V_{11on}	Turn-on Threshold		10	11	12	V	7A
$V_{11\ Hyst}$	Turn-off Hysteresys			1		V	7A
I_{11Q}	Quiescent Current	$V_8 = 0$; S1 = D		13	19	mA	7A
I_{11OQ}	Operating Supply Current	$V_8 = 0$; S1 = B; S2 = B		16	23	mA	7A
I_{20L}	Out Leak Current	$V_i = 55V$; S3 = A; $V_8 = 0$			2	mA	7A

SOFT START (pin 8)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit	Fig.
I_8	Soft Start Source Current	$V_8 = 3V$; $V_9 = 0V$	80	115	150	µA	7B
V_8	Output Saturation Voltage	$I_8 = 20mA$; $V_{11} = 10V$ $I_8 = 200µA$; $V_{11} = 10V$			1 0.7	V V	7B 7B

ERROR AMPLIFIER

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit	Fig.
V_{7H}	High Level Out Voltage	$I_7 = -100µA$; S1 = C $V_9 = 4.7V$	6			V	7C
V_{7L}	Low Level Out Voltage	$I_7 = 100µA$; S1 = C $V_9 = 5.3V$;			1.2	V	7C
I_{7H}	Source Output Current	$V_7 = 1V$; $V_7 = 4.7V$	100	150		µA	7C
$-I_{7L}$	Sink Output Current	$V_7 = 6V$; $V_9 = 5.3V$	100	150		µA	7C
I_9	Input Bias Current	S1 = B; $R_S = 10K\Omega$		0.4	3	µA	7C
G_V	DC Open Loop Gain	S1 = A; $R_S = 10\Omega$	60			dB	7C
SVR	Supply Voltage Rejection	$15 < V_i < 50V$	60	80		dB	7C
V_{OS}	Input Offset Voltage	$R_S = 50\Omega$ S1 = A		2	10	mV	7C

RAMP GENERATOR (pin 18)

Symbol	Parameter	Test Condition		Min.	Typ.	Max.	Unit	Fig.
V_{18}	Ramp Valley	S1 = B; S2 = B		1.2	1.5		V	7A
V_{18}	Ramp Peak	S1 = B	$V_i = 15V$		2.5		V	7A
		S2 = B	$V_i = 45V$		5.5		V	7A
I_{18}	Min. Ramp Current	S1 = A; $I_{17} = 100µA$			270	300	µA	7A
I_{18}	Max. Ramp Current	S1 = A; $I_{17} = 1mA$		2.4	2.7		mA	7A

SYNC FUNCTION (pin 10)

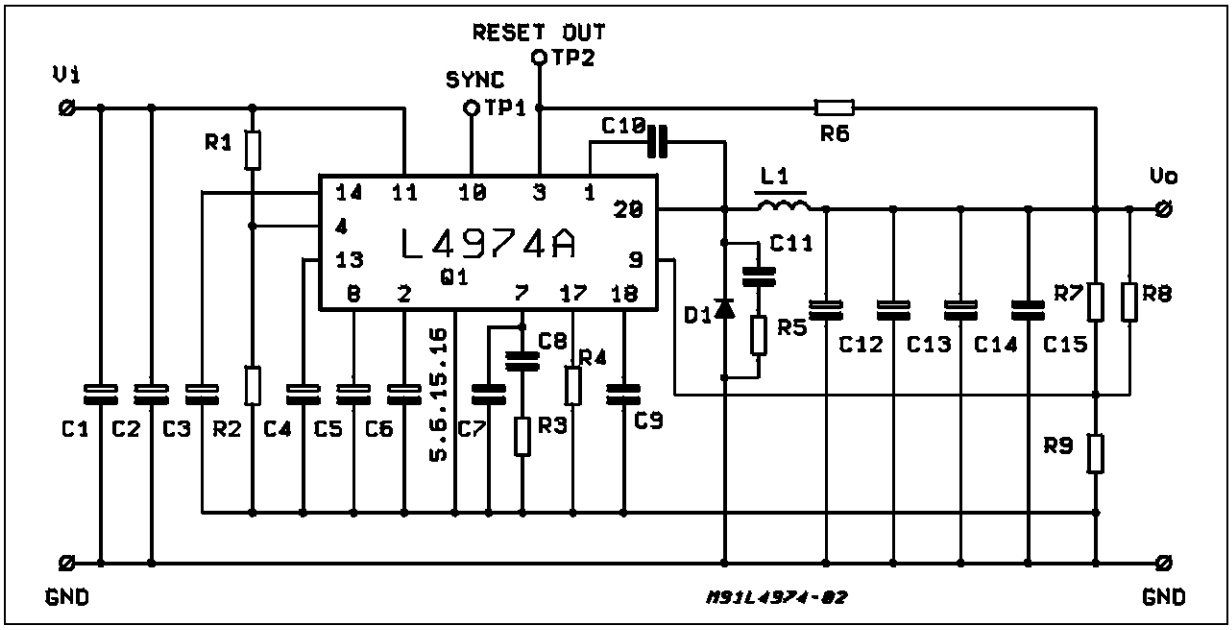
Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit	Fig.
V_{10}	Low Input Voltage	$V_i = 15V$ to 50V; $V_8 = 0$; S1 = B; S2 = B; S4 = B	–0.3		0.9	V	7A
V_{10}	High Input voltage	$V_8 = 0$; S1 = B; S2 = B; S4 = B	2.5		5.5	V	7A
$+I_{10L}$	Sync Input Current with Low Input Voltage	$V_{10} = V_{18} = 0.9V$; S4 = B; S1 = B; S2 = B			0.4	mA	7A
$+I_{10H}$	Input Current with High Input Voltage	$V_{10} = 2.5V$			1.5	mA	7A
V_{10}	Output Amplitude		4	5		V	–
t_W	Output Pulse Width	$V_{thr} = 2.5V$	0.3	0.5	0.8	µs	–

ELECTRICAL CHARACTERISTICS (continued)

RESET AND POWER FAIL FUNCTIONS

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit	Fig.
V_{9R}	Rising Thereshold Voltage (pin 9)	V_i = 15 to 50V V_4 = 5.3V	V_{ref} -130	V_{ref} -100	V_{ref} -80	V mV	7D
V_{9F}	Falling Thereshold Voltage (pin 9)	Vi = 15 to 50V V_4 = 5.3V	4.77	Vref -200	V_{ref} -160	V mV	7D
V_{2H}	Delay High Threshold Volt.	Vi = 15 to 50V V_4 = 5.3V $V_9 = V_{13}$	4.95	5.1	5.25	V	7D
V_{2L}	Delay Low Threshold Volt.	Vi = 15 to 50V V_4 = 4.7V $V_9 = V_{13}$	1	1.1	1.2	V	7D
I_{2SO}	Delay Source Current	V_4 = 5.3V; V_2 = 3V	30	60	80	µA	7D
I_{2SI}	Delay Source Sink Current	V_4 = 4.7V; V_2 = 3V	10			mA	7D
V_{3S}	Output Saturation Voltage	I_3 = 15mA; S1 = B V_4 = 4.7V			0.4	V	7D
I_3	Output Leak Current	V3 = 50V; S1 = A			100	µA	7D
V_{4R}	Rising Threshold Voltage	V9 = V_{13}	4.955	5.1	5.25	V	7D
V_{4H}	Hysteresis		0.4	0.5	0.6	V	7D
I_4	Input Bias Current			1	3	µA	7D

Figure 5 : Test and Evaluation Board Circuit.



TYPICAL PERFORMANCES (using evaluation board) :

n = 83% (V_i = 35V ; V_o = VREF ; I_o = 3.5A ; f_{SW} = 100KHz)

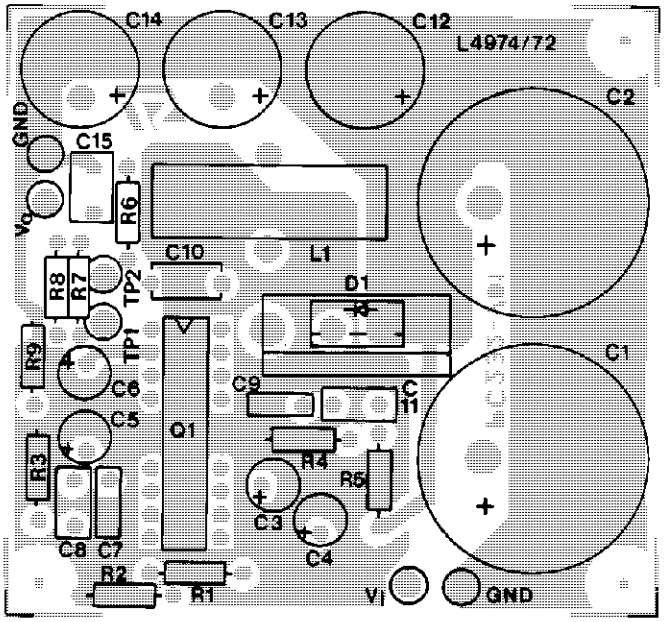
$V_{o\ RIPPLE}$ = 30mV (at 1A)

Line regulation = 12mV (V_i = 15 to 50V)

Load regulation = 8mV (I_o = 1 to 3.5A)

for component values Refer to the fig. 5 (Part list).

Figure 6a : Component Layout of fig.5 (1 : 1 scale). Evaluation Board Available



PART LIST

R_1 = 30KΩ
R_2 = 10KΩ
R_3 = 15KΩ
R_4 = 30KΩ
R_5 = 22Ω
R_6 = 4.7KΩ
R_7 = see table A
R_8 = OPTION
R_9 = 4.7KΩ

* C_1 = C_2 = 1000µF 63V EYF (ROE)
C_3 = C_4 = C_5 = C_6 = 2,2µF 50V
C_7 = 390pF Film
C_8 = 22nF MKT 1837 (ERO)
C_9 = 2.7nF KP 1830 (ERO)
C_{10} = 0.33µF Film
C_{11} = 1nF
** C_{12} = C_{13} = C_{14} = 100µF 40V EKR (ROE)
C_{15} = 1µF Film

D1 = SB 560 (OR EQUIVALENT)

L1 = 150µH
core 58310 MAGNETICS
45 TURNS 0.91mm (AWG 19)
COGEMA 949181

* 2 capacitors in parallel to increase input RMS current capability.
* * 3 capacitors in parallel to reduce total output ESR.

Table A

V_0	R_9	R_7
12V	4.7kΩ	6.2kW
15V	4.7kΩ	9.1kΩ
18V	4.7kΩ	12Ω
24V	4.7kΩ	18Ω

Table B
SUGGESTED BOOSTRAP CAPACITORS

Operating Frequency	Boostrap Cap.c10
f = 20KHz	≥680nF
f = 50KHz	≥470nF
f = 100KHz	≥330nF
f = 200KHz	≥220nF
f = 500KHz	≥100nF

Figure 6b: P.C. Board and Component Layout of the Circuit of Fig. 5. (1:1 scale)

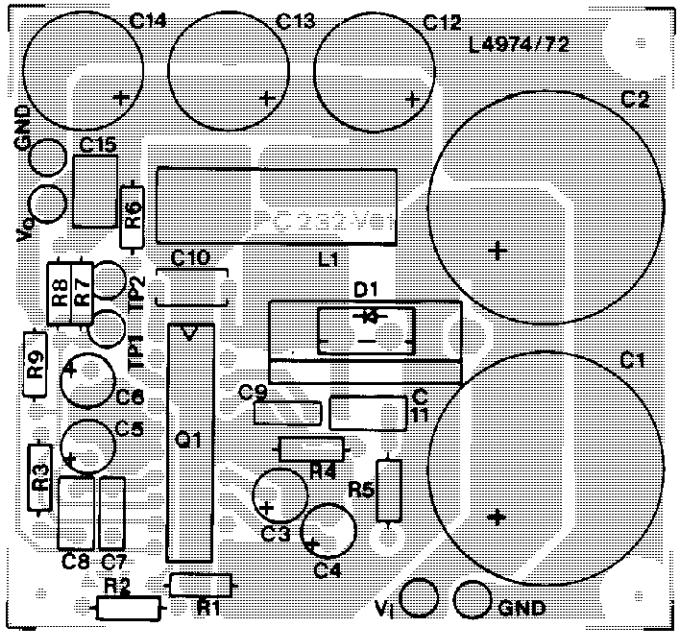


Figure 7 : DC Test Circuits.

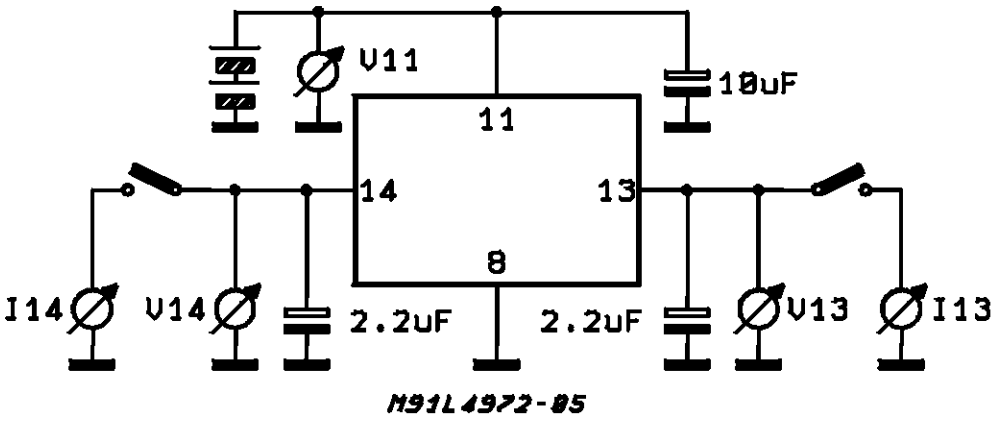


Figure 7A.

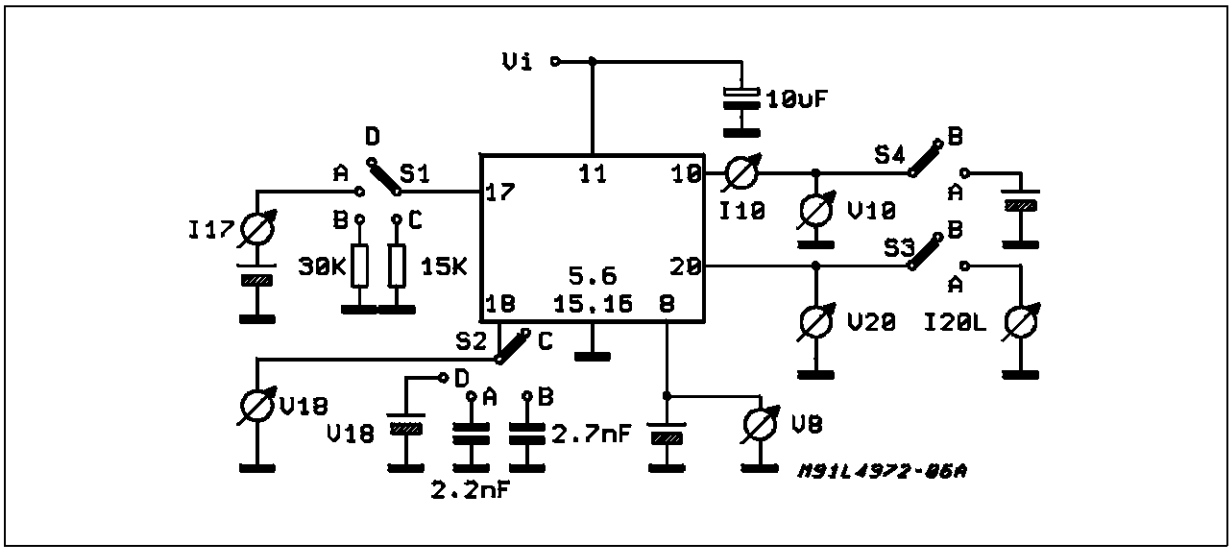


Figure 7B.

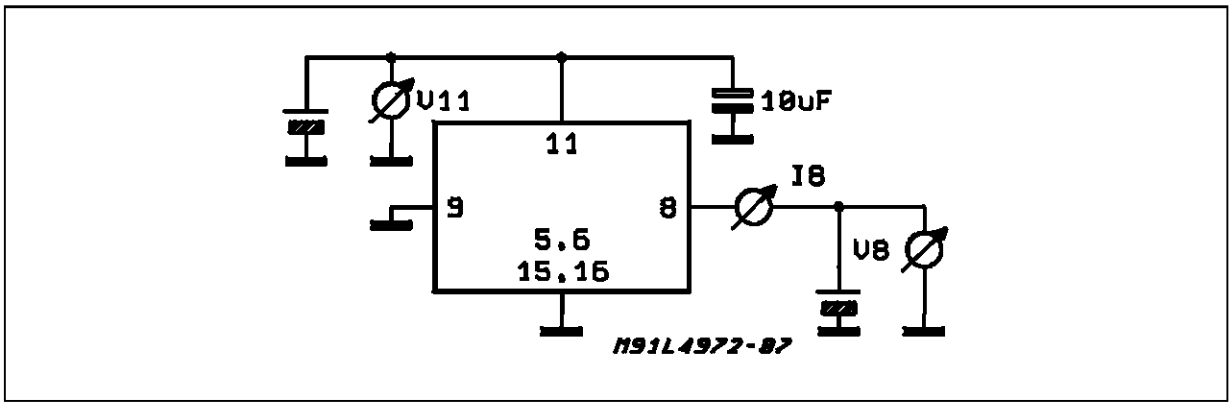


Figure 7C.

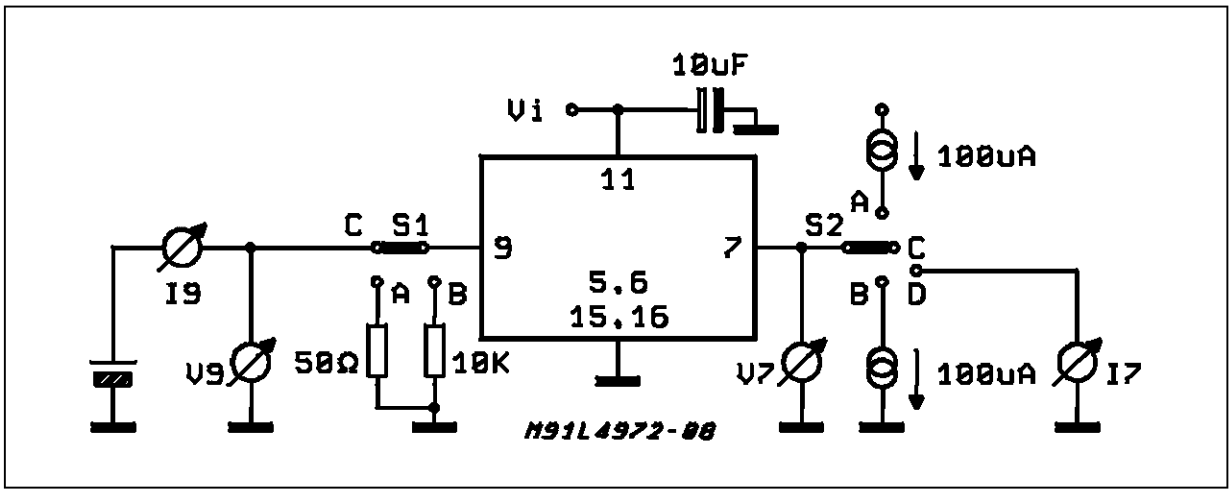


Figure 7D.

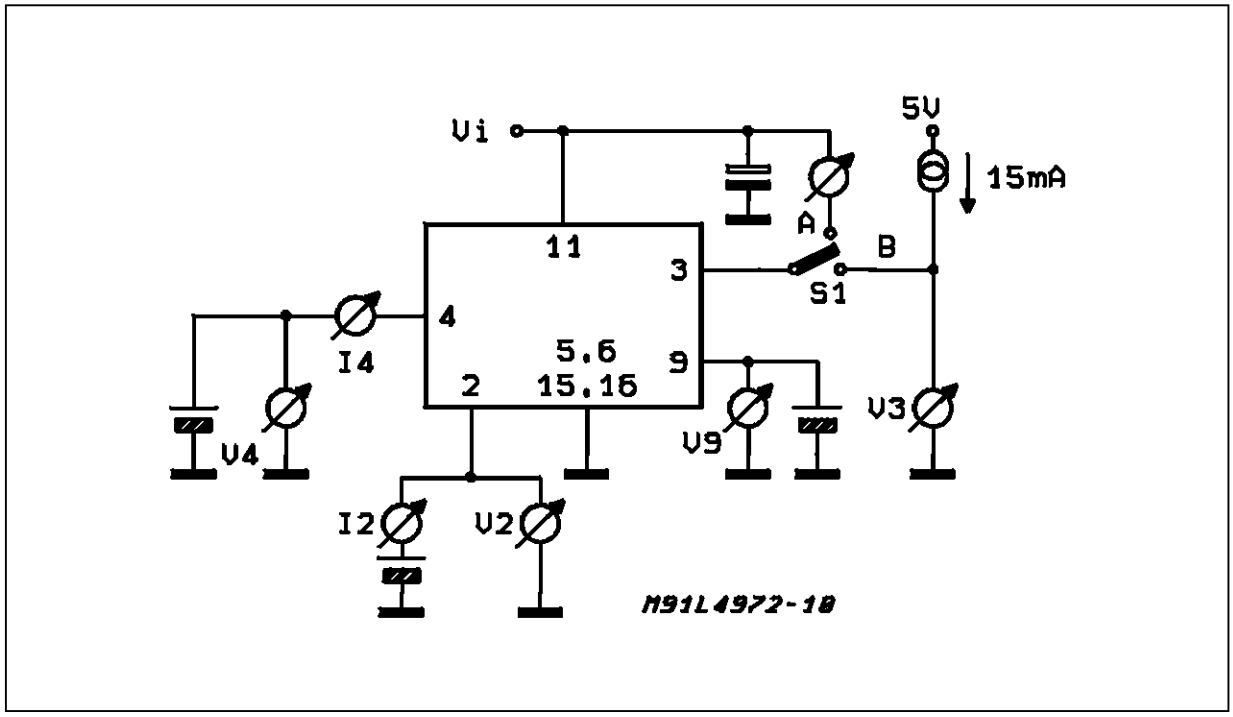


Figure 8 : Quiescent Drain Current vs. Supply Voltage (0% duty cycle - see fig. 7A).

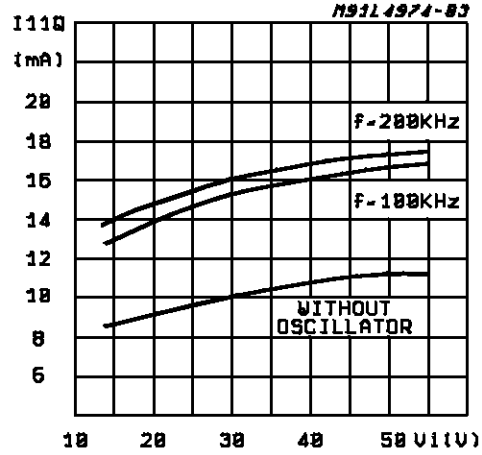


Figure 9 : Quiescent Drain Current vs. Junction Temperature (0% duty cycle).

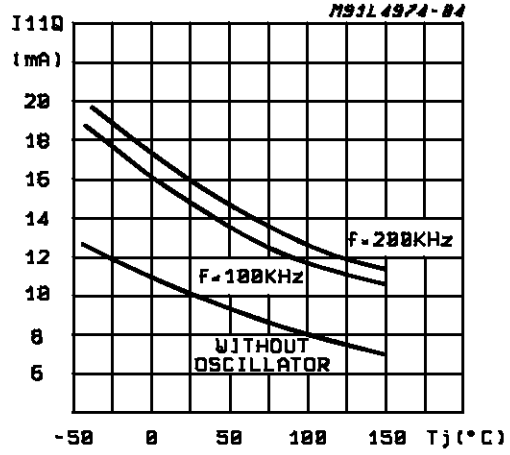


Figure 10 : Quiescent Drain Current vs. Duty Cycle.

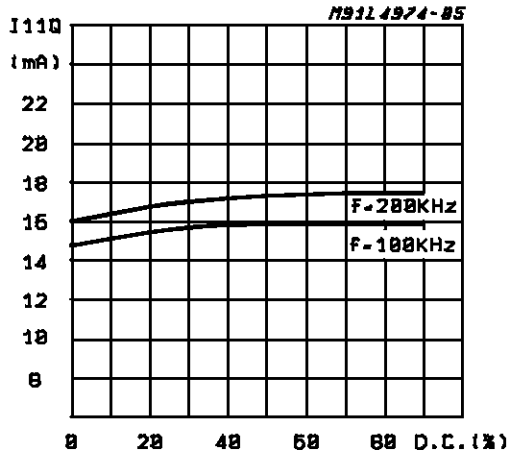


Figure 11 : Reference Voltage (pin 13) vs. Vi (see fig. 7).

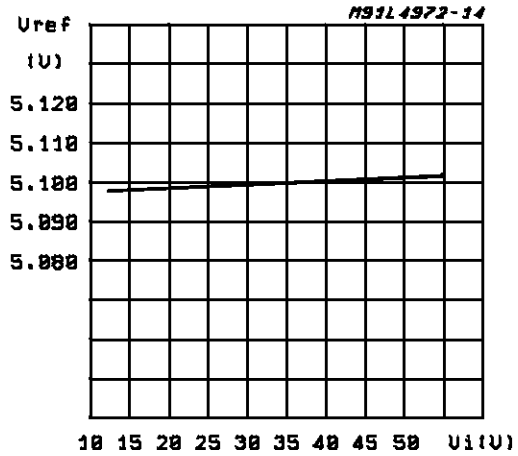


Figure 12 : Reference Voltage (pin 13) vs. Junction Temperature (see fig. 7).

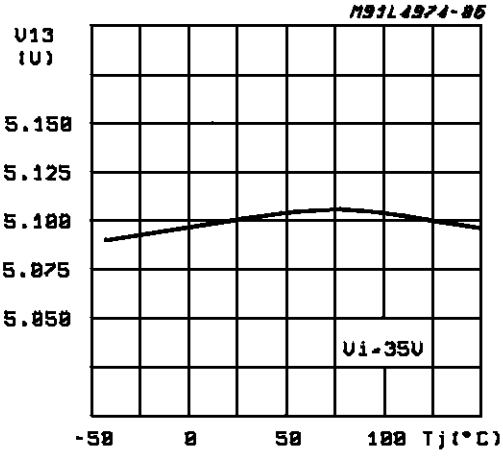


Figure 13 : Reference Voltage (pin 14) vs. Vi (see fig. 7).

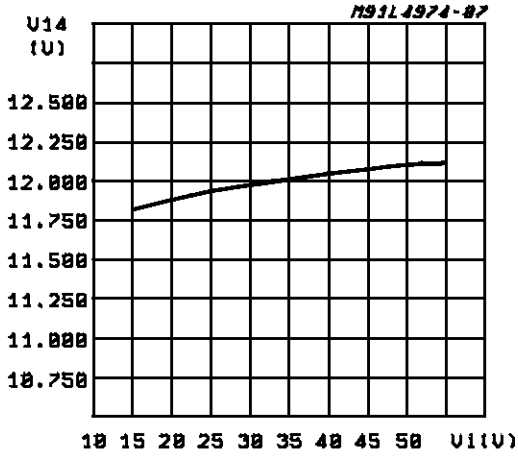


Figure 14 : Reference Voltage (pin 14) vs. Junction Temperature (see fig. 7).

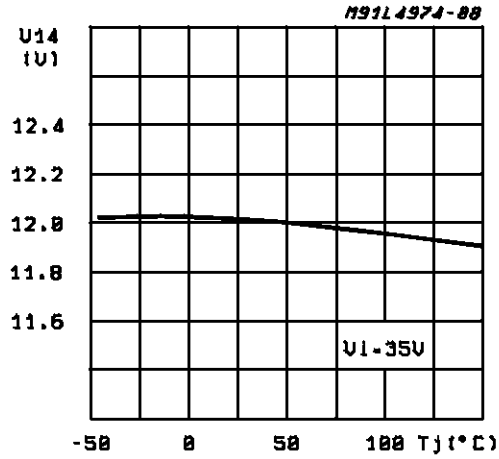


Figure 15 : Reference Voltage 5.1V (pin 13) Supply Voltage Ripple Rejection vs. Fre-

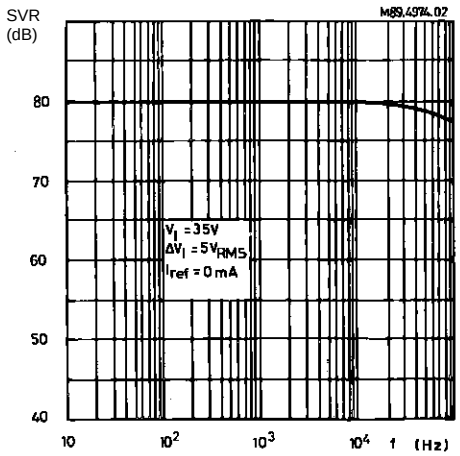


Figure 16 : Switching Frequency vs. Input Voltage (see fig. 5).

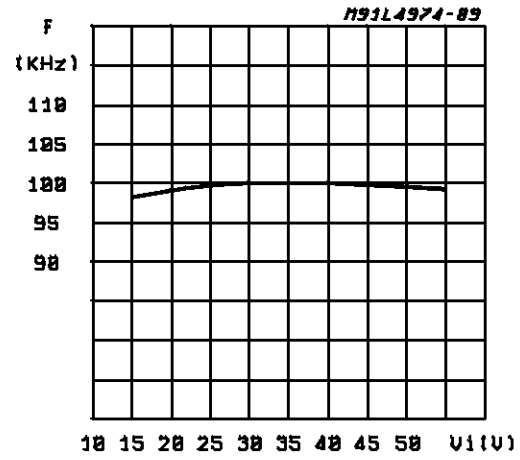


Figure 17 : Switching Frequency vs. Junction Temperature (see fig. 5).

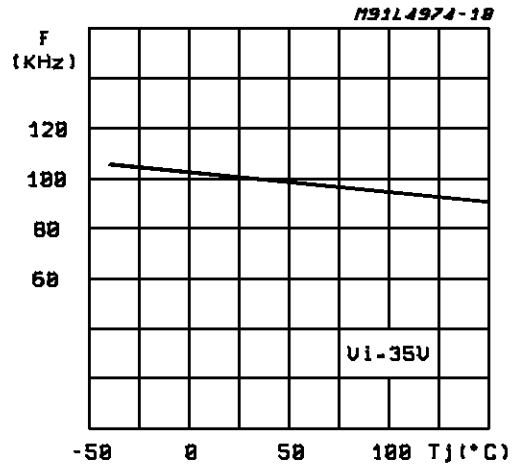


Figure 18 : Switching Frequency vs. R4 (see fig.5).

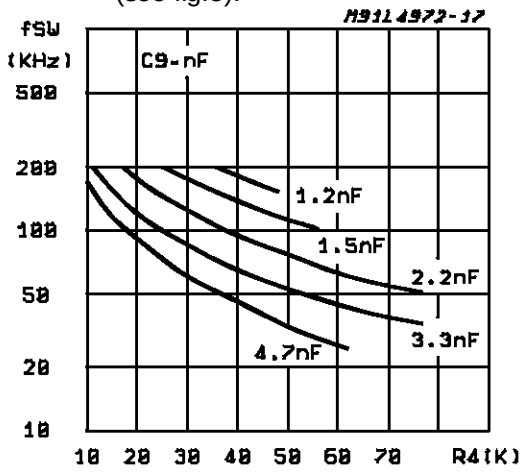


Figure 19 : Maximum Duty Cycle vs. Frequency.

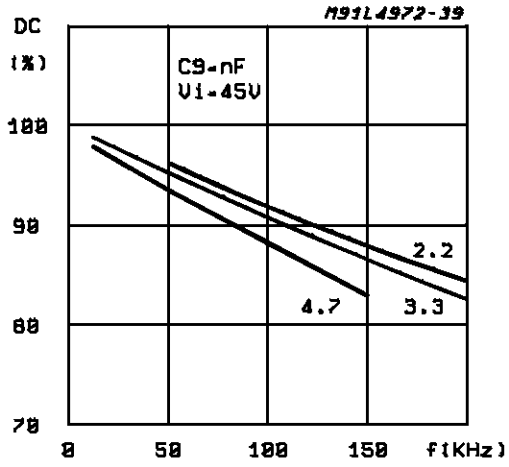


Figure 20 : Supply Voltage Ripple Rejection vs. Frequency (see fig. 5).

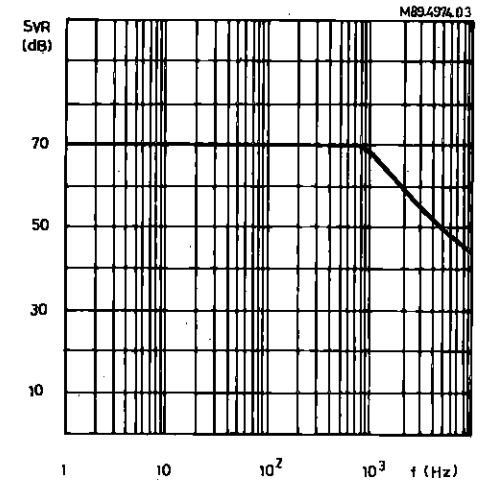


Figure 21 : Efficiency vs. Output Voltage.

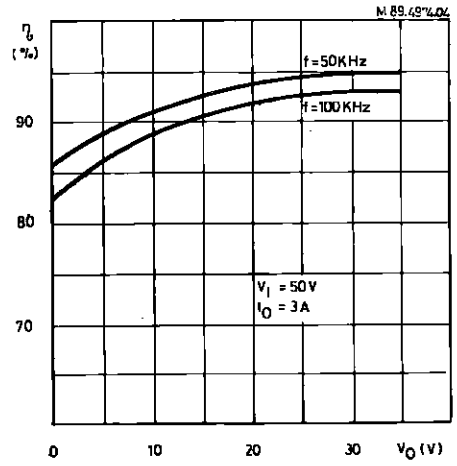


Figure 22 : Line Transient Response (see fig. 5).

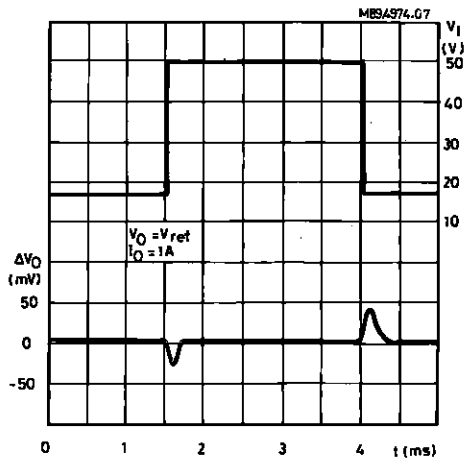


Figure 23 : Load Transient Response (see fig. 5).

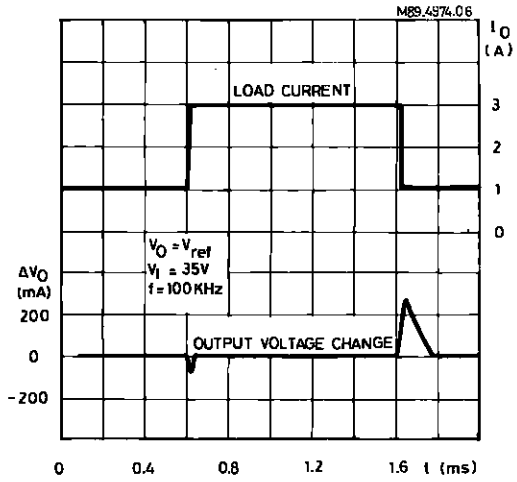


Figure 24 : Dropout Voltage between Pin 11 and Pin 20 vs. Current at Pin 20.

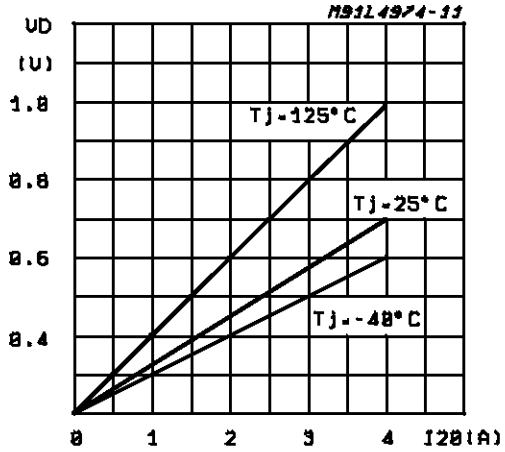


Figure 25 : .Dropout Voltage between Pin 11 and Pin 20 vs. Junction Temperature.

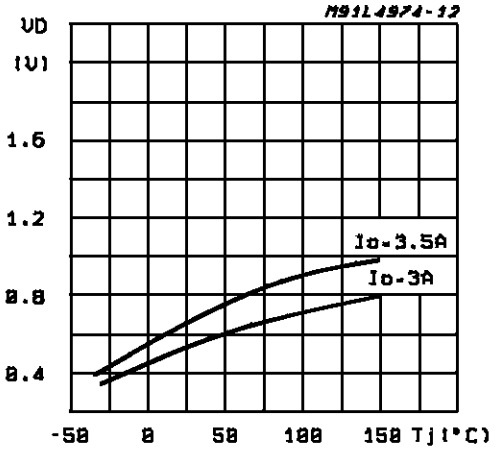


Figure 26 : Power Dissipation (device only) vs. Input Voltage.

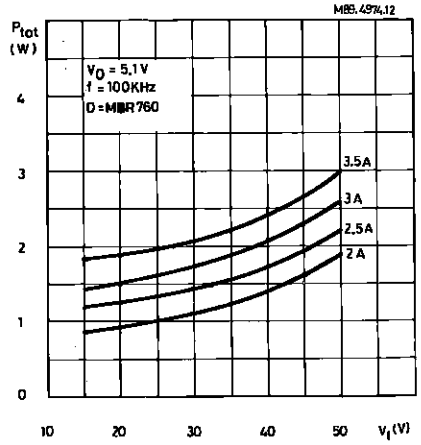


Figure 27 : Power Dissipation (device only) vs. Input Voltage.

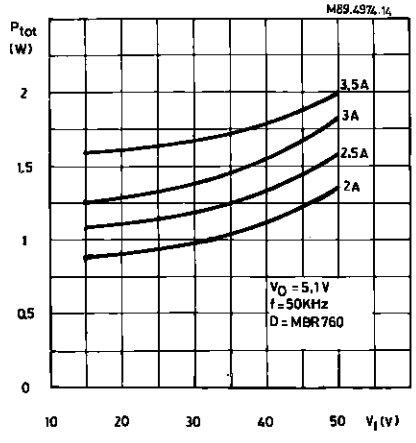


Figure 28 : Power Dissipation (device only) vs. Output Voltage.

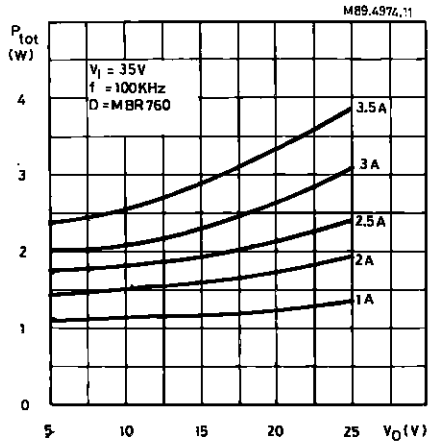


Figure 29 : Power Dissipation (device only) vs. Output Voltage.

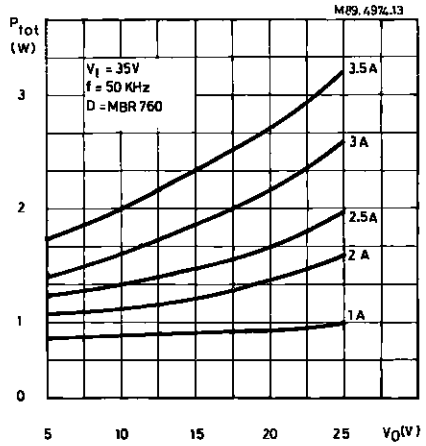


Figure 30 : Power Dissipation (device only) vs. Output Current.

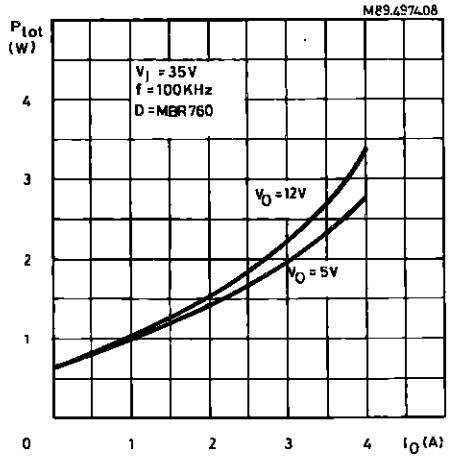


Figure 31 : Power Dissipation (device only) vs. Output Current.

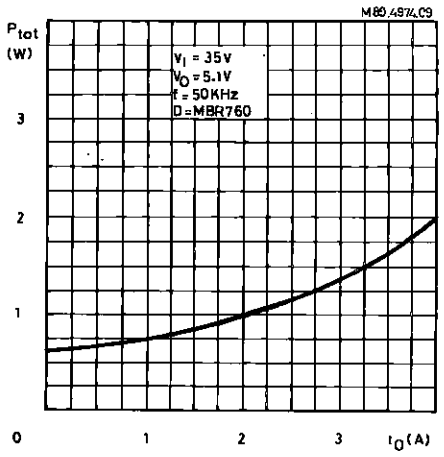


Figure 32 : Efficiency vs. Output Current.

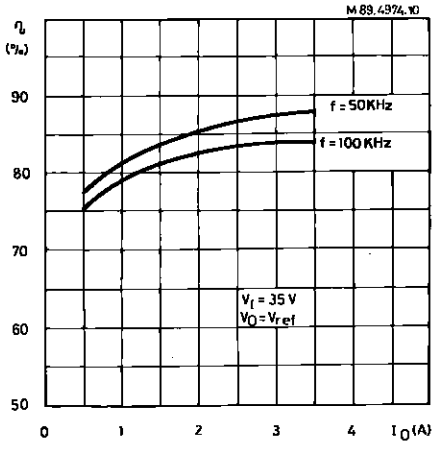


Figure 33 : Test PCB Thermal Characteristic.

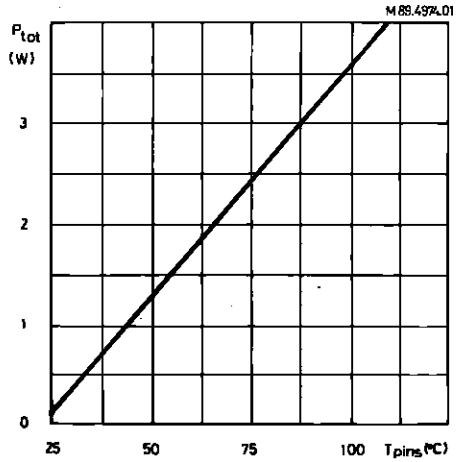


Figure 34 : Junction to Ambient Thermal Resistance vs. Area on Board Heatsink (DIP 16+2+2)

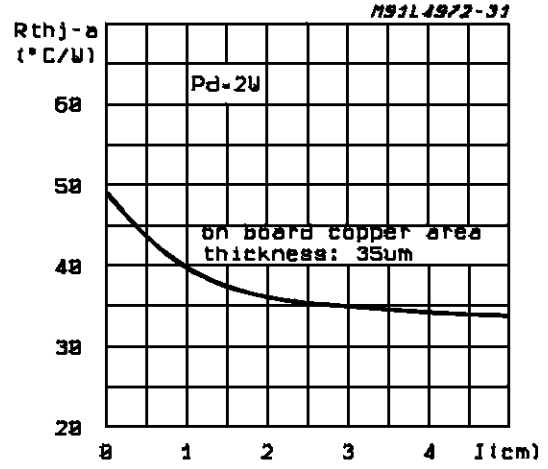


Figure 35: Maximum Allowable Power Dissipation vs. Ambient Temperature (Powerdip)

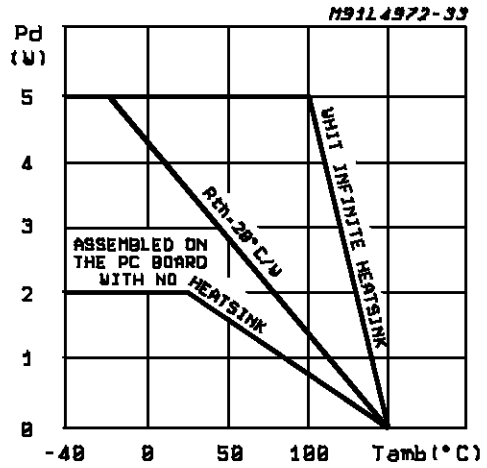


Figure 36: Open Loop Frequency and Phase of Error Amplifier (see fig. 7C).

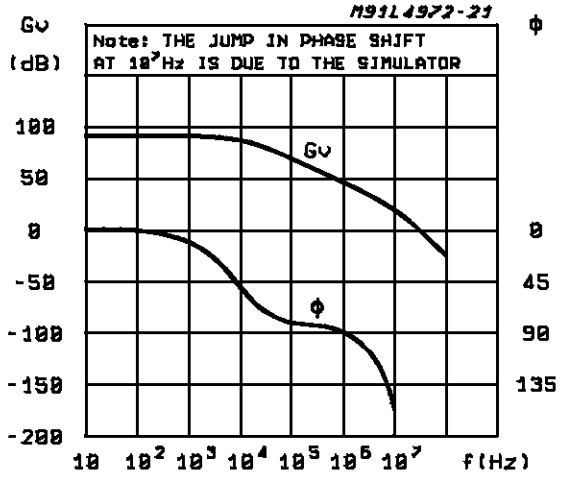


Figure 37 : 3.5A – 5.1V Low Cost Application Circuit.

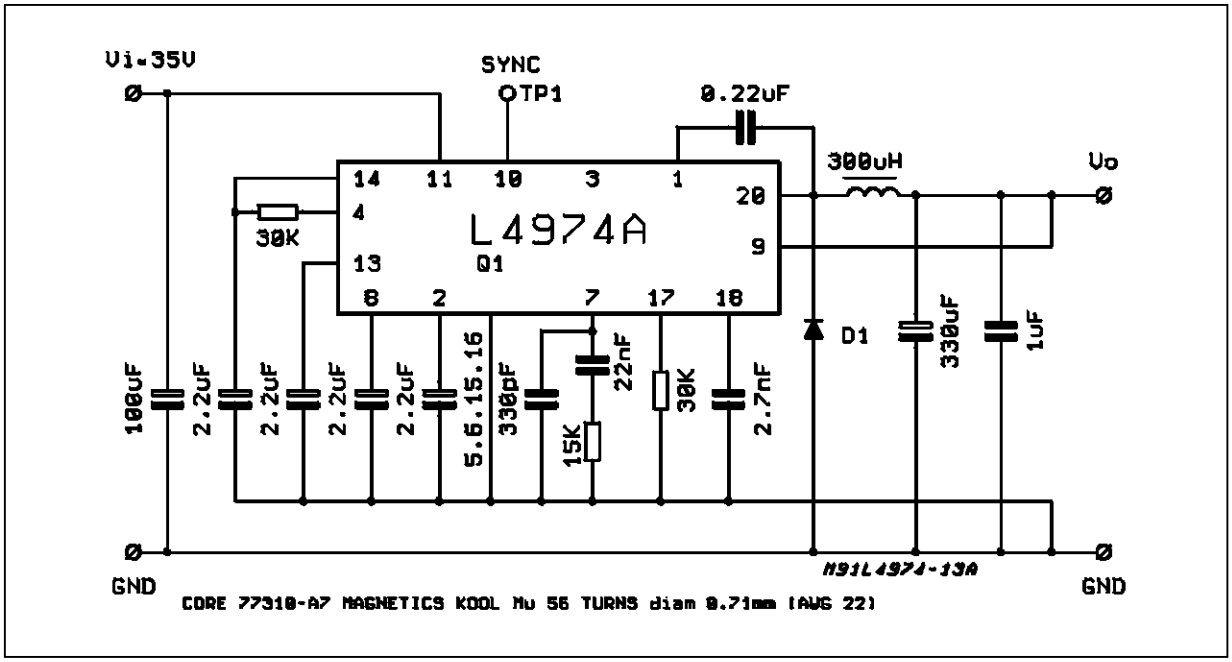


Figure 38 : A 5.1V/12V Multiple Supply. Note the Synchronization between the L4974A and L4970A.

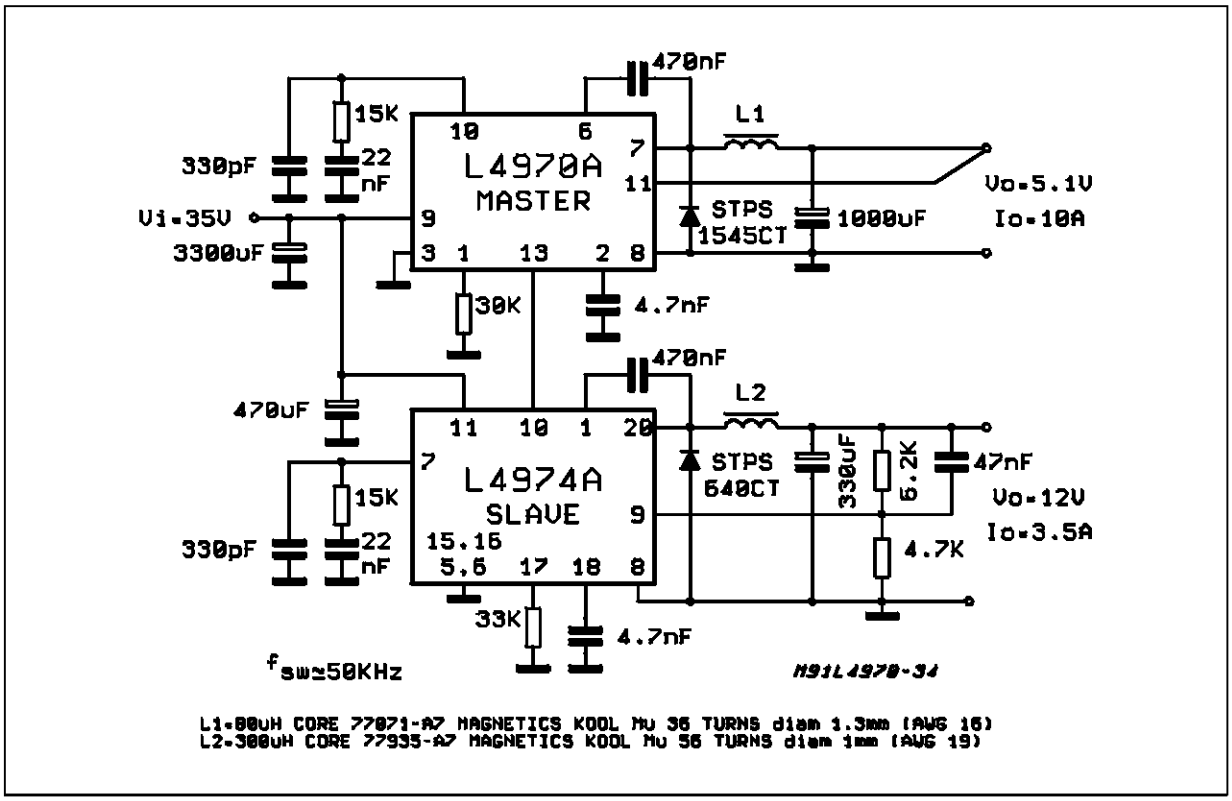


Figure 39 : L4974A's Sync. Example.

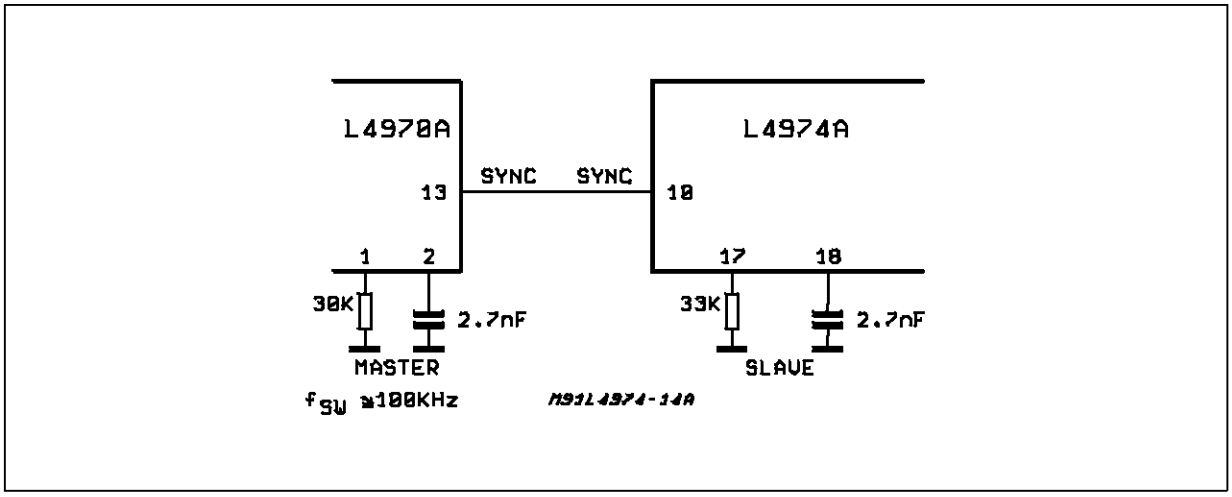
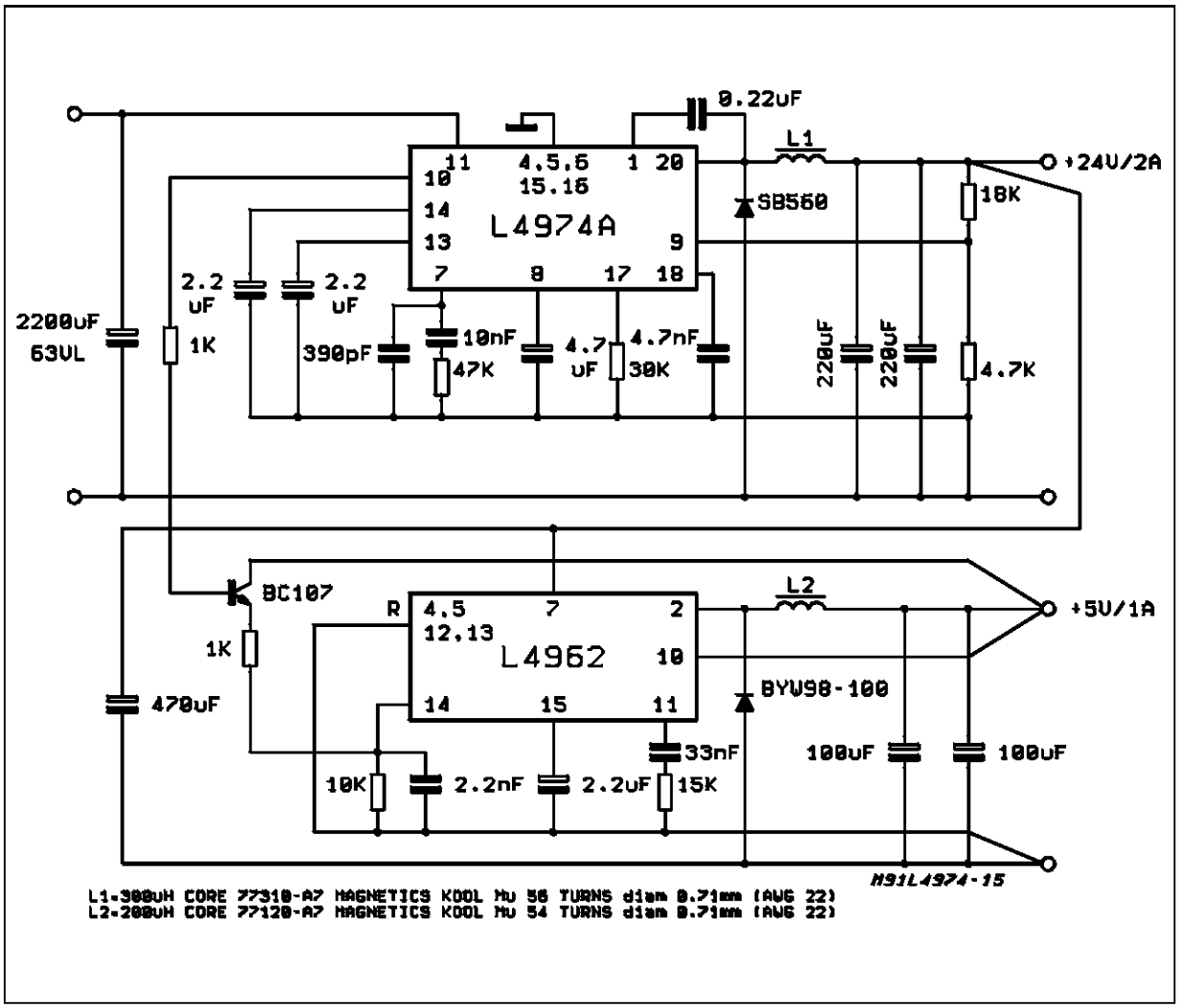
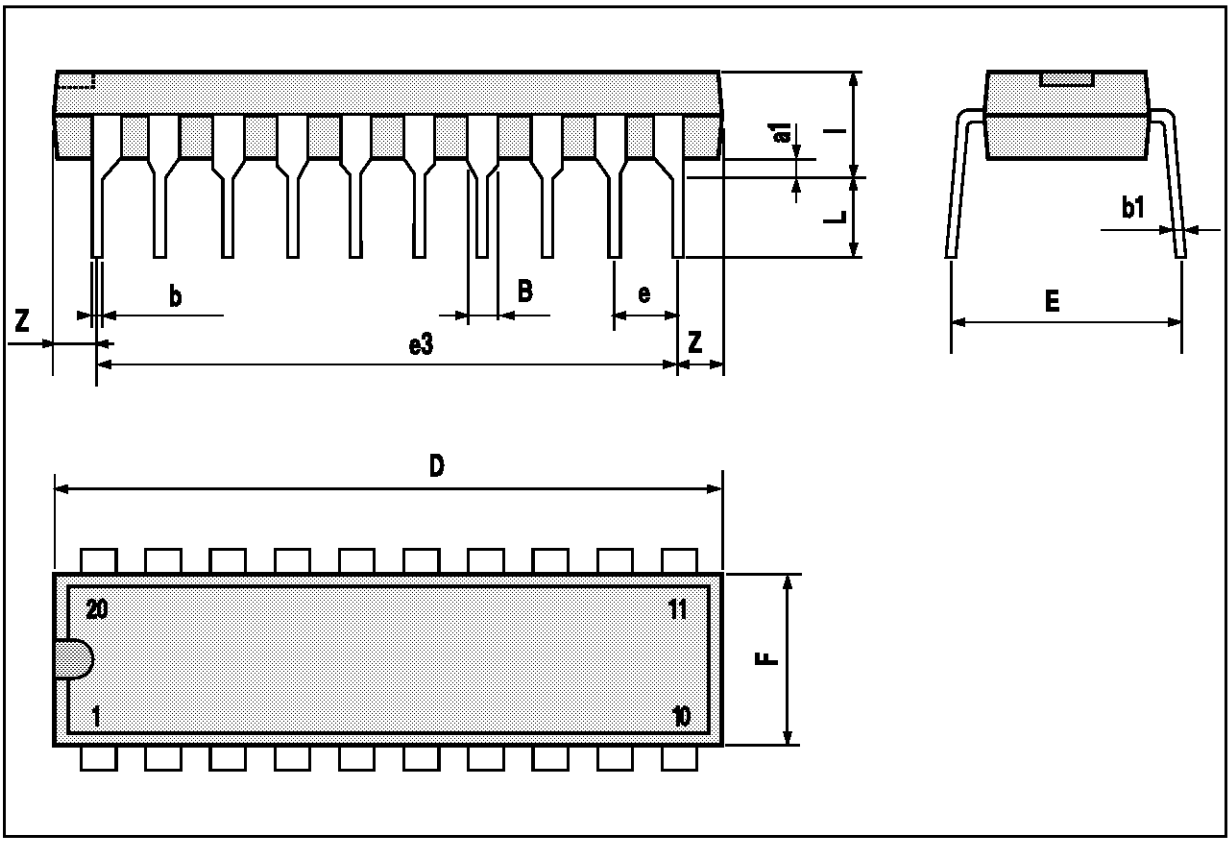


Figure 40: 1A/24V Multiple Supply. Note the synchronization between the L4974A and L4962



POWERDIP20 PACKAGE MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
a1	0.51			0.020		
B	0.85		1.40	0.033		0.055
b		0.50			0.020	
b1	0.38		0.50	0.015		0.020
D			24.80			0.976
E		8.80			0.346	
e		2.54			0.100	
e3		22.86			0.900	
F			7.10			0.280
I			5.10			0.201
L		3.30			0.130	
Z			1.27			0.050



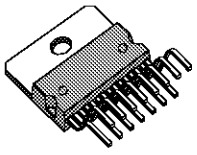
SGS-THOMSON MICROELECTRONICS

L4975A

5A SWITCHING REGULATOR

- 5A OUTPUT CURRENT
- 5.1V TO 40V OUTPUT VOLTAGE RANGE
- 0 TO 90% DUTY CYCLE RANGE
- INTERNAL FEED-FORWARD LINE REGULATION
- INTERNAL CURRENT LIMITING
- PRECISE 5.1V ± 2% ON CHIP REFERENCE
- RESET AND POWER FAIL FUNCTIONS
- SOFT START
- INPUT/OUTPUT SYNC PIN
- UNDER VOLTAGE LOCK OUT WITH HYSTERETIC TURN-ON
- PWM LATCH FOR SINGLE PULSE PER PERIOD
- VERY HIGH EFFICIENCY
- SWITCHING FREQUENCY UP TO 500KHz
- THERMAL SHUTDOWN
- CONTINUOUS MODE OPERATION

MULTIPOWER BCD TECHNOLOGY



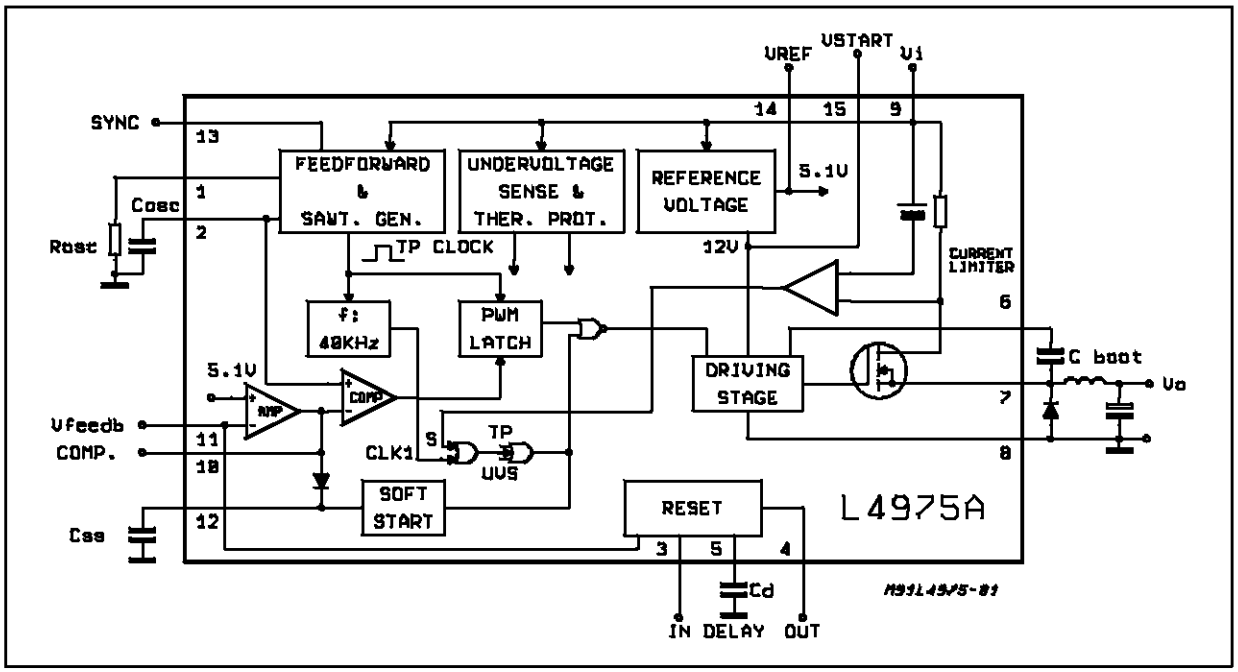
Multiwatt15V
ORDERING NUMBER: L4975A

DESCRIPTION

The L4975A is a stepdown monolithic power switching regulator delivering 5A at a voltage variable from 5.1 to 40V.

Realized with BCD mixed technology, the device uses a DMOS output transistor to obtain very high efficiency and very fast switching times. Features of the L4975A include reset and power fail for microprocessors, feed forward line regulation, soft start, limiting current and thermal protection. The device is mounted in a 15-lead multiwatt plastic power package and requires few external components. Efficient operation at switching frequencies up to 500KHz allows reduction in the size and cost of external filter components.

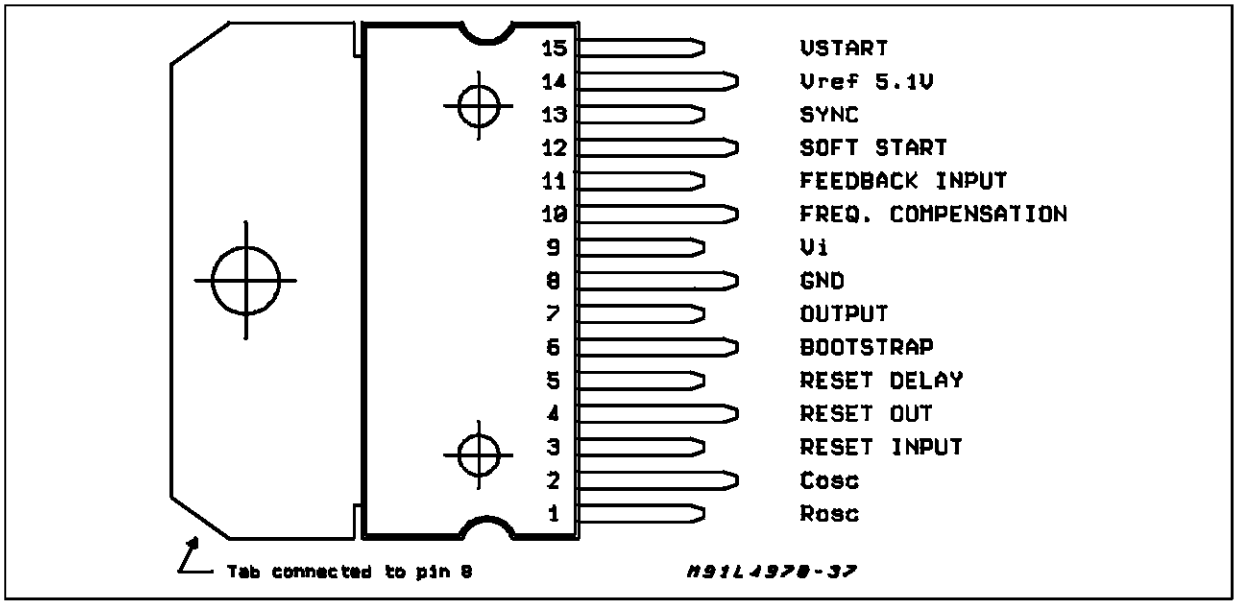
BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_9	Input Voltage	55	V
V_9	Input Operating Voltage	50	V
V_7	Output DC Voltage Output Peak Voltage at t = 0.1µs f = 200KHz	-1 -7	V V
I_7	Maximum Output Current	Internally Limited	
V_6	Bootstrap Voltage Bootstrap Operating Voltage	65 V_9 + 15	V V
V_3, V_{12}	Input Voltage at Pins 3, 12	12	V
V_4	Reset Output Voltage	50	V
I_4	Reset Output Sink Current	50	mA
V_5, V_{10}, V_{11}, V_{13}	Input Voltage at Pin 5, 10, 11, 13	7	V
I_5	Reset Delay Sink Current	30	mA
I_{10}	Error Amplifier Output Sink Current	1	A
I_{12}	Soft Start Sink Current	30	mA
P_{tot}	Total Power Dissipation at T_{case} < 120°C	30	W
T_j, T_{stg}	Junction and Storage Temperature	-40 to 150	°C

PIN CONNECTION (Top view)



THERMAL DATA

Symbol	Parameter		Value	Unit
$R_{th\ j\text{-}case}$	Thermal Resistance Junction-case	max	1	°C/W
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient	max	35	°C/W

PIN FUNCTIONS

N°	Name	Function
1	OSCILLATOR	R_{osc}. External resistor connected to ground determines the constant charging current of C_{osc}.
2	OSCILLATOR	C_{osc}. External capacitor connected to ground determines (with R_{osc}) the switching frequency.
3	RESET INPUT	Input of Power Fail Circuit. The threshold is 5.1V. It may be connected via a divider to the input for power fail function. It must be connected to the pin 14 an external 30KΩ resistor when power fail signal not required.
4	RESET OUT	Open Collector Reset/power Fail Signal Output. This output is high when the supply and the output voltages are safe.
5	RESET DELAY	A C_d capacitor connected between this terminal and ground determines the reset signal delay time.
6	BOOTSTRAP	A C_{boot} capacitor connected between this terminal and the output allows to drive properly the internal D-MOS transistor.
7	OUTPUT	Regulator Output.
8	GROUND	Common Ground Terminal
9	SUPPLY VOLTAGE	Unregulated Input Voltage.
10	FREQUENCY COMPENSATION	A series RC network connected between this terminal and ground determines the regulation loop gain characteristics.
11	FEEDBACK INPUT	The Feedback Terminal of the Regulation Loop. The output is connected directly to this terminal for 5.1V operation; It is connected via a divider for higher voltages.
12	SOFT START	Soft Start Time Constant. A capacitor is connected between thi sterminal and ground to define the soft start time constant.
13	SYNC INPUT	Multiple L4975A are synchronized by connecting pin 13 inputs together or via an external syncr. pulse.
14	V_{ref}	5.1V V_{ref} Device Reference Voltage.
15	V_{start}	Internal Start-up Circuit to Drive the Power Stage.

CIRCUIT OPERATION (refer to the block diagram)

The L4975A is a 5A monolithic stepdown switching regulator working in continuous mode realized in the new BCD Technology. This technology allows the integration of isolated vertical DMOS power transistors plus mixed CMOS/Bipolar transistors.

The device can deliver 5A at an output voltage adjustable from 5.1V to 40V, and contains diagnostic and control functions that make it particularly suitable for microprocessor based systems.

BLOCK DIAGRAM

The block diagram shows the DMOS power transistor and the PWM control loop. Integrated functions include a reference voltage trimmed to 5.1V ± 2%, soft start, undervoltage lockout, oscillator with feedforward control, pulse by pulse current limit, thermal shutdown and finally the reset and power fail circuit. The reset and power fail circuit provides an output signal for a microprocessor indicating the status of the system.

Device turn on is around 11V with a typical 1V hysteresis, this threshold provides a correct voltage for the driving stage of the DMOS gate and the hysteresis prevents instabilities.

An external bootstrap capacitor charged to 12V by an internal voltage reference is needed to provide correct gate drive to the power DMOS. The driving circuit is able to source and sink peak currents of around 0.5A to the gate of the DMOS transistor. A typical switching time of the current in the DMOS transistor is 50ns. Due to the fast commutation switching frequencies up to 500kHz are possible.

The PWM control loop consists of a sawtooth oscillator, error amplifier, comparator, latch and the output stage. An error signal is produced by comparing the output voltage with the precise 5.1V ± 2% on chip reference. This error signal is then compared with the sawtooth oscillator, in order to generate a fixed frequency pulse width modulated drive for the output stage. A PWM latch is included to eliminate multiple pulsing within a period even in noisy environments. The gain and

Figure 1: Feedforward Waveform

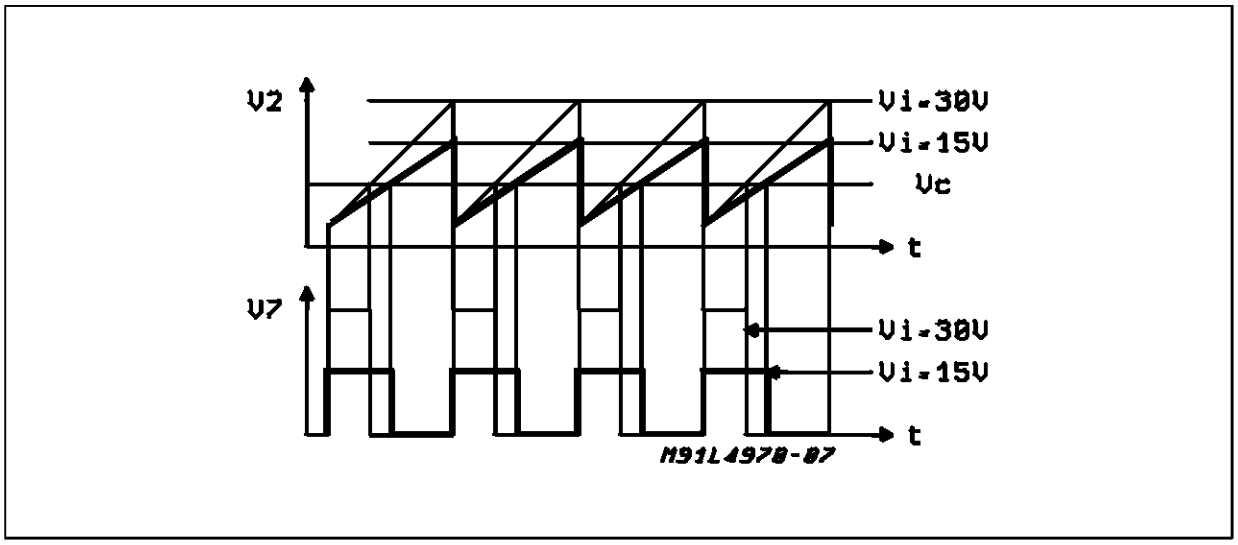


Figure 2: Soft Start Function

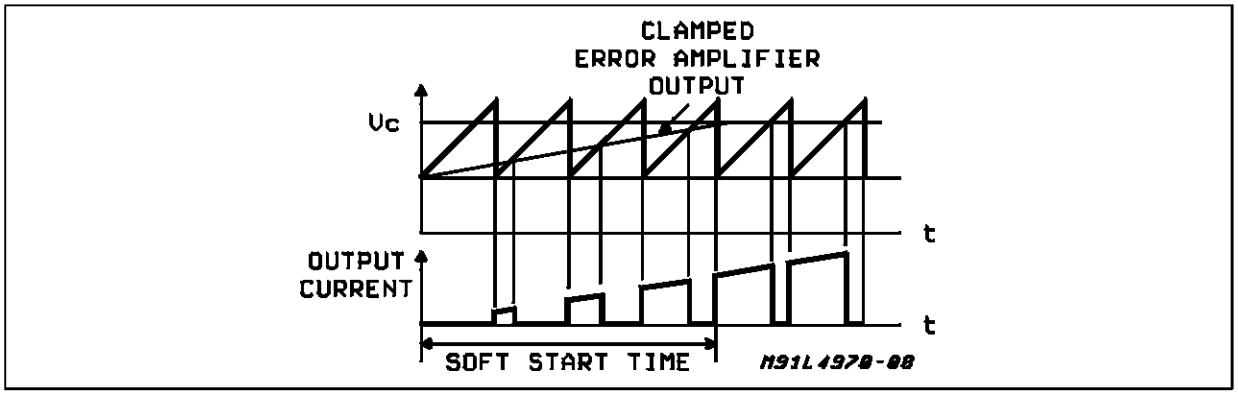
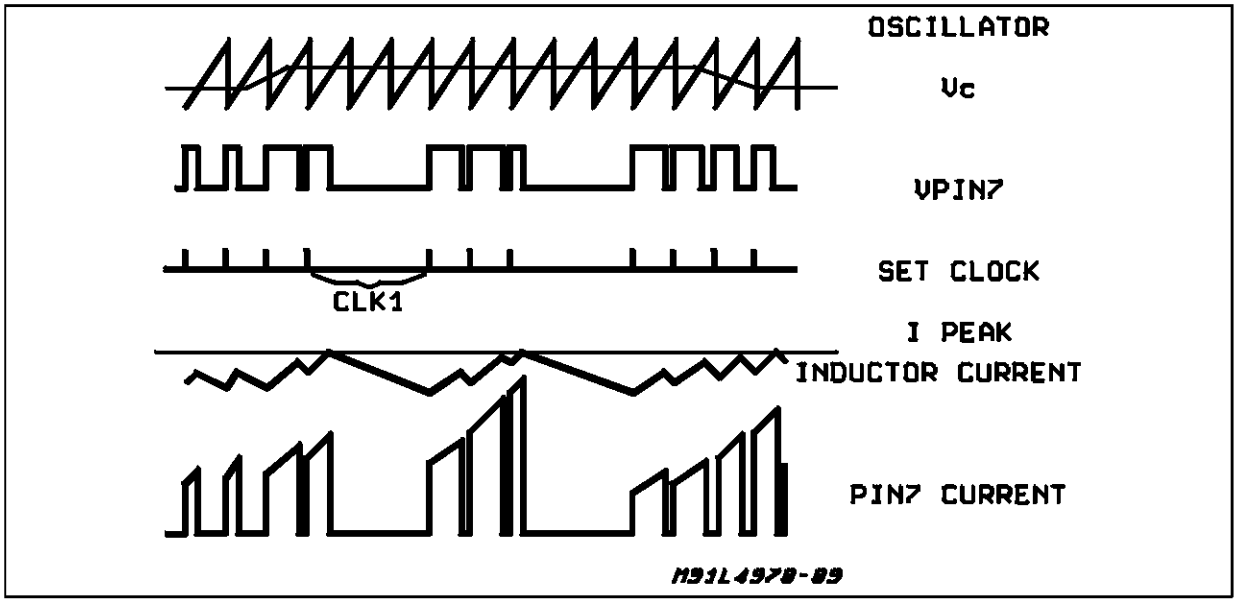


Figure 3: Limiting Current Function



stability of the loop can be adjusted by an external RC network connected to the output of the error amplifier. A voltage feedforward control has been added to the oscillator, this maintains superior line regulation over a wide input voltage range. Closing the loop directly gives an output voltage of 5.1V, higher voltages are obtained by inserting a voltage divider.

At turn on output overcurrents are prevented by the soft start function (fig. 2). The error amplifier is initially clamped by an external capacitor Css and allowed to rise linearly under the charge of an internal constant current source.

Output overload protection is provided by a current limit circuit (fig. 3). The load current is sensed by an internal metal resistor connected to a comparator. When the load current exceeds a preset threshold the output of the comparator sets a flip flop which turns off the power DMOS. The next clock pulse, from an internal 40kHz oscillator will reset the flip flop and the power DMOS will again conduct. This current protection method, ensures a constant current output when the system is overloaded or short circuited and limits the switching frequency, in this condition, to 40kHz.

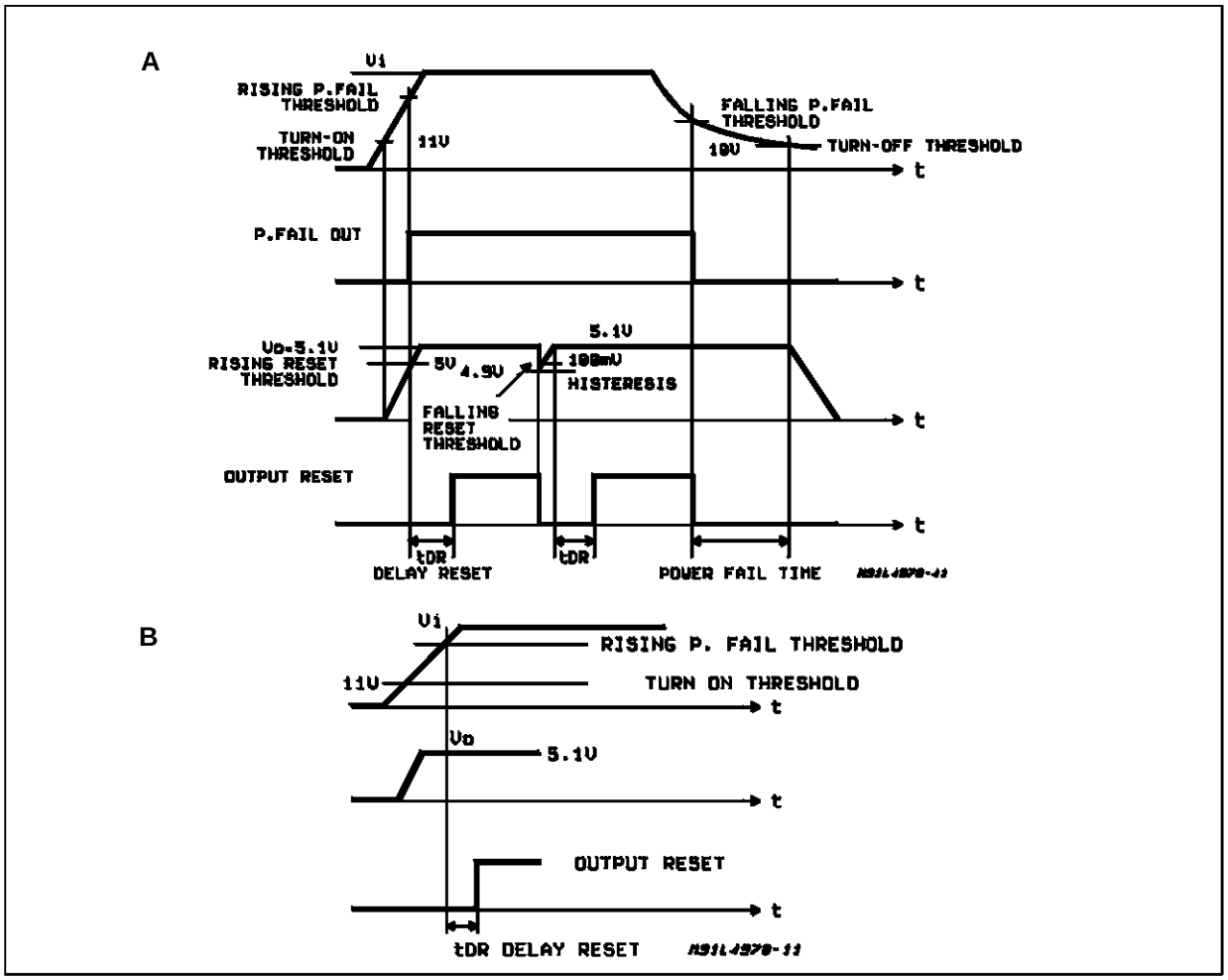
The Reset and Power fail circuitry (fig 4) generates an output signal when the supply voltage exceeds a threshold programmed by an external voltage divider. The reset signal, is generated with a delay time programmed by an external capacitor on the delay pin. When the supply voltage falls below the threshold or the output voltage goes below 5V the reset output goes low immediately. The reset output is an open collector-drain.

Fig 4A shows the case when the supply voltage is higher than the threshold, but the output voltage is not yet 5V.

Fig 4B shows the case when the output is 5.1V but the supply voltage is not yet higher than the fixed threshold.

The thermal protection disables circuit operation when the junction temperature reaches about 150°C and has an hysterysis to prevent unstable conditions.

Figure 4: Reset and Power Fail Functions.



ELECTRICAL CHARACTERISTICS (Refer to the test circuit, T_j = 25°C, V_i = 35V, R_4 = 16KΩ, C_9 = 2.2nF, f_{SW} = 200KHz typ, unless otherwise specified)

DYNAMIC CHARACTERISTICS

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit	Fig.
V_i	input Voltage Range (pin 9)	V_o = V_{ref} to 40V I_o = 5A	15		50	V	5
V_o	Output Votage	V_i = 15V to 50V I_o = 3A; V_o = V_{ref}	5	5.1	5.2	V	5
ΔV_o	Line Regulation	V_i = 15V to 50V I_o = 2A; V_o = V_{ref}		12	30	mV	5
ΔV_o	Load Regulation	V_o = V_{ref} I_o = 2A to 4A I_o = 1A to 5A		 10 20	 30 50	 mV mV	5
V_d	Dropout Voltage Between Pin 9 and 7	I_o = 3A I_o = 5A		0.4 0.55	0.6 0.8	V V	5
I_{7L}	Max. Limiting Current	V_i = 15 to 50V V_o = V_{ref} to 40V	5.5	6.5	7.5	A	5
η	Efficiency	I_o = 3A V_o = V_{ref} V_o = 12V	70	 75 80		 % %	5
		I_o = 5A V_o = V_{ref} V_o = 12V	80	 85 92		 % %	5
SVR	Supply Voltage Ripple Reject.	V_i = 2VRMS; I_o = 3A f = 100Hz; V_o = V_{ref}	56	60		dB	5
f	Switching Frequency		180	200	220	KHz	5
$\frac{\Delta f}{\Delta V_i}$	Voltage Stability of Swiching Frequency	V_i = 15V to 45V		2	6	%	5
$\frac{\Delta f}{T_j}$	Temperature Stability of Swiching Frequency	T_j = 0 to 125°C		1		%	5
f_{max}	Maximum Operating Switching Frequency	V_o = V_{ref}; R_4 = 10KΩ I_o = 5A; C_9 = 1nF	500			KHz	5

V_{ref} SECTION (pin 14)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit	Fig.
V_{14}	Reference Voltage		5	5.1	5.2	V	7
ΔV_{14}	Line Regulation	V_i = 15V to 50V		10	25	mV	7
ΔV_{14}	Load Regulation	I_{14} = 0 to 1mA		20	40	mV	7
$\frac{\Delta V_{14}}{\Delta T}$	Average Temperature Coefficient Reference Voltage	T_j = 0°C to 125°C		0.4		mV/°C	7
$I_{14\ short}$	Short Circuit Current Limit	V_{14} = 0		70		mA	7

V_{START} SECTION (pin 15)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit	Fig.
V_{15}	Reference Voltage		11.4	12	12.6	V	7
ΔV_{15}	Line Regulation	V_i = 15 to 50V		0.6	1.4	V	7
ΔV_{15}	Load Regulation	I_{15} = 0 to 1mA		50	200	mV	7
$I_{15\ short}$	Short Circuit Current Limit	V_{15} = 0V		80		mA	7

ELECTRICAL CHARACTERISTICS (continued)

DC CHARACTERISTICS

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit	Fig.
V_{9on}	Turn-on Threshold		10	11	12	V	7A
$V_{9\ Hyst}$	Turn-off Hysteresys			1		V	7A
I_{9Q}	Quiescent Current	V_{12} = 0; S1 = D		13	19	mA	7A
I_{9OQ}	Operating Supply Current	V_{12} = 0; S1 = C; S2 = B		16	23	mA	7A
I_{7L}	Out Leak Current	V_i = 55V; S3 = A; V_{12} = 0			2	mA	7A

SOFT START

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit	Fig.
I_{12}	Soft Start Source Current	V_{12} = 3V; V_{11} = 0V	70	100	130	µA	7B
V_{12}	Output Saturation Voltage	I_{12} = 20mA; V_9 = 10V			1	V	7B
		I_{12} = 200µA; V_9 = 10V			0.7	V	7B

ERROR AMPLIFIER

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit	Fig.
V_{10H}	High Level Out Voltage	I_{10} = -100µA; S1 = C V_{11} = 4.7V	6			V	7C
V_{10L}	Low Level Out Voltage	I_{10} = +100µA; S1 = C V_{11} = 5.3V;			1.2	V	7C
I_{10H}	Source Output Current	V_{10} = 1V; S1 = E V_{11} = 4.7V	100	150		µA	7C
I_{10L}	Sink Output Current	V_{10} = 6V; S1 = D V_{11} = 5.3V	100	150		µA	7C
I_{11}	Input Bias Current	R_S = 10KΩ		0.4	3	µA	–
G_V	DC Open Loop Gain	V_{VCM} = 4V; R_S = 10Ω	60			dB	–
SVR	Supply Voltage Rejection	15 < V_i < 50V; R_S = 10Ω	60	80		dB	–
V_{OS}	Input Offset Voltage	R_S = 50Ω		2	10	mV	–

RAMP GENERATOR (pin 2)

Symbol	Parameter	Test Condition		Min.	Typ.	Max.	Unit	Fig.
V_2	Ramp Valley	S1 = C; S2 = B		1.2	1.5		V	7A
V_2	Ramp Peak	S1 = C	V_i = 15V		2.5		V	7A
		S2 = B	V_i = 45V		5.5		V	7A
I_2	Min. Ramp Current	S1 = A; I_1 = 100µA			270	300	µA	7A
I_2	Max. Ramp Current	S1 = A; I1 = 1mA		2.4	2.7		mA	7A

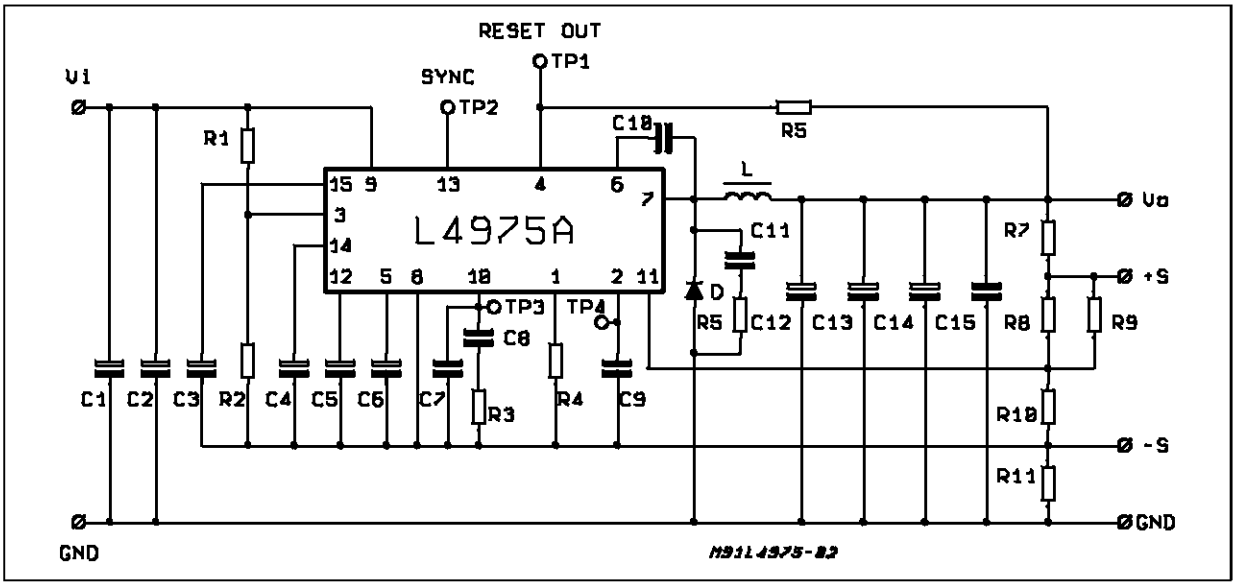
SYNC FUNCTION (pin 13)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit	Fig.
V_{13}	Low Input Voltage	V_i = 15V to 50V; V_{12} = 0; S1 = C; S2 = B; S4 = B	–0.3		0.9	V	7A
V_{13}	High Input voltage	V_{12} = 0; S1 = C; S2 = B; S4 = B	3.5		5.5	V	7A
I_{13L}	Sync Input Current with Low Input Voltage	V_2 = V_{13} = 0.9V; S4 = A; S1 = C; S2 = B			0.4	mA	7A
I_{13H}	Input Current with High Input Voltage	V_{13} = 3.5V; S4 = A; S1 = C; S2 = B			1.5	mA	7A
V_{13}	Output Amplitude		4	5		V	–
t_W	Output Pulse Width	V_{thr} = 2.5V	0.3	0.5	0.8	µs	–

ELECTRICAL CHARACTERISTICS (continued)
RESET AND POWER FAIL FUNCTIONS

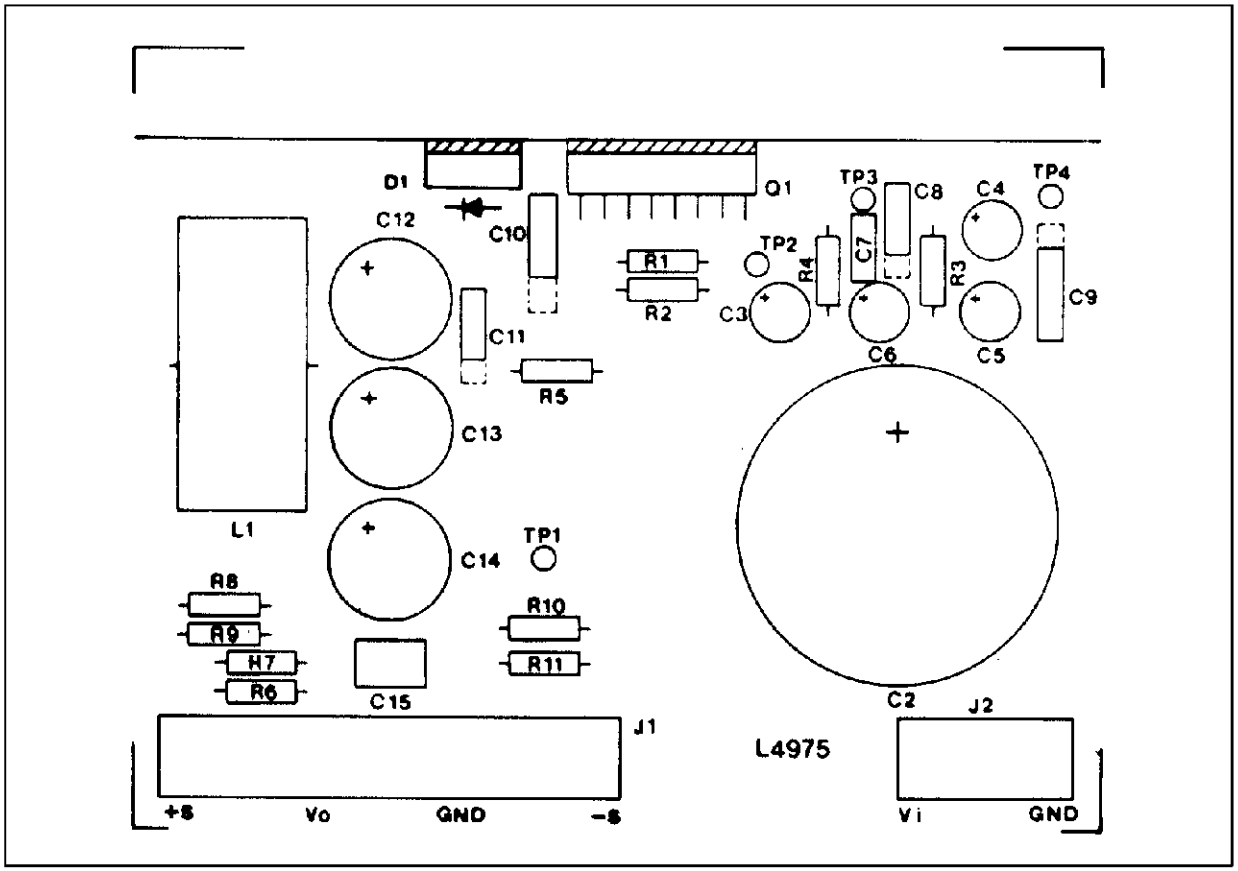
Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit	Fig.
V_{11R}	Rising Threshold Voltage (pin 11)	V_i = 15 to 50V V_3 = 5.3V	V_{ref} –120	V_{ref} –100	V_{ref} –80	V mV	7D
V_{11F}	Falling Threshold Voltage (pin 11)	Vi = 15 to 50V V_3 = 5.3V	4.77	V_{ref} –200	V_{ref} –160	V mV	7D
V_{5H}	Delay High Threshold Voltage	V_i = 15 to 50V V_{11} = V_{14}	4.95	5.1	5.25	V	7D
V_{5L}	Delay Low Threshold Voltage	Vi = 15 to 50V V_{11} = V_{14} V_3 = 5.3V	1	1.1	1.2	V	7D
$-I_{5SO}$	Delay Source Current	V_3 = 5.3V; V_5 = 3V	40	60	80	µA	7D
I_{5SI}	Delay Sink Current	V_3 = 4.7V; V_5 = 3V	10			mA	7D
V_{4S}	Out Saturation Voltage	I_4 = 15mA; S1 = B V_3 = 4.7V			0.4	V	7D
I_4	Output Leak Current	V_4 = 50V; S1 = A V_3 = 5.3V			100	µA	7D
V_{3R}	Rising Threshold Voltage	V_{11} = V_{14}	4.95	5.1	5.25	V	7D
V_{3H}	Hysteresys		0.4	0.5	0.6	V	7D
I_3	Input Bias Current			1	3	µA	7D

Figure 5: Test and Evaluation Board Circuit



TYPICAL PERFORMANCES (using evaluation board) :
n = 83% (V_i = 35V ; V_o = V_{REF} ; I_o = 5A ; f_{SW} = 200KHz)
$V_{o\ RIPPLE}$ = 30mV (at 5A) with output filter capacitor ESR ≤ 60mΩ
Line regulation = 5mV (V_i = 15 to 50V)
Load regulation = 15mV (I_o = 2 to 5A)
For component values, refer to test circuit part list.

Figure 6a: P.C. Board (components side) and Components Layout of Figure 5 (1:1 scale).



PARTS LIST

R_1 = 30KΩ	C_1, C_2 = 3300µF 63V_L EYF (ROE
R_2 = 10KΩ	C_3, C_4, C_5, C_6 = 2.2µF
R_3 = 15KΩ	C_7 = 390pF Film
R_4 = 16KΩ	C_8 = 22nF MKT 1817 (ERO)
R_5 = 22Ω 0,5W	
R_6 = 4K7	C_9 = 2.2nF KP1830
R_7 = 10Ω	C_{10} = 220nF MKT
R_8 = see tab. A	C_{11} = 2.2nF MP1830
R_9 = OPTION	**C_{12}, C_{13}, C_{14} = 220µF 40V_L EKR
R_{10} = 4K7	C_{15} = 1µF Film
R_{11} = 10Ω	
D1 = MBR 760CT (or 7.5A/60V or equivalent)	
L1 = 80µH	core 58930 MAGNETICS 24 TURNS Ø 1.1mm (AWG 17) COGEMA 949178

* 2 capacitors in parallel to increase input RMS current capability
** 3 capacitors in parallel to reduce total output ESR

Table A

V_0	R_9	R_7
12V	4.7kΩ	6.2kW
15V	4.7kΩ	9.1kΩ
18V	4.7kΩ	12kΩ
24V	4.7kΩ	18kΩ

Table B
SUGGESTED BOOTSTRAP CAPACITORS

Operating Frequency	Bootstrap Cap.c10
f = 20KHz	≥680nF
f = 50KHz	≥470nF
f = 100KHz	≥330nF
f = 200KHz	≥220nF
f = 500KHz	≥100nF

Figure 6b: P.C. Board (Back side) and Components Layout of the Circuit of Fig. 5. (1:1 scale)

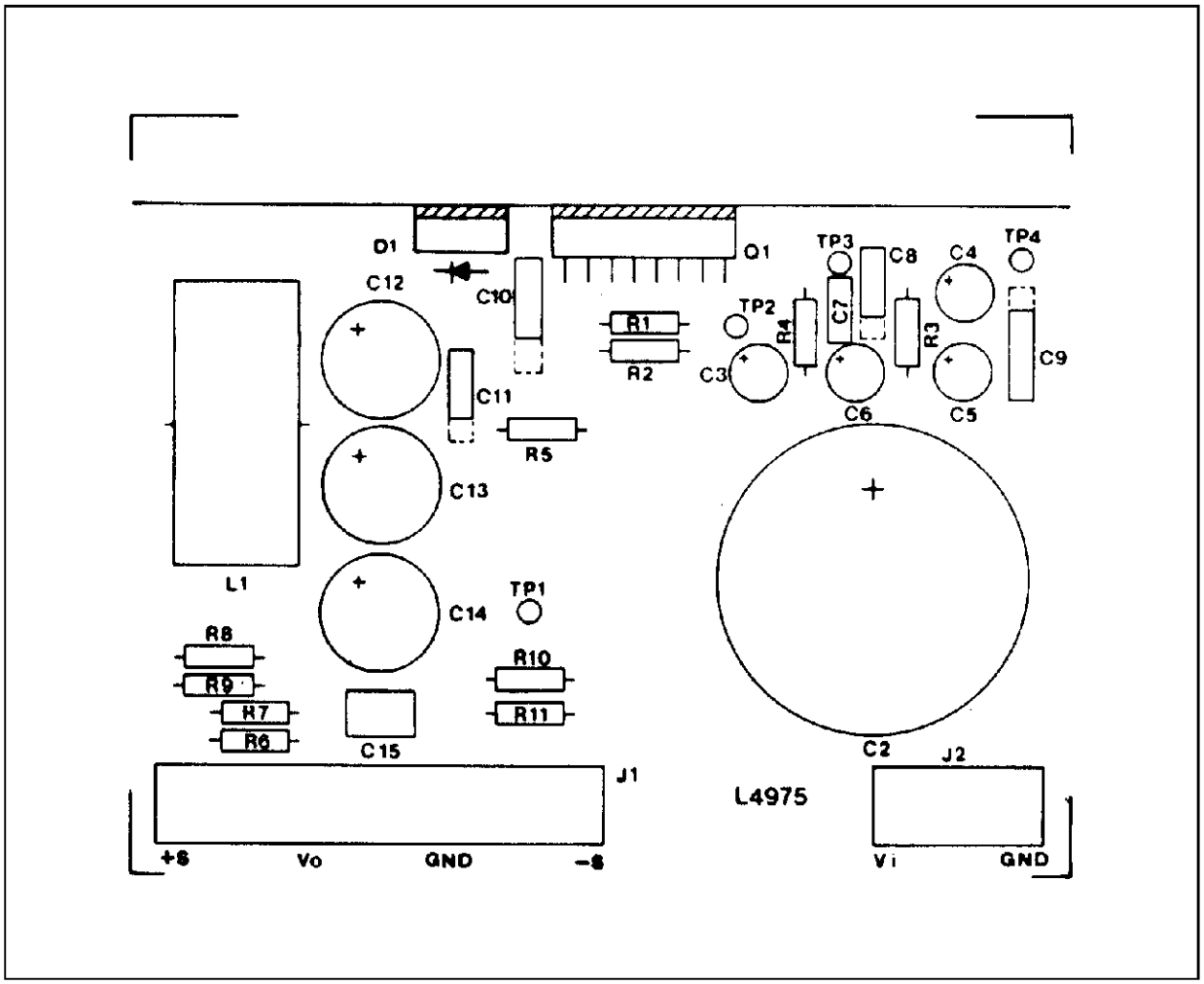


Figure 7: DC Test Circuits

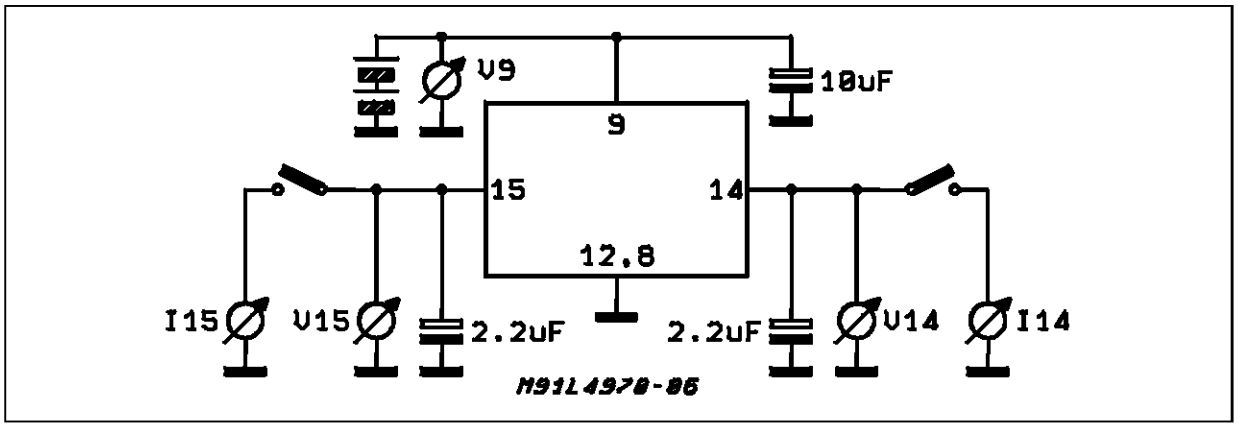


Figure 7A

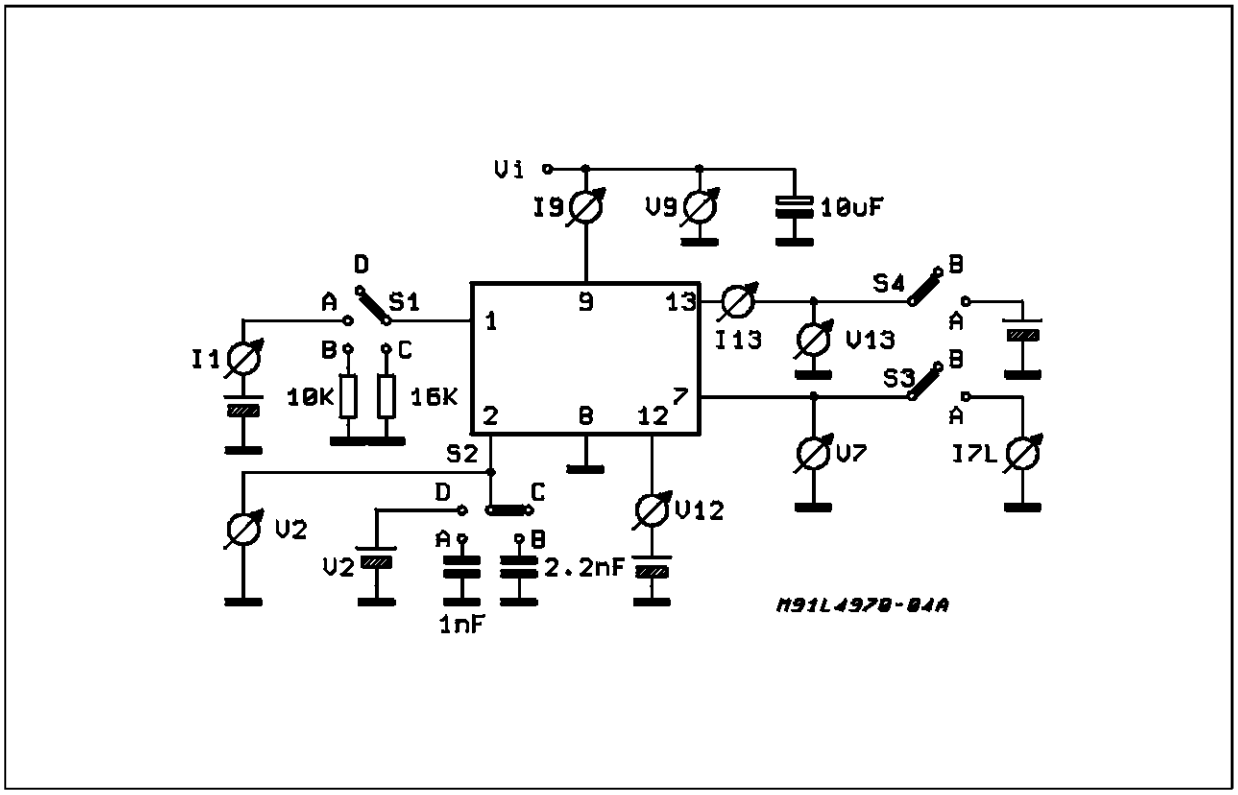


Figure 7B

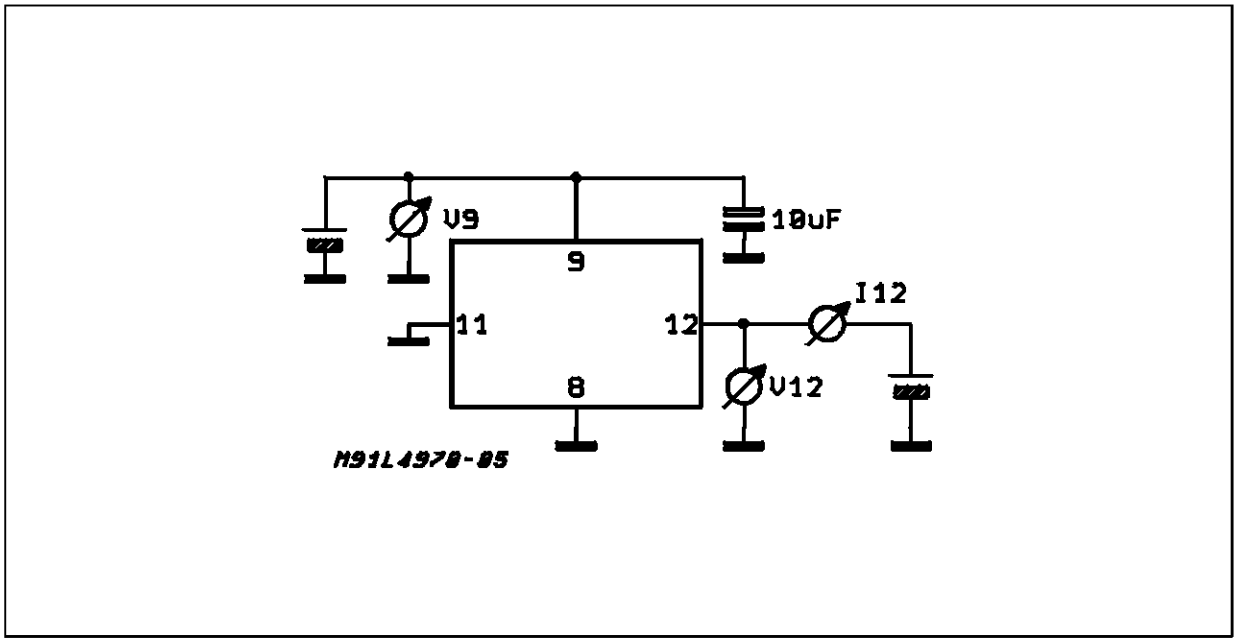


Figure 7D

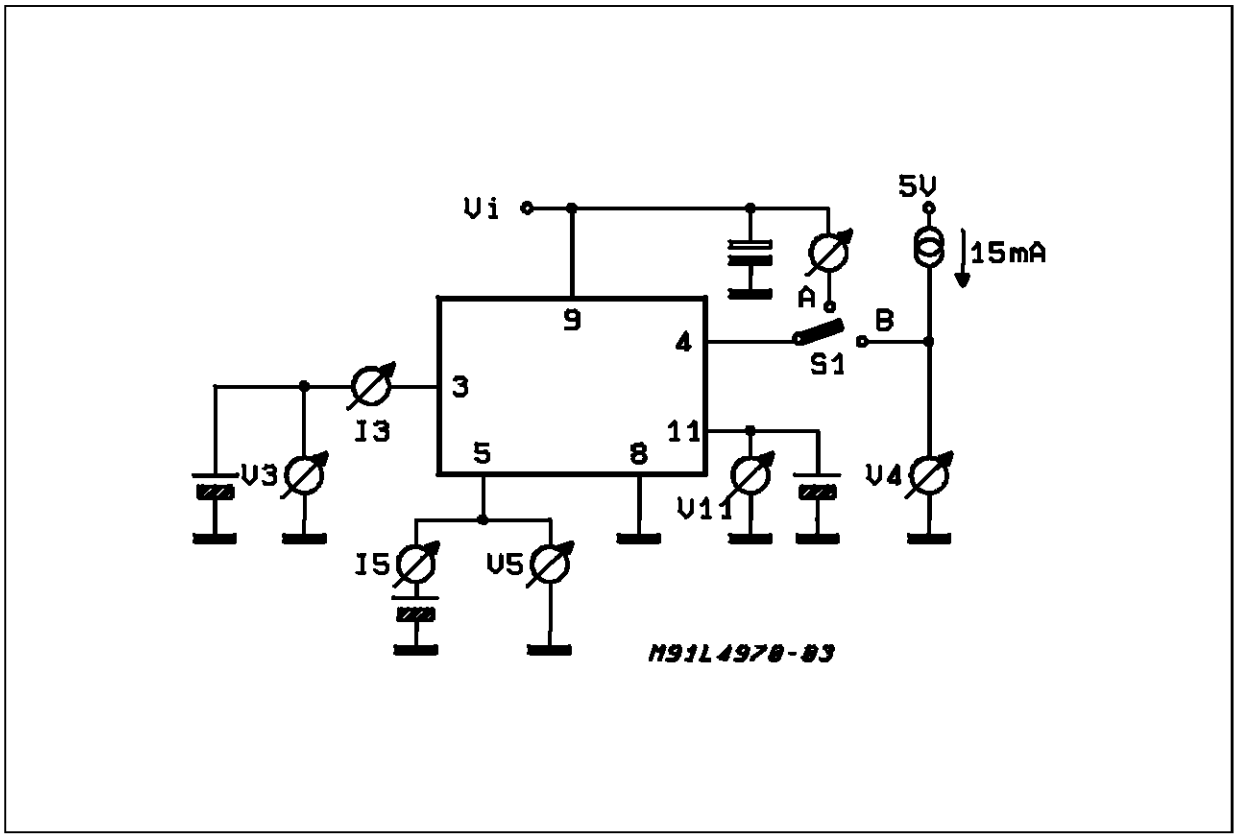


Figure 7C

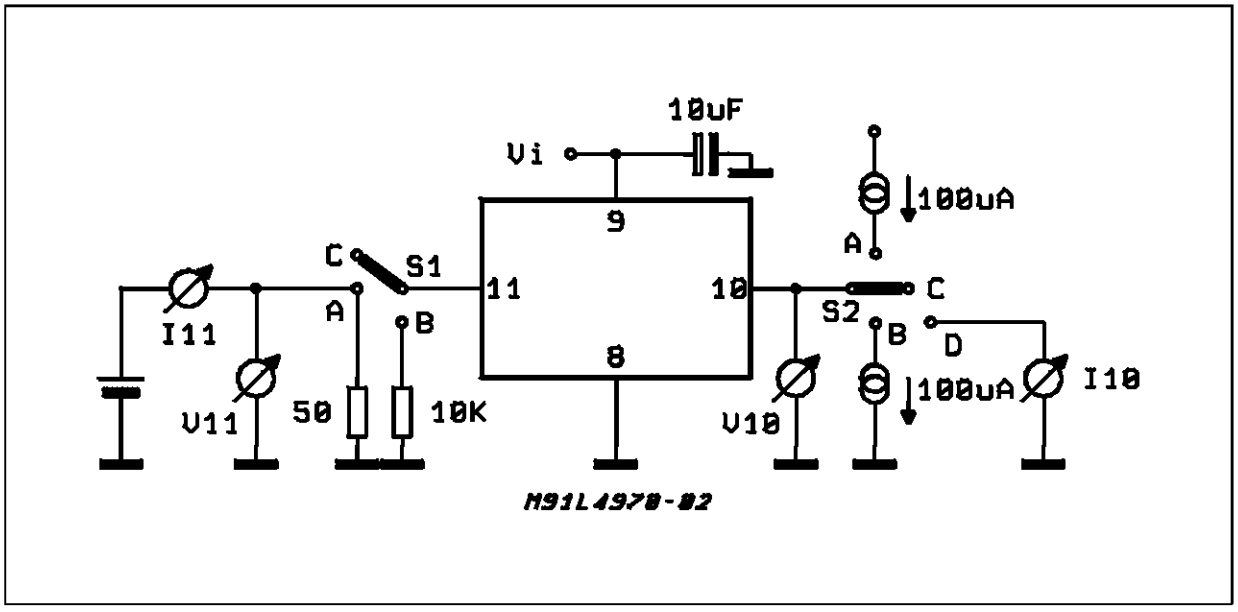


Figure 8: Quiescent Drain Current vs. Supply Voltage (0% duty cycle - see fig. 7A).

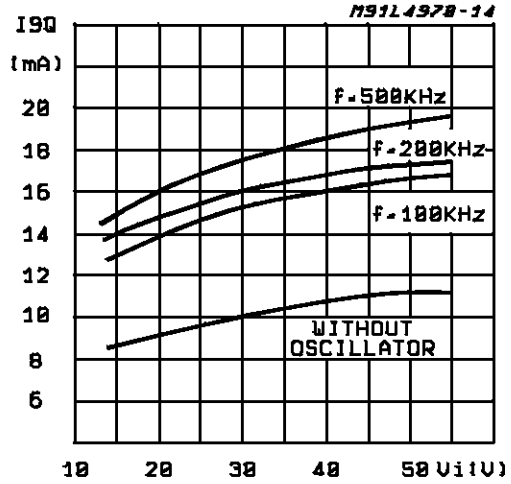


Figure 9: Quiescent Drain Current vs. Junction Temperature (0% duty cycle).

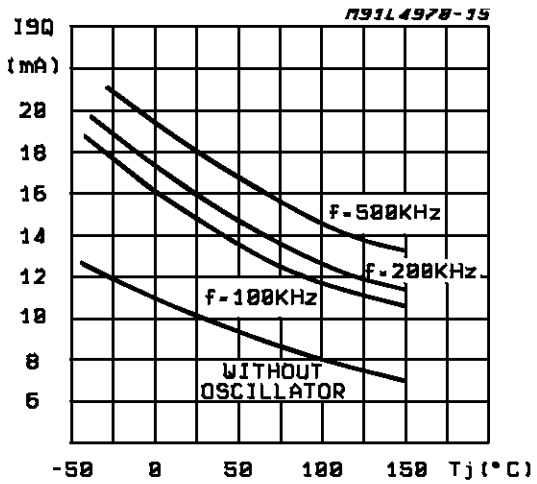


Figure 10: Quiescent Drain Current vs. Duty Cycle

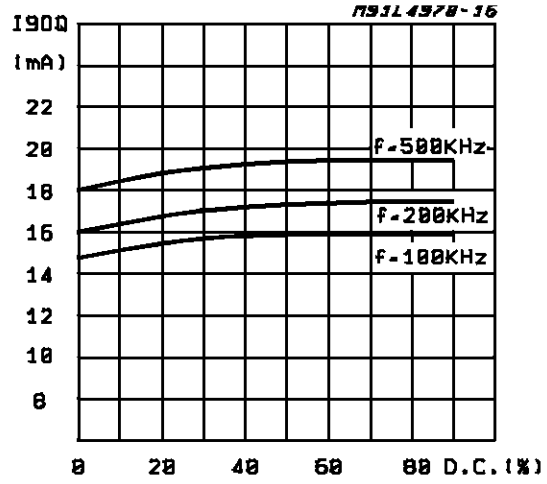


Figure 11: Reference Voltage (pin14) vs. V_i (see fig. 7)

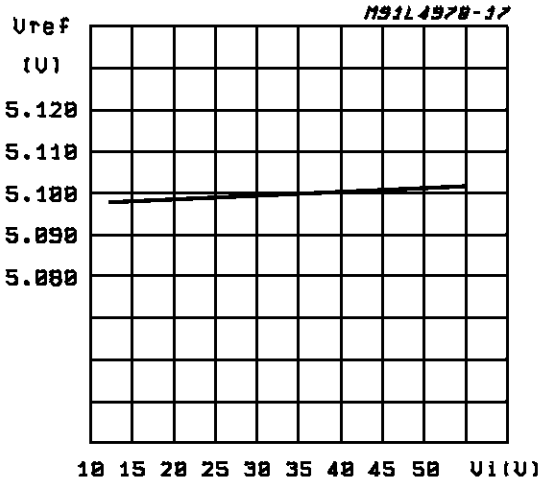


Figure 12: Reference Voltage (pin 14) vs. Junction Temperature (see fig. 7)

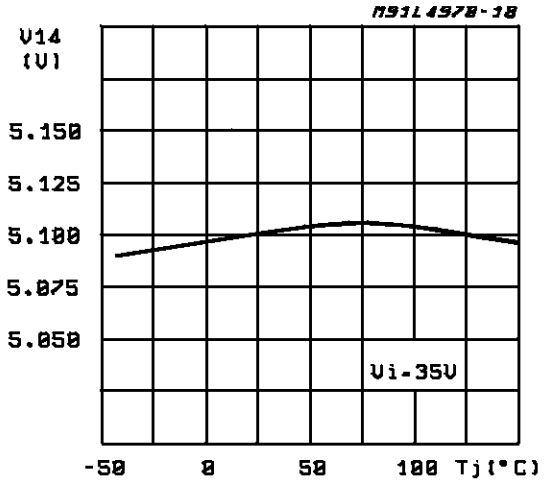


Figure 13: Reference Voltage (pin15) vs. V_i (see fig. 7)

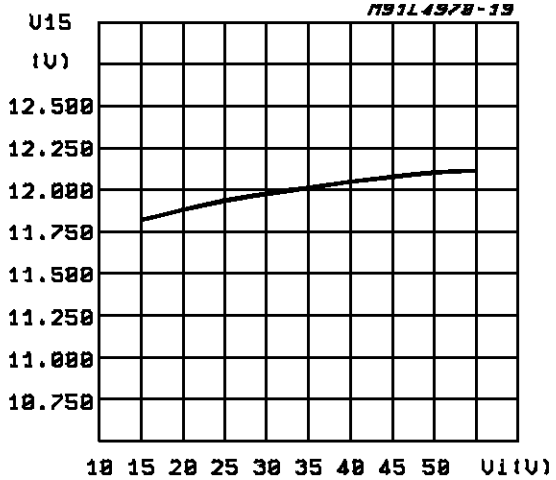


Figure 14: Reference Voltage (pin 15) vs. Junction Temperature (see fig. 7)

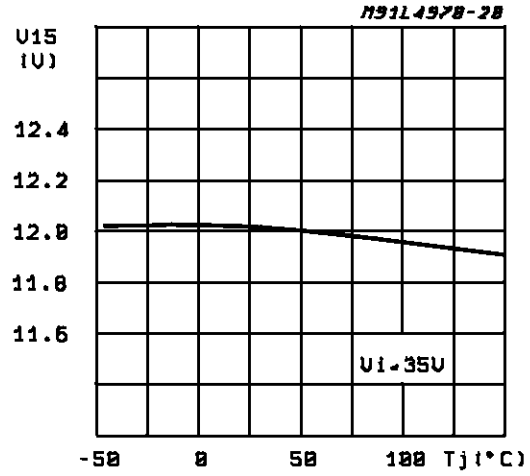


Figure 15: Reference Voltage 5.1V (pin 14) Supply Voltage Ripple Rejection vs. Frequency

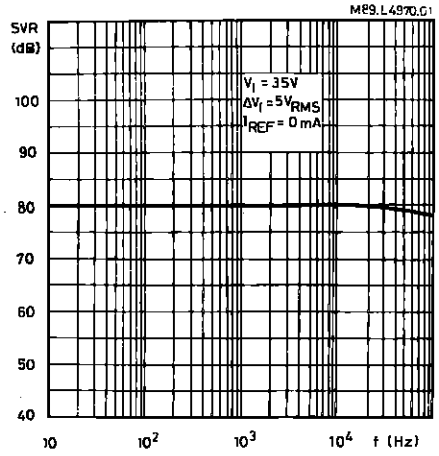


Figure 16: Switching Frequency vs. Input Voltage (see fig. 5)

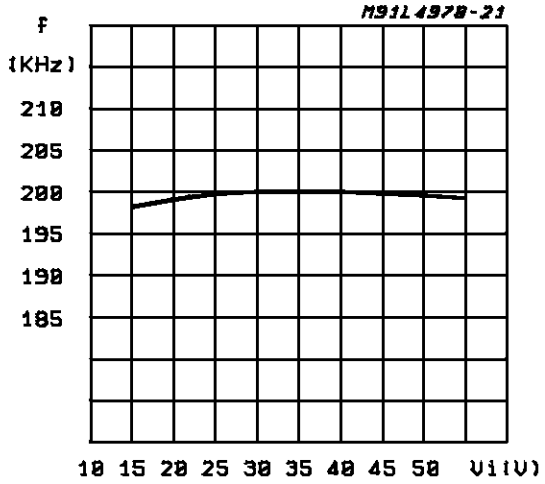


Figure 17: Switching Frequency vs. Junction Temperature (see fig 5)

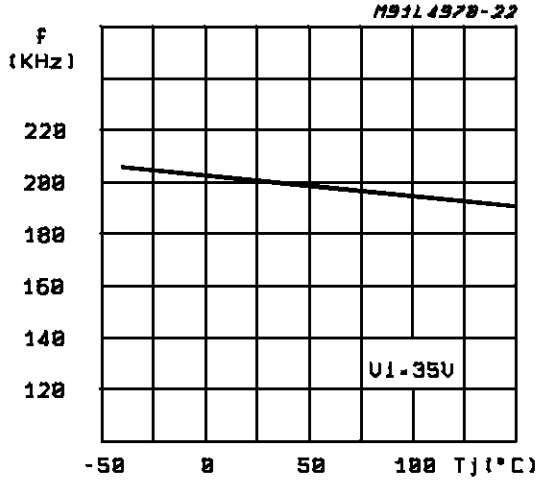


Figure 18: Switching Frequency vs. R4 (see fig. 5)

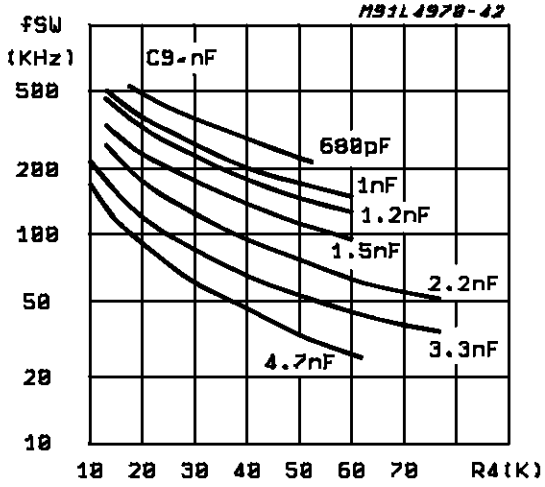


Figure 19: Max. Duty Cycle vs. Frequency

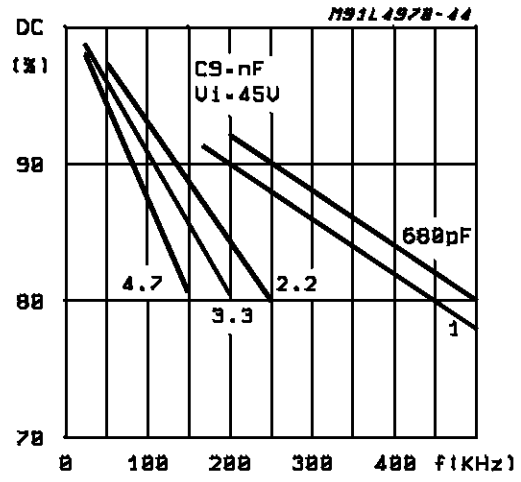


Figure 20: Supply Voltage Ripple Rejection vs. Frequency (see fig. 5)

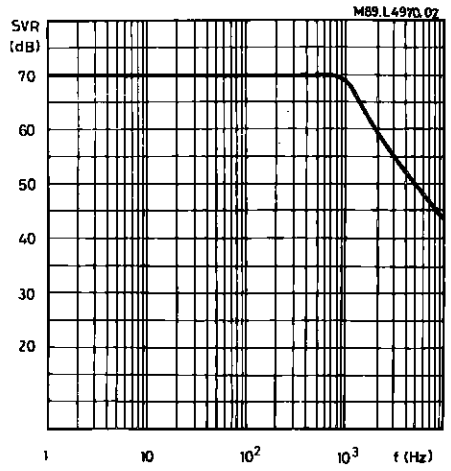


Figure 21: Line Transient Response (see fig. 5)

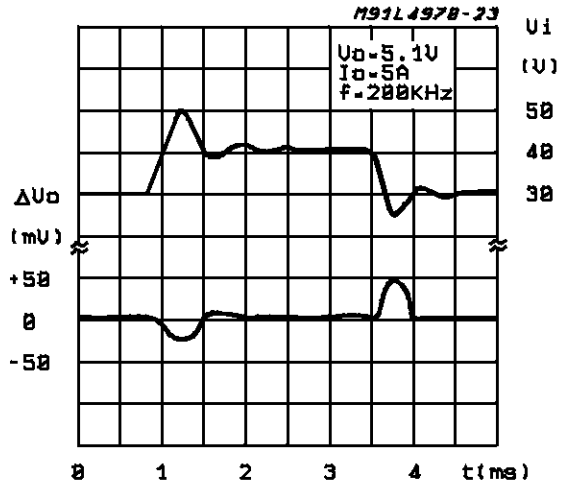


Figure 22: Load Transient Response (see fig. 5)

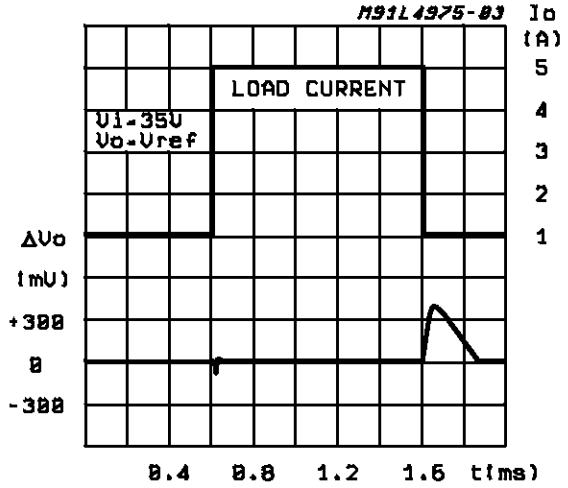


Figure 23: Dropout Voltage Between Pin 9 and Pin 7 vs. Current at Pin 7

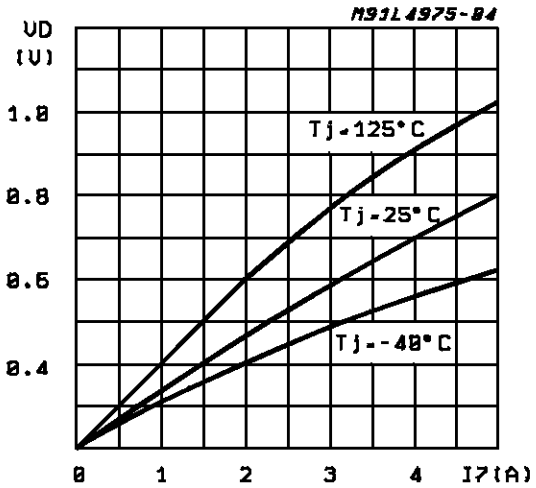


Figure 24: Dropout Voltage Between Pin 9 and Pin 7 vs. Junction Temperature

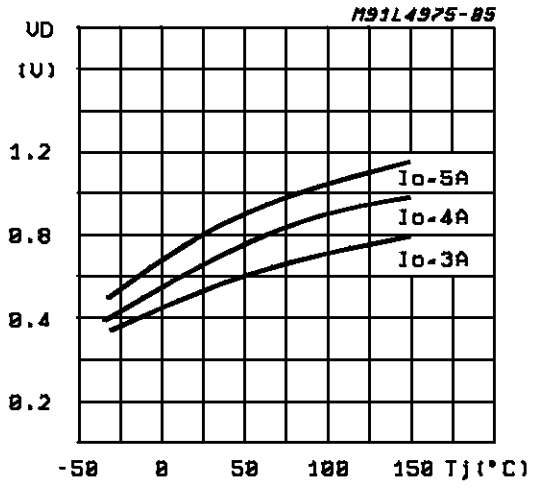


Figure 25: Power Dissipation (device only) vs. Input Voltage

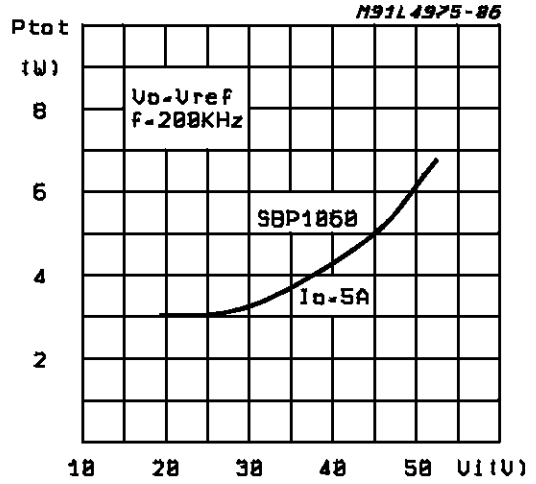


Figure 26: Power Dissipation (device only) vs. Output Voltage

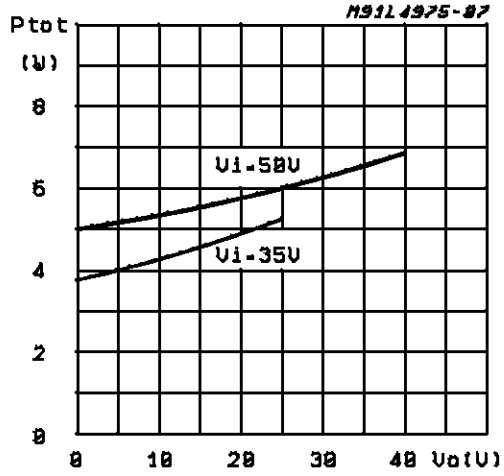


Figure 27: Heatsink Used to Derive the Device's Power Dissipation

$$R_{th} \text{ - Heatsink} = \frac{T_{case} - T_{amb}}{P_d}$$

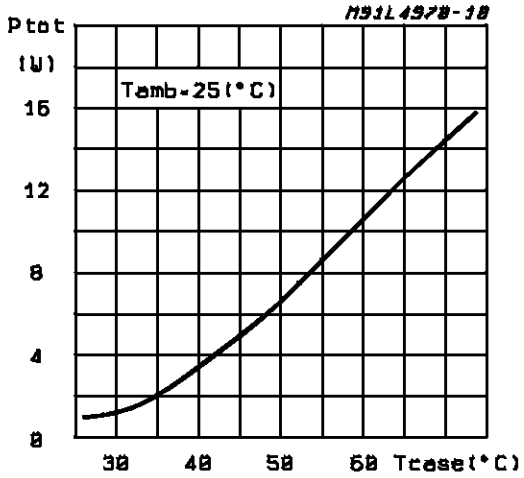


Figure 28: Efficiency vs. Output Current

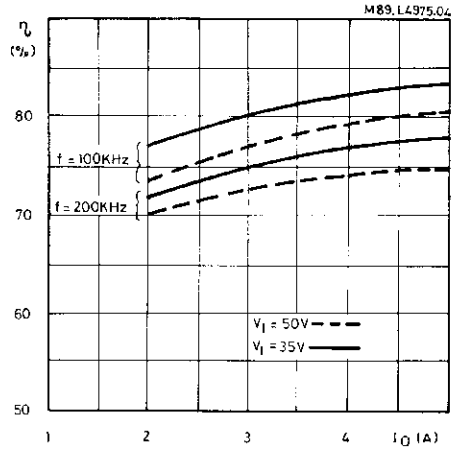


Figure 29: Efficiency vs. Output Voltage

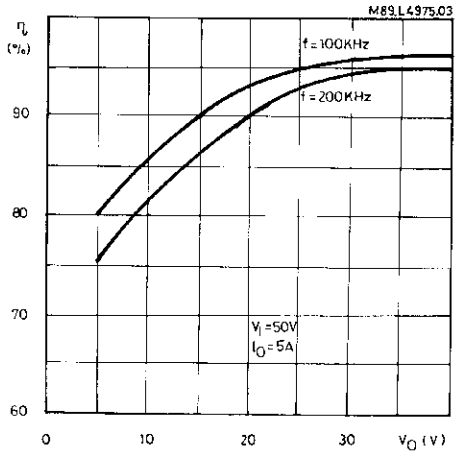


Figure 30: Efficiency vs. Output Voltage

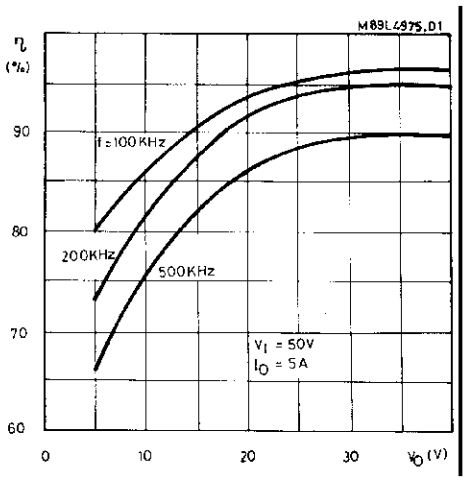


Figure 31: Open Loop Frequency and Phase Response of Error Amplifier (see fig.7C)

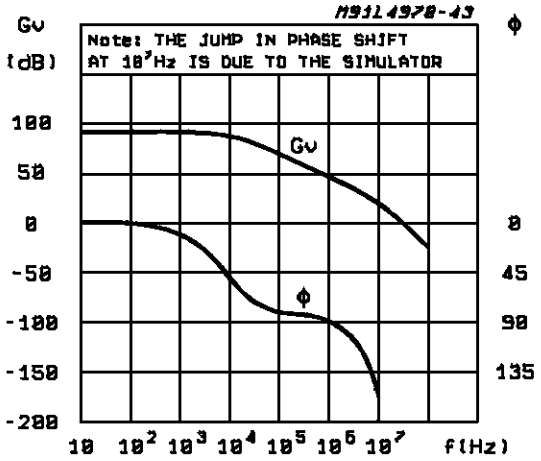


Figure 32: Power Dissipation Derating Curve

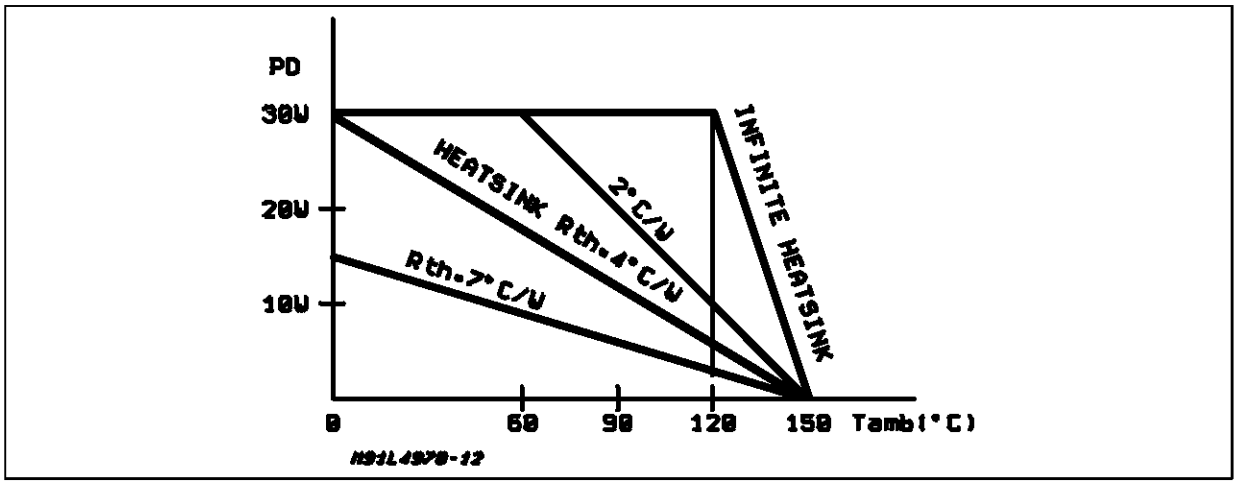


Figure 33: 5.1V/12V Multiple Supply. Note the Synchronization between the L4975A and the L4974A

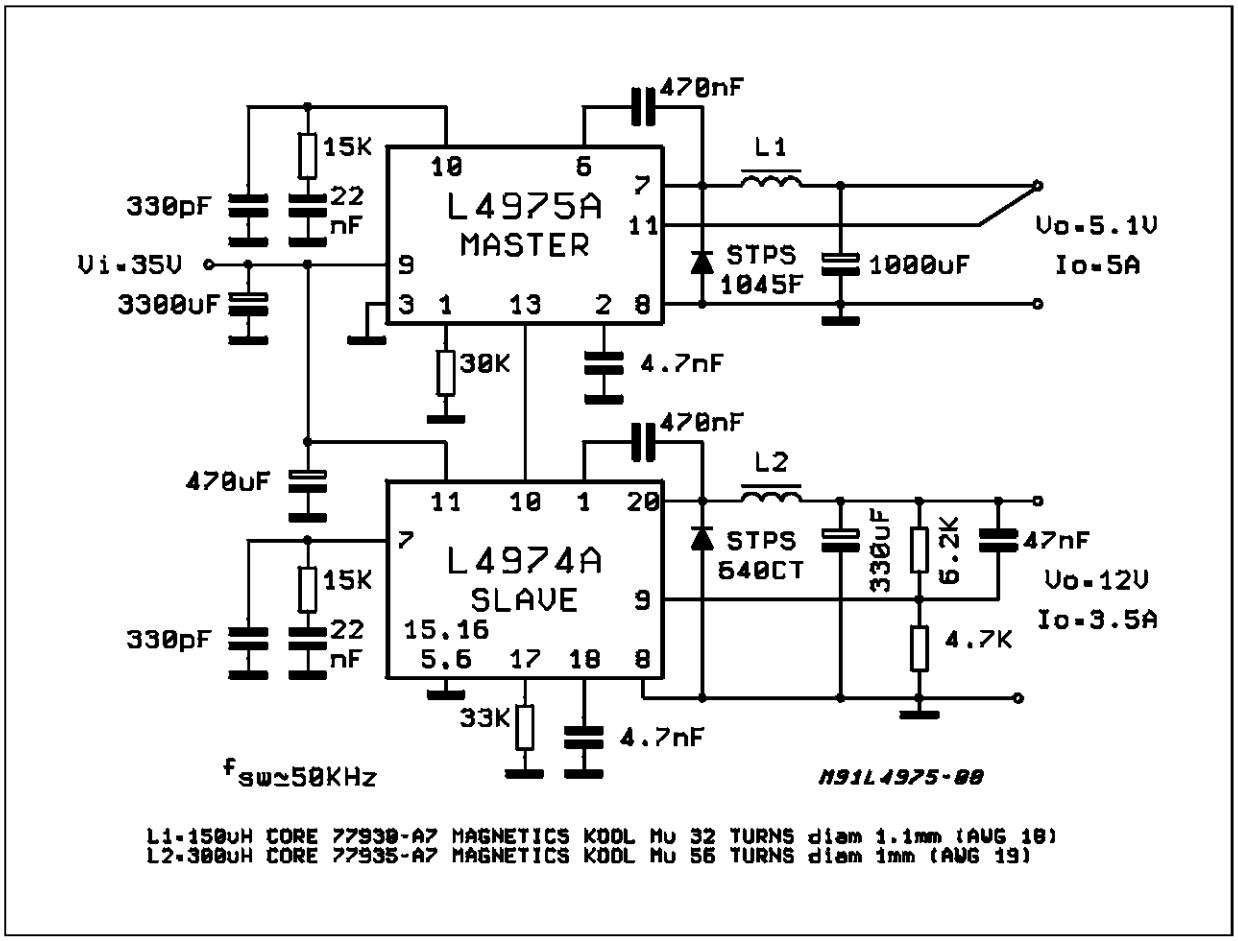


Figure 34: 5.1V / 5A Low Cost Application

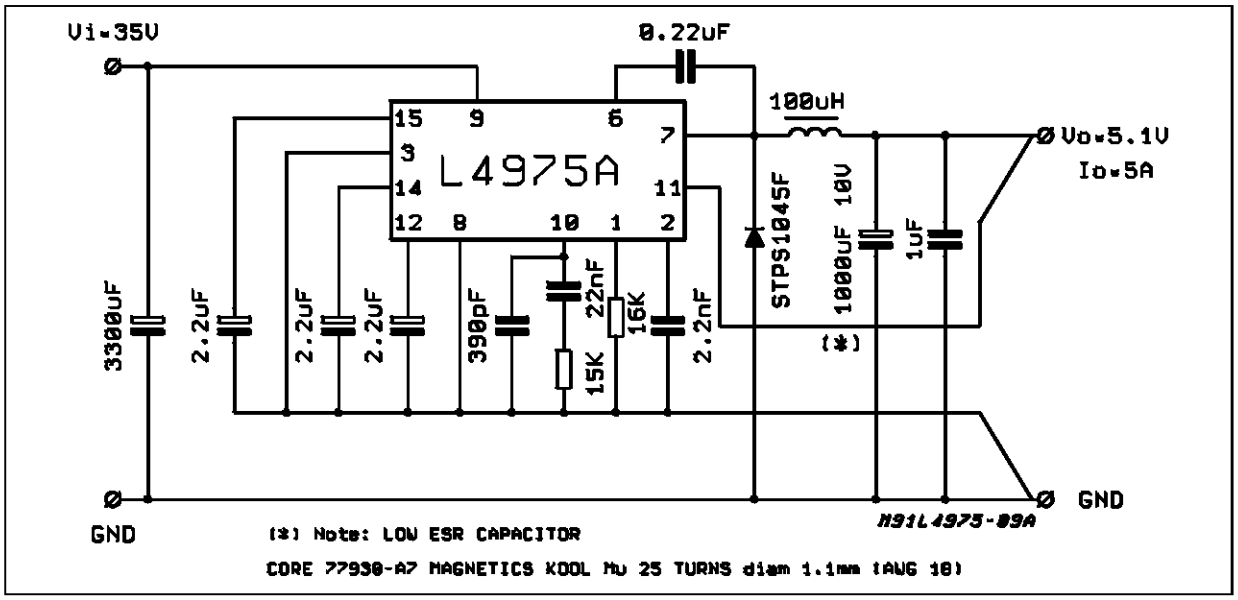


Figure 35: 5A Switching Regulator, Adjustable from 0V to 25V.

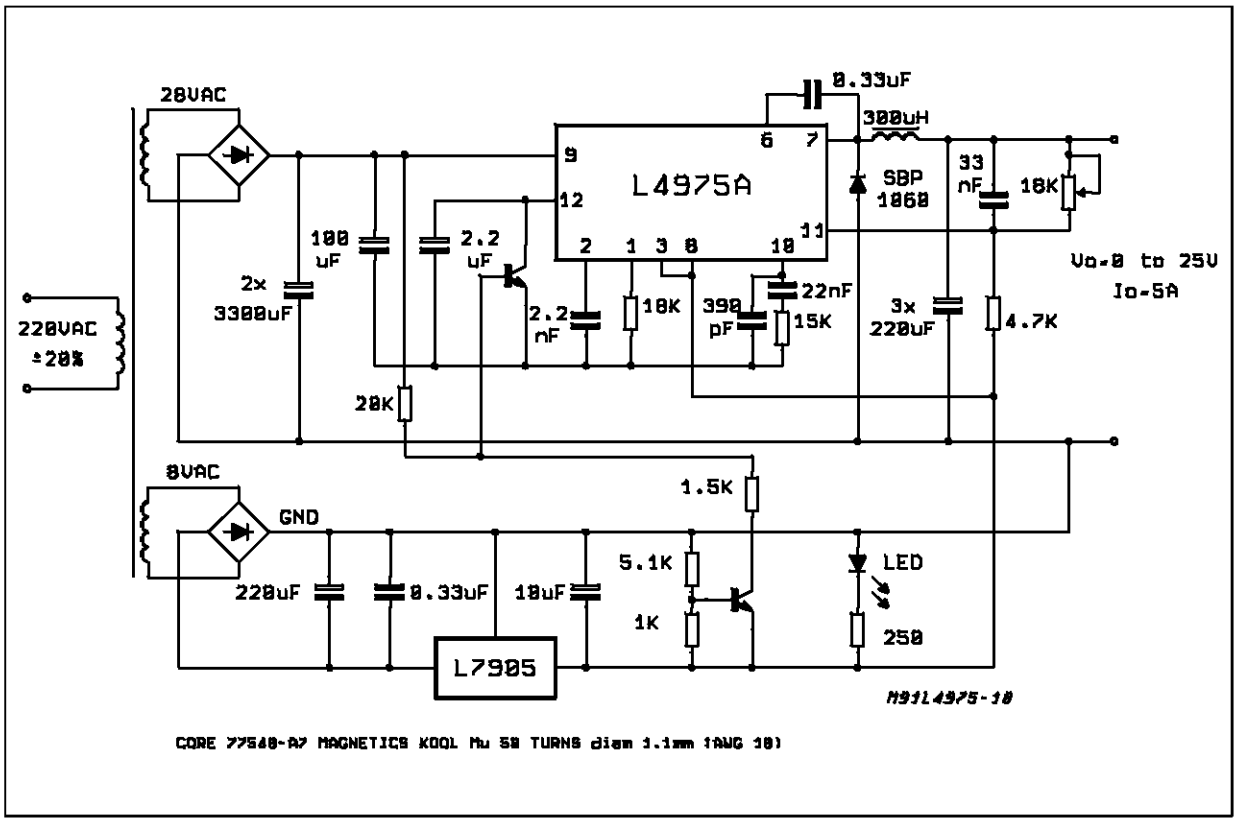
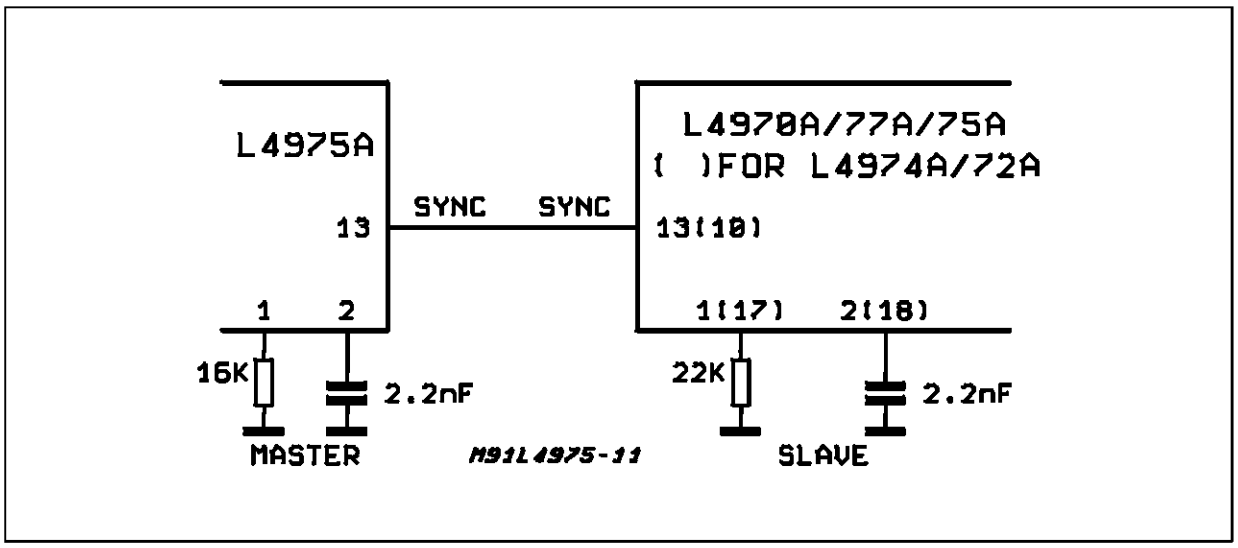
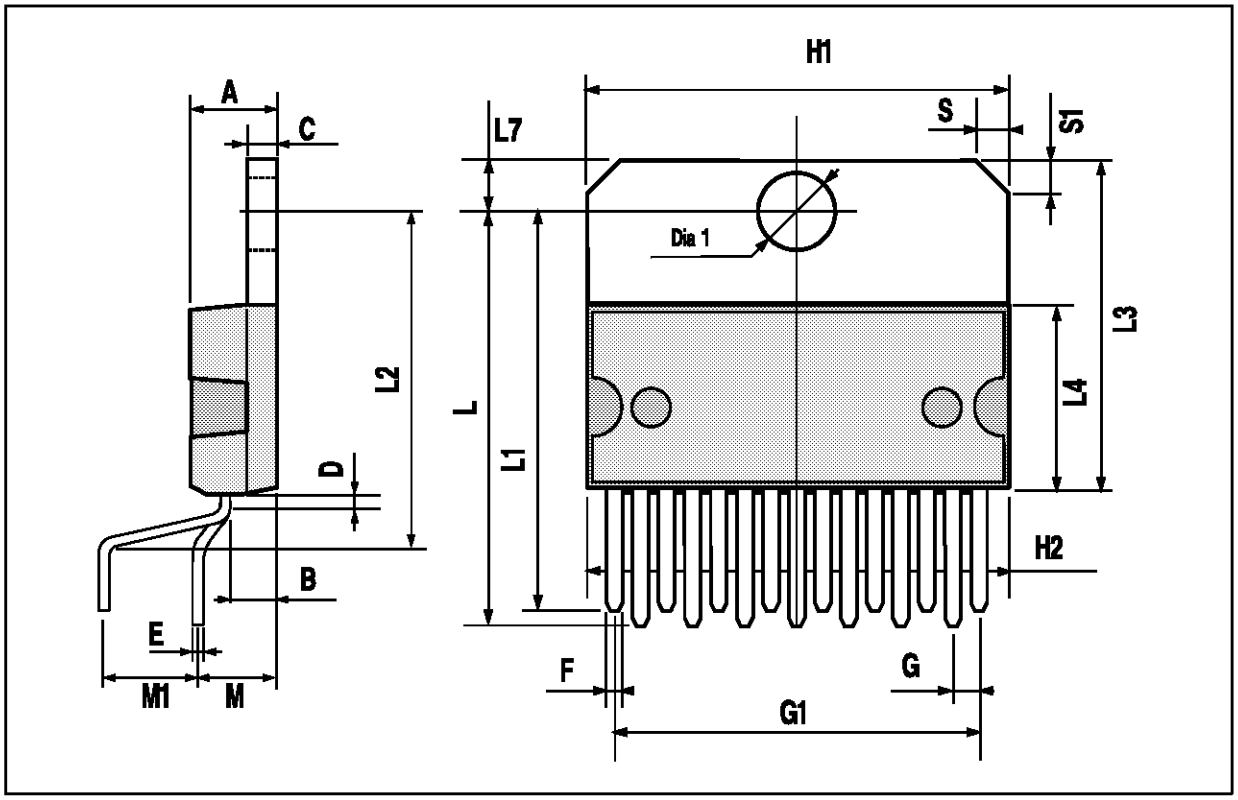


Figure 36: L4975A's Sync. Example



MULTIWATT15 PACKAGE MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			5			0.197
B			2.65			0.104
C			1.6			0.063
D		1			0.039	
E	0.49		0.55	0.019		0.022
F	0.66		0.75	0.026		0.030
G	1.14	1.27	1.4	0.045	0.050	0.055
G1	17.57	17.78	17.91	0.692	0.700	0.705
H1	19.6			0.772		
H2			20.2			0.795
L	22.1		22.6	0.870		0.890
L1	22		22.5	0.866		0.886
L2	17.65		18.1	0.695		0.713
L3	17.25	17.5	17.75	0.679	0.689	0.699
L4	10.3	10.7	10.9	0.406	0.421	0.429
L7	2.65		2.9	0.104		0.114
M	4.2	4.3	4.6	0.165	0.169	0.181
M1	4.5	5.08	5.3	0.177	0.200	0.209
S	1.9		2.6	0.075		0.102
S1	1.9		2.6	0.075		0.102
Dia1	3.65		3.85	0.144		0.152



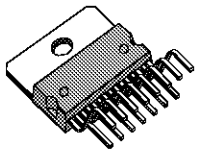
SGS-THOMSON MICROELECTRONICS

L4977A

7A SWITCHING REGULATOR

- 7A OUTPUT CURRENT
- 5.1V TO 40V OUTPUT VOLTAGE RANGE
- 0 TO 90% DUTY CYCLE RANGE
- INTERNAL FEED-FORWARD LINE REGULATION
- INTERNAL CURRENT LIMITING
- PRECISE 5.1V ± 2% ON CHIP REFERENCE
- RESET AND POWER FAIL FUNCTIONS
- SOFT START
- INPUT/OUTPUT SYNC PIN
- UNDER VOLTAGE LOCK OUT WITH HYSTERETIC TURN-ON
- PWM LATCH FOR SINGLE PULSE PER PERIOD
- VERY HIGH EFFICIENCY
- SWITCHING FREQUENCY UP TO 500KHz
- THERMAL SHUTDOWN
- CONTINUOUS MODE OPERATION

MULTIPOWER BCD TECHNOLOGY



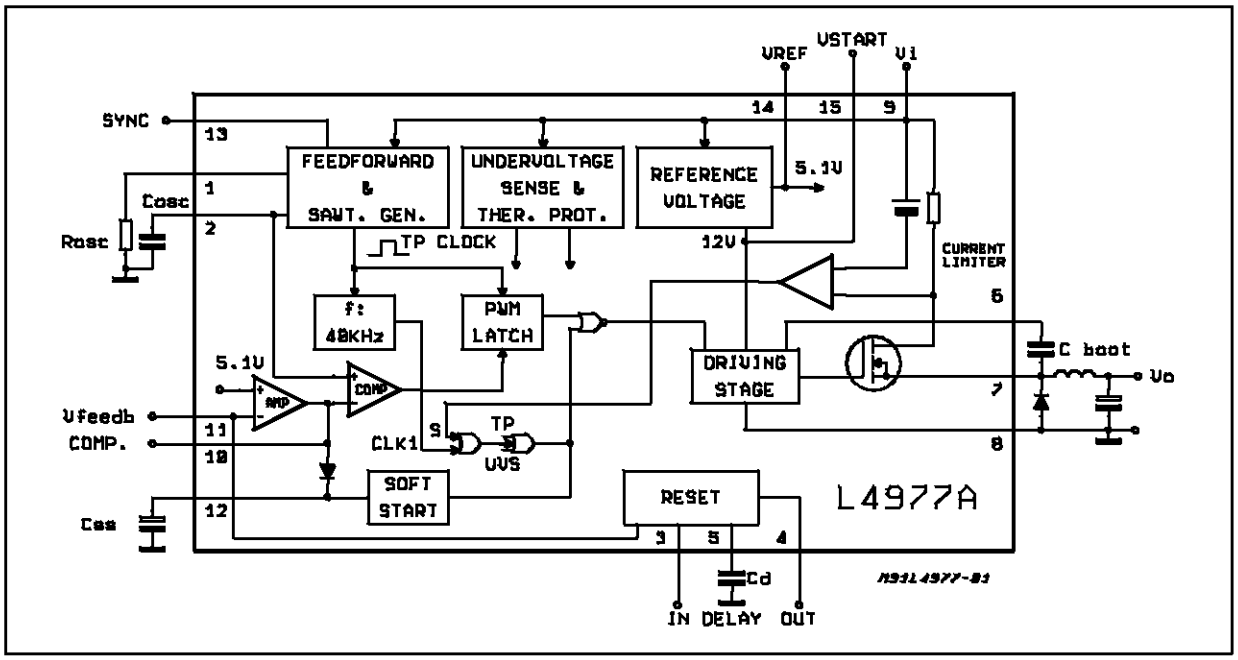
Multiwatt15V
ORDERING NUMBER: L4977A

DESCRIPTION

The L4977A is a stepdown monolithic power switching regulator delivering 7A at a voltage variable from 5.1 to 40V.

Realized with BCD mixed technology, the device uses a DMOS output transistor to obtain very high efficiency and very fast switching times. Features of the L4977A include reset and power fail for microprocessors, feed forward line regulation, soft start, limiting current and thermal protection. The device is mounted in a 15-lead multiwatt plastic power package and requires few external components. Efficient operation at switching frequencies up to 500KHz allows reduction in the size and cost of external filter components.

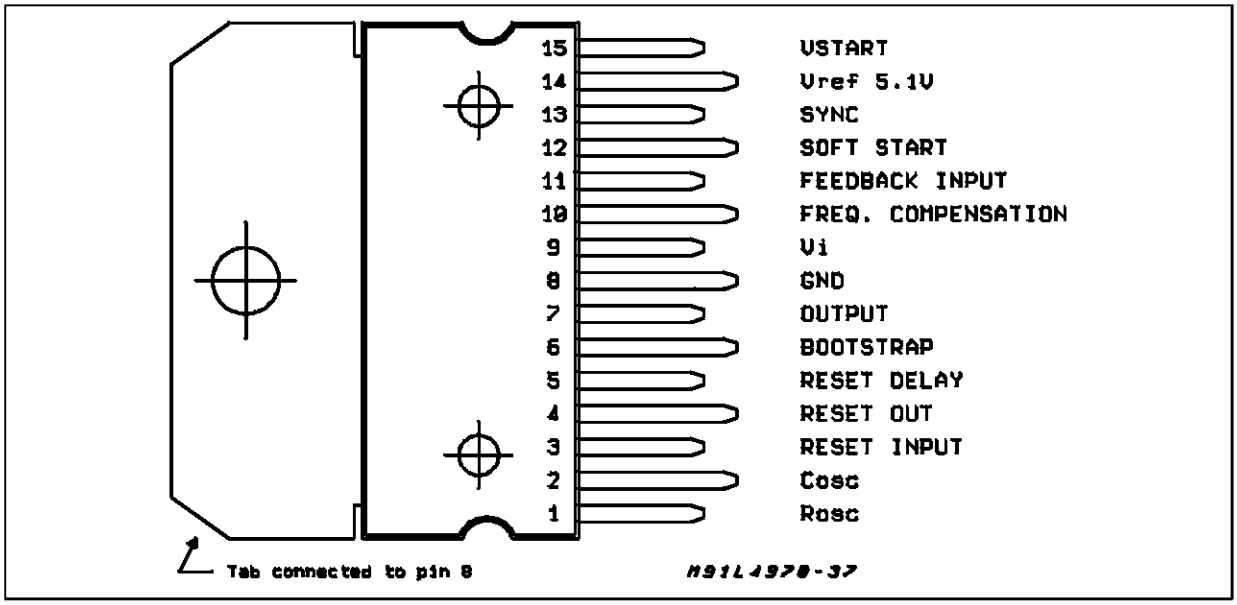
BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_9	Input Voltage	55	V
V_9	Input Operating Voltage	50	V
V_7	Output DC Voltage Output Peak Voltage at t = 0.1µs f = 200KHz	-1 -7	V V
I_7	Maximum Output Current	Internally Limited	
V_6	Bootstrap Voltage Bootstrap Operating Voltage	65 V_9 + 15	V V
V_3, V_{12}	Input Voltage at Pins 3, 12	12	V
V_4	Reset Output Voltage	50	V
I_4	Reset Output Sink Current	50	mA
V_5, V_{10}, V_{11}, V_{13}	Input Voltage at Pin 5, 10, 11, 13	7	V
I_5	Reset Delay Sink Current	30	mA
I_{10}	Error Amplifier Output Sink Current	1	A
I_{12}	Soft Start Sink Current	30	mA
P_{tot}	Total Power Dissipation at T_{case} < 120°C	30	W
T_j, T_{stg}	Junction and Storage Temperature	-40 to 150	°C

PIN CONNECTION (Top view)



THERMAL DATA

Symbol	Parameter		Value	Unit
$R_{th\ j\text{-}case}$	Thermal Resistance Junction-case	max	1	°C/W
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient	max	35	°C/W

PIN FUNCTIONS

N°	Name	Function
1	OSCILLATOR	R_{osc}. External resistor connected to ground determines the constant charging current of C_{osc}.
2	OSCILLATOR	C_{osc}. External capacitor connected to ground determines (with R_{osc}) the switching frequency.
3	RESET INPUT	Input of Power Fail Circuit. The threshold is 5.1V. It may be connected via a divider to the input for power fail function. It must be connected to the pin 14 an external 30KΩ resistor when power fail signal not required.
4	RESET OUT	Open Collector Reset/power Fail Signal Output. This output is high when the supply and the output voltages are safe.
5	RESET DELAY	A C_d capacitor connected between this terminal and ground determines the reset signal delay time.
6	BOOTSTRAP	A C_{boot} capacitor connected between this terminal and the output allows to drive properly the internal D-MOS transistor.
7	OUTPUT	Regulator Output.
8	GROUND	Common Ground Terminal
9	SUPPLY VOLTAGE	Unregulated Input Voltage.
10	FREQUENCY COMPENSATION	A series RC network connected between this terminal and ground determines the regulation loop gain characteristics.
11	FEEDBACK INPUT	The Feedback Terminal of the Regulation Loop. The output is connected directly to this terminal for 5.1V operation; It is connected via a divider for higher voltages.
12	SOFT START	Soft Start Time Constant. A capacitor is connected between thi sterminal and ground to define the soft start time constant.
13	SYNC INPUT	Multiple L4977A are synchronized by connecting pin 13 inputs together or via an external syncr. pulse.
14	V_{ref}	5.1V V_{ref} Device Reference Voltage.
15	V_{start}	Internal Start-up Circuit to Drive the Power Stage.

CIRCUIT OPERATION (refer to the block diagram)

The L4977A is a 7A monolithic stepdown switching regulator working in continuous mode realized in the new BCD Technology. This technology allows the integration of isolated vertical DMOS power transistors plus mixed CMOS/Bipolar transistors.

The device can deliver 7A at an output voltage adjustable from 5.1V to 40V, and contains diagnostic and control functions that make it particularly suitable for microprocessor based systems.

BLOCK DIAGRAM

The block diagram shows the DMOS power transistor and the PWM control loop. Integrated functions include a reference voltage trimmed to 5.1V ± 2%, soft start, undervoltage lockout, oscillator with feedforward control, pulse by pulse current limit, thermal shutdown and finally the reset and power fail circuit. The reset and power fail circuit provides an output signal for a microprocessor indicating the status of the system.

Device turn on is around 11V with a typical 1V hysteresis, this threshold provides a correct voltage for the driving stage of the DMOS gate and the hysteresis prevents instabilities.

An external bootstrap capacitor charged to 12V by an internal voltage reference is needed to provide correct gate drive to the power DMOS. The driving circuit is able to source and sink peak currents of around 0.5A to the gate of the DMOS transistor. A typical switching time of the current in the DMOS transistor is 50ns. Due to the fast commutation switching frequencies up to 500kHz are possible.

The PWM control loop consists of a sawtooth oscillator, error amplifier, comparator, latch and the output stage. An error signal is produced by comparing the output voltage with the precise 5.1V ± 2% on chip reference. This error signal is then compared with the sawtooth oscillator, in order to generate a fixed frequency pulse width modulated drive for the output stage. A PWM latch is included to eliminate multiple pulsing within a period even in noisy environments. The gain and

Figure 1: Feedforward Waveform

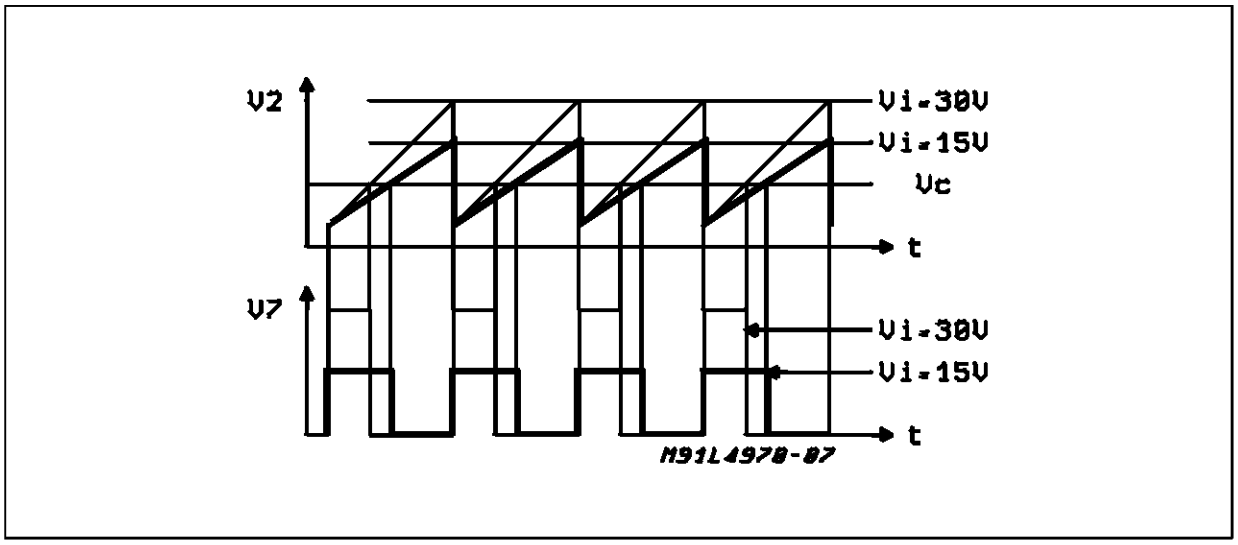


Figure 2: Soft Start Function

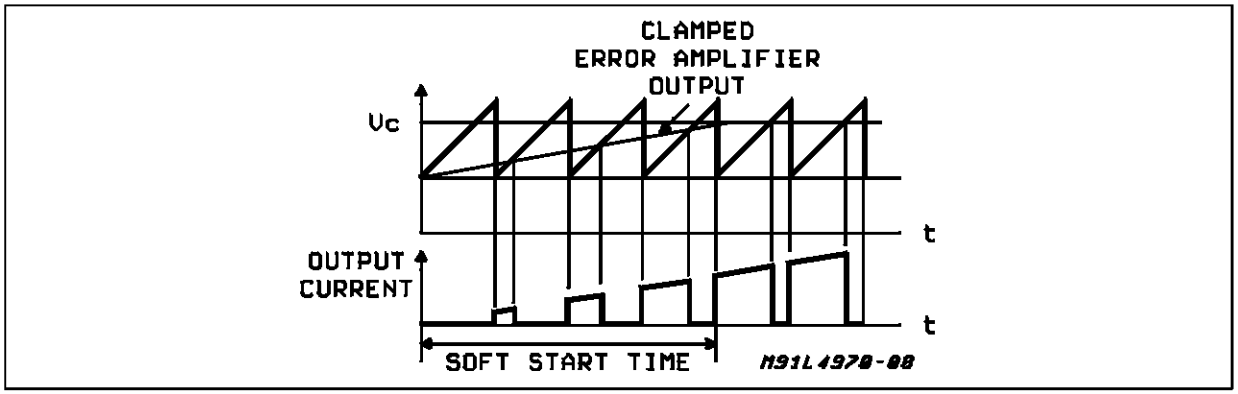
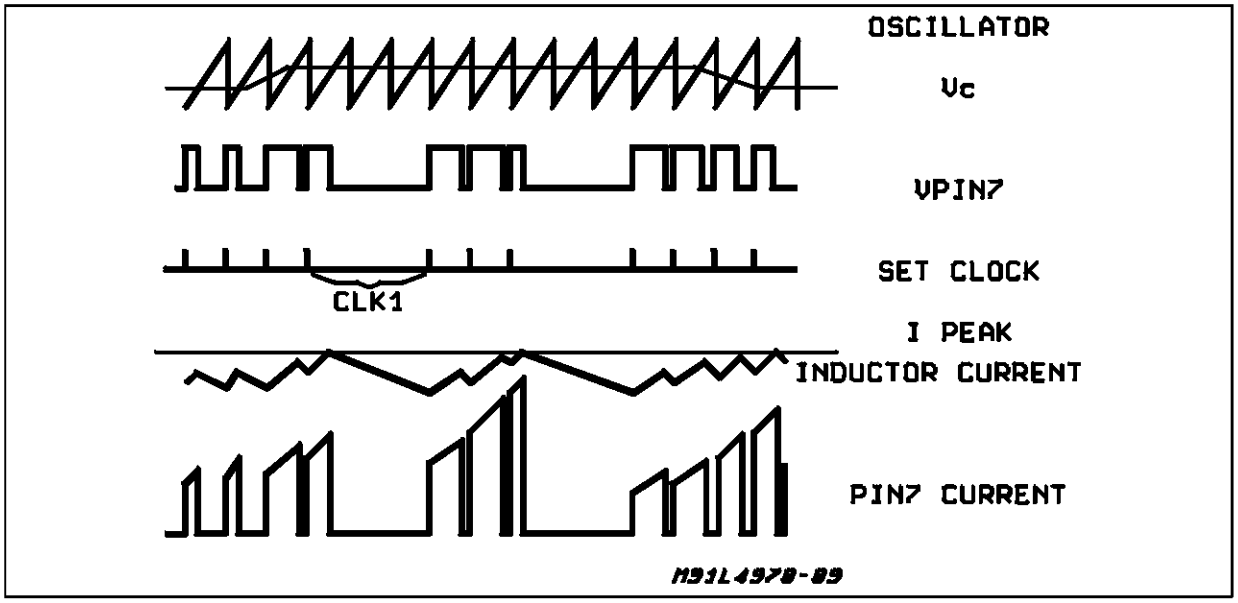


Figure 3: Limiting Current Function



stability of the loop can be adjusted by an external RC network connected to the output of the error amplifier. A voltage feedforward control has been added to the oscillator, this maintains superior line regulation over a wide input voltage range. Closing the loop directly gives an output voltage of 5.1V, higher voltages are obtained by inserting a voltage divider.

At turn on output overcurrents are prevented by the soft start function (fig. 2). The error amplifier is initially clamped by an external capacitor Css and allowed to rise linearly under the charge of an internal constant current source.

Output overload protection is provided by a current limit circuit (fig. 3). The load current is sensed by an internal metal resistor connected to a comparator. When the load current exceeds a preset threshold the output of the comparator sets a flip flop which turns off the power DMOS. The next clock pulse, from an internal 40kHz oscillator will reset the flip flop and the power DMOS will again conduct. This current protection method, ensures a constant current output when the system is overloaded or short circuited and limits the switching frequency, in this condition, to 40kHz.

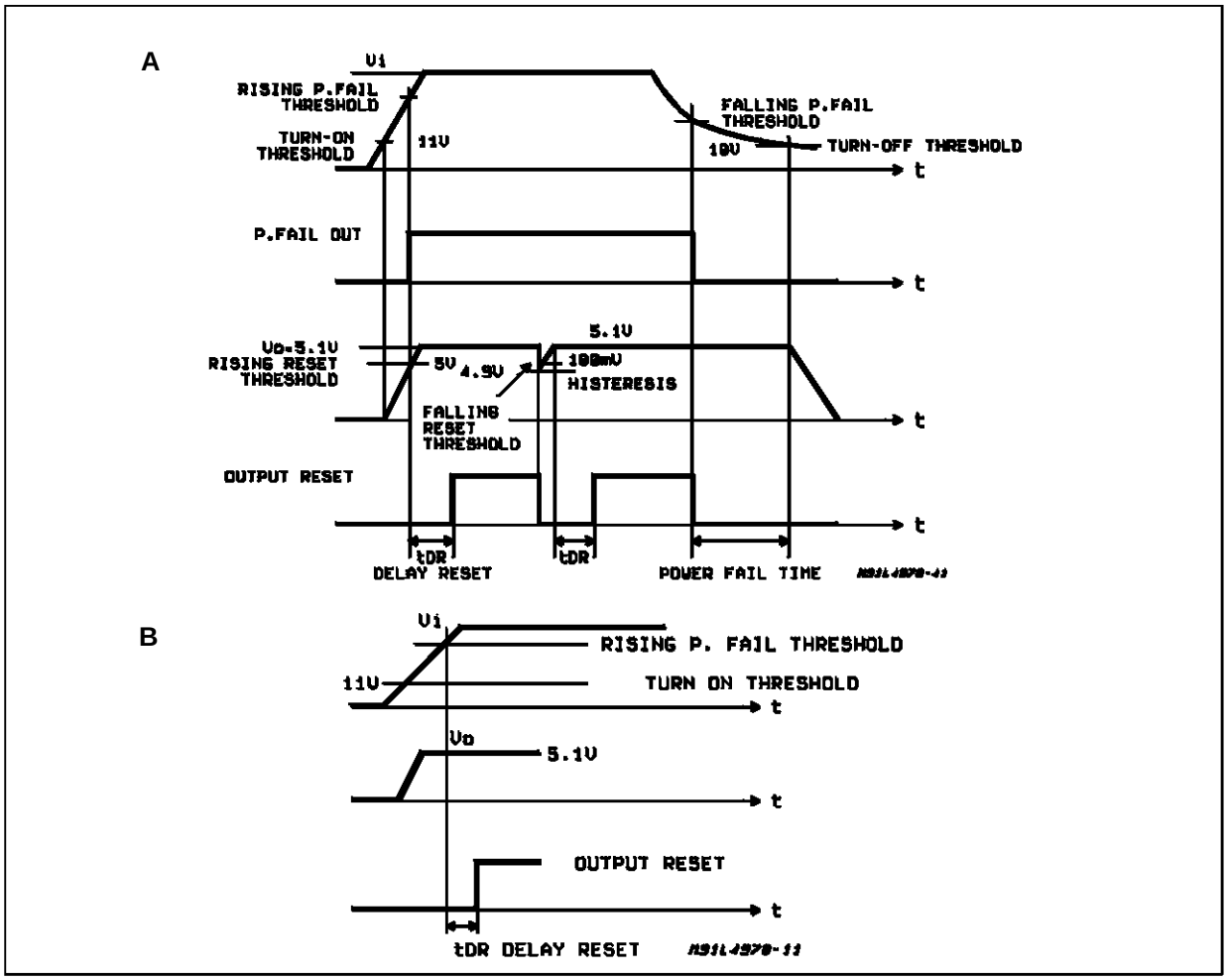
The Reset and Power fail circuitry (fig 4) generates an output signal when the supply voltage exceeds a threshold programmed by an external voltage divider. The reset signal, is generated with a delay time programmed by an external capacitor on the delay pin. When the supply voltage falls below the threshold or the output voltage goes below 5V the reset output goes low immediately. The reset output is an open collector-drain.

Fig 4A shows the case when the supply voltage is higher than the threshold, but the output voltage is not yet 5V.

Fig 4B shows the case when the output is 5.1V but the supply voltage is not yet higher than the fixed threshold.

The thermal protection disables circuit operation when the junction temperature reaches about 150°C and has an hysterysis to prevent unstable conditions.

Figure 4: Reset and Power Fail Functions.



ELECTRICAL CHARACTERISTICS (Refer to the test circuit, T_j = 25°C, V_i = 35V, R_4 = 16KΩ, C_9 = 2.2nF, f_{SW} = 200KHz typ, unless otherwise specified)

DYNAMIC CHARACTERISTICS

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit	Fig.
V_i	input Voltage Range (pin 9)	V_o = V_{ref} to 40V I_o = 7A	15		50	V	5
V_o	Output Votage	V_i = 15V to 50V I_o = 3A; V_o = V_{ref}	5	5.1	5.2	V	5
ΔV_o	Line Regulation	V_i = 15V to 50V I_o = 2A; V_o = V_{ref}		12	30	mV	5
ΔV_o	Load Regulation	V_o = V_{ref} I_o = 3A to 5A I_o = 2A to 7A		 10 20	 25 40	 mV mV	5
V_d	Dropout Voltage Between Pin 9 and 7	I_o = 5A I_o = 7A		0.4 0.8	0.6 1.1	V V	5
I_{7L}	Max. Limiting Current	V_o = V_{ref} to 40V V_i = 15 to 50V	8	9.5	11	A	5
η	Efficiency	I_o = 3A V_o = V_{ref} V_o = 12V	70	 75 80		 % %	5
		I_o = 7A V_o = V_{ref} V_o = 12V	75	 80 87		 % %	5
SVR	Supply Voltage Ripple Reject.	V_i = 2VRMS; I_o = 3A f = 100Hz; V_o = V_{ref}	56	60		dB	5
f	Switching Frequency		180	200	220	KHz	5
$\frac{\Delta f}{\Delta V_i}$	Voltage Stability of Swiching Frequency	V_i = 15V to 45V		2	6	%	5
$\frac{\Delta f}{T_j}$	Temperature Stability of Swiching Frequency	T_j = 0 to 125°C		1		%	5
f_{max}	Maximum Operating Switching Frequency	V_o = V_{ref}; R_4 = 10KΩ I_o = 7A; C_9 = 1nF	500			KHz	5

V_{ref} SECTION (pin 14)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit	Fig.
V_{14}	Reference Voltage		5	5.1	5.2	V	7
ΔV_{14}	Line Regulation	V_i = 15V to 50V		10	25	mV	7
ΔV_{14}	Load Regulation	I_{14} = 0 to 1mA		20	40	mV	7
$\frac{\Delta V_{14}}{\Delta T}$	Average Temperature Coefficient Reference Voltage	T_j = 0°C to 125°C		0.4		mV/°C	7
$I_{14\ short}$	Short Circuit Current Limit	V_{14} = 0		70		mA	7

V_{START} SECTION (pin 15)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit	Fig.
V_{15}	Reference Voltage		11.4	12	12.6	V	7
ΔV_{15}	Line Regulation	V_i = 15 to 50V		0.6	1.4	V	7
ΔV_{15}	Load Regulation	I_{15} = 0 to 1mA		50	200	mV	7
$I_{15\ short}$	Short Circuit Current Limit	V_{15} = 0V		80		mA	7

ELECTRICAL CHARACTERISTICS (continued)

DC CHARACTERISTICS

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit	Fig.
V_{9on}	Turn-on Threshold		10	11	12	V	7A
$V_{9\ Hyst}$	Turn-off Hysteresys			1		V	7A
I_{9Q}	Quiescent Current	V_{12} = 0; S1 = D		13	19	mA	7A
I_{9OQ}	Operating Supply Current	V_{12} = 0; S1 = C; S2 = B		16	23	mA	7A
I_{7L}	Out Leak Current	V_i = 55V; S3 = A; V_{12} = 0			2	mA	7A

SOFT START

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit	Fig.
I_{12}	Soft Start Source Current	V_{12} = 3V; V_{11} = 0V	70	100	130	µA	7B
V_{12}	Output Saturation Voltage	I_{12} = 20mA; V_9 = 10V			1	V	7B
		I_{12} = 200µA; V_9 = 10V			0.7	V	7B

ERROR AMPLIFIER

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit	Fig.
V_{10H}	High Level Out Voltage	I_{10} = -100µA; S1 = C V_{11} = 4.7V	6			V	7C
V_{10L}	Low Level Out Voltage	I_{10} = +100µA; S1 = C V_{11} = 5.3V;			1.2	V	7C
I_{10H}	Source Output Current	V_{10} = 1V; S1 = E V_{11} = 4.7V	100	150		µA	7C
I_{10L}	Sink Output Current	V_{10} = 6V; S1 = D V_{11} = 5.3V	100	150		µA	7C
I_{11}	Input Bias Current	R_S = 10KΩ		0.4	3	µA	–
G_V	DC Open Loop Gain	V_{VCM} = 4V; R_S = 10Ω	60			dB	–
SVR	Supply Voltage Rejection	15 < V_i < 50V; R_S = 10Ω	60	80		dB	–
V_{OS}	Input Offset Voltage	R_S = 50Ω		2	10	mV	–

RAMP GENERATOR (pin 2)

Symbol	Parameter	Test Condition		Min.	Typ.	Max.	Unit	Fig.
V_2	Ramp Valley	S1 = C; S2 = B		1.2	1.5		V	7A
V_2	Ramp Peak	S1 = C	V_i = 15V		2.5		V	7A
		S2 = B	V_i = 45V		5.5		V	7A
I_2	Min. Ramp Current	S1 = A; I_1 = 100µA			270	300	µA	7A
I_2	Max. Ramp Current	S1 = A; I_1 = 1mA		2.4	2.7		mA	7A

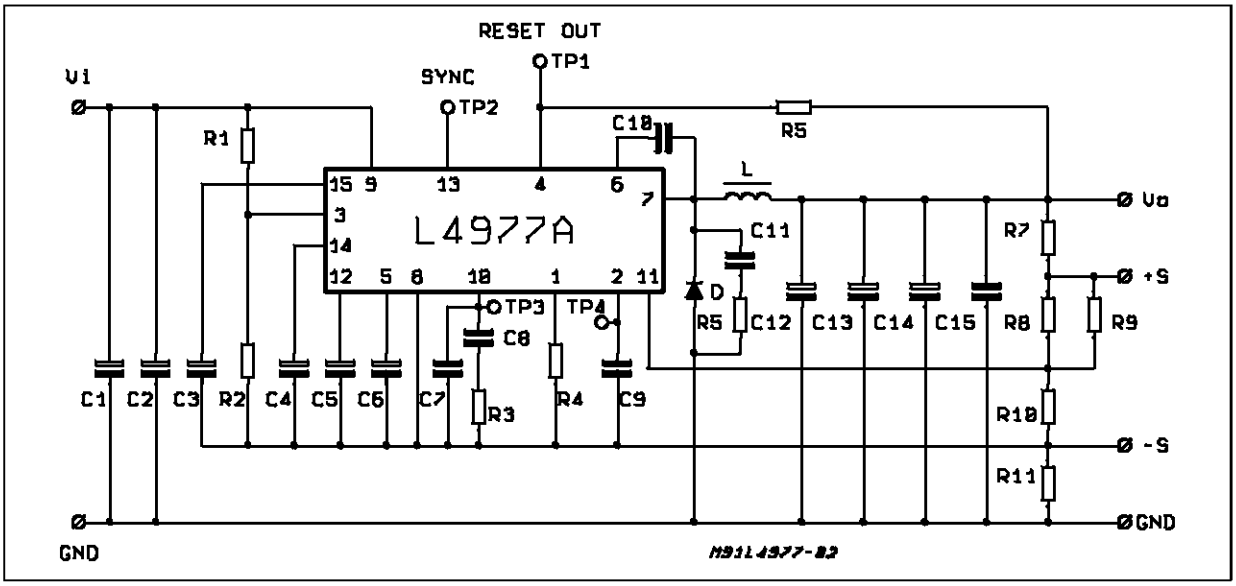
SYNC FUNCTION (pin 13)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit	Fig.
V_{13}	Low Input Voltage	V_i = 15V to 50V; V_{12} = 0; S1 = C; S2 = B; S4 = B	–0.3		0.9	V	7A
V_{13}	High Input voltage	V_{12} = 0; S1 = C; S2 = B; S4 = B	3.5		5.5	V	7A
I_{13L}	Sync Input Current with Low Input Voltage	V_{13} = V_2 = 0.9V; S4 = A; S1 = C; S2 = B			0.4	mA	7A
I_{13H}	Input Current with High Input Voltage	V_{13} = 3.5V; S4 = A; S1 = C; S2 = B			1.5	mA	7A
V_{13}	Output Amplitude		4	5		V	–
t_W	Output Pulse Width	V_{thr} = 2.5V	0.3	0.5	0.8	µs	–

ELECTRICAL CHARACTERISTICS (continued)
RESET AND POWER FAIL FUNCTIONS

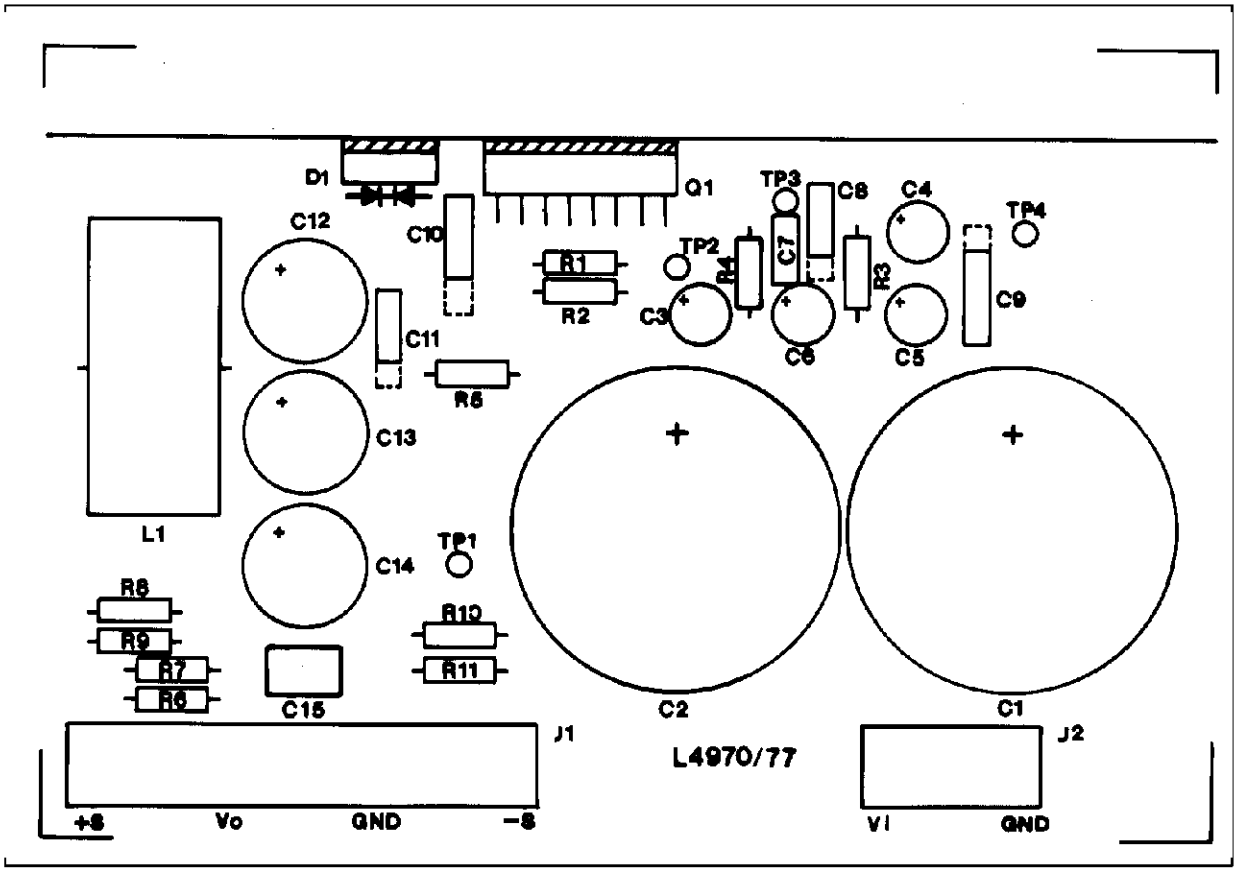
Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit	Fig.
V_{11R}	Rising Threshold Voltage (pin 11)	V_i = 15 to 50V V_3 = 5.3V	V_{ref} –120	V_{ref} –100	V_{ref} –80	V mV	7D
V_{11F}	Falling Threshold Voltage (pin 11)	Vi = 15 to 50V V_3 = 5.3V	4.77	V_{ref} –200	V_{ref} –160	V mV	7D
V_{5H}	Delay High Threshold Voltage	V_i = 15 to 50V V_{11} = V_{14} V_3 = 5.3V	4.95	5.1	5.25	V	7D
V_{5L}	Delay Low Threshold Voltage	Vi = 15 to 50V V_{11} = V_{14} V_3 = 5.3V	1	1.1	1.2	V	7D
$-I_{5SO}$	Delay Source Current	V_3 = 5.3V; V_5 = 3V	40	60	80	µA	7D
I_{5SI}	Delay Sink Current	V_3 = 4.7V; V_5 = 3V	10			mA	7D
V_{4S}	Out Saturation Voltage	I_4 = 15mA; S1 = B V_3 = 4.7V			0.4	V	7D
I_4	Output Leak Current	V_4 = 50V; S1 = A V_3 = 5.3V			100	µA	7D
V_{3R}	Rising Threshold Voltage	V_{11} = V_{14}	4.95	5.1	5.25	V	7D
V_{3H}	Hysteresys		0.4	0.5	0.6	V	7D
I_3	Input Bias Current			1	3	µA	7D

Figure 5: Test and Evaluation Board Circuit



TYPICAL PERFORMANCES (using evaluation board) :
n = 83% (V_i = 35V ; V_o = V_{REF} ; I_o = 7A ; f_{SW} = 200KHz)
$V_{o\ RIPPLE}$ = 30mV (at 7A) with output filter capacitor ESR ≤ 60mΩ
Line regulation = 5mV (V_i = 15 to 50V)
Load regulation = 15mV (I_o = 2 to 7A)
For component values, refer to test circuit part list.

Figure 6a: P.C. Board (components side) and Components Layout of Figure 5 (1:1 scale).



PARTS LIST

R_1 = 30KΩ	C_1, C_2 = 3300µF 63V_L EYF (ROE
R_2 = 10KΩ	C_3, C_4, C_5, C_6 = 2.2µF
R_3 = 15KΩ	C_7 = 390pF Film
R_4 = 16KΩ	C_8 = 22nF MKT 1817 (ERO)
R_5 = 22Ω 0,5W	
R_6 = 4K7	C_9 = 2.2nF KP1830
R_7 = 10Ω	C_{10} = 220nF MKT
R_8 = see tab. A	C_{11} = 2.2nF MP1830
R_9 = OPTION	**C_{12}, C_{13}, C_{14} = 220µF 40V_L EKR
R_{10} = 4K7	C_{15} = 1µF Film
R_{11} = 10Ω	
D1 = MBR 1560CT (or 16A/60V or equivalent)	
L1 = 40µH	core 58071 MAGNETICS 27 TURNS Ø 1,3mm (AWG 16) COGEMA 949178

* 2 capacitors in parallel to increase input RMS current capability
** 3 capacitors in parallel to reduce total output ESR

Table A

V_0	R_9	R_7
12V	4.7kΩ	6.2kW
15V	4.7kΩ	9.1kΩ
18V	4.7kΩ	12kΩ
24V	4.7kΩ	18kΩ

Table B
SUGGESTED BOOTSTRAP CAPACITORS

Operating Frequency	Bootstrap Cap.c10
f = 20KHz	≥680nF
f = 50KHz	≥470nF
f = 100KHz	≥330nF
f = 200KHz	≥220nF
f = 500KHz	≥100nF

Figure 6b: P.C. Board (Back side) and Components Layout of the Circuit of Fig. 5. (1:1 scale)

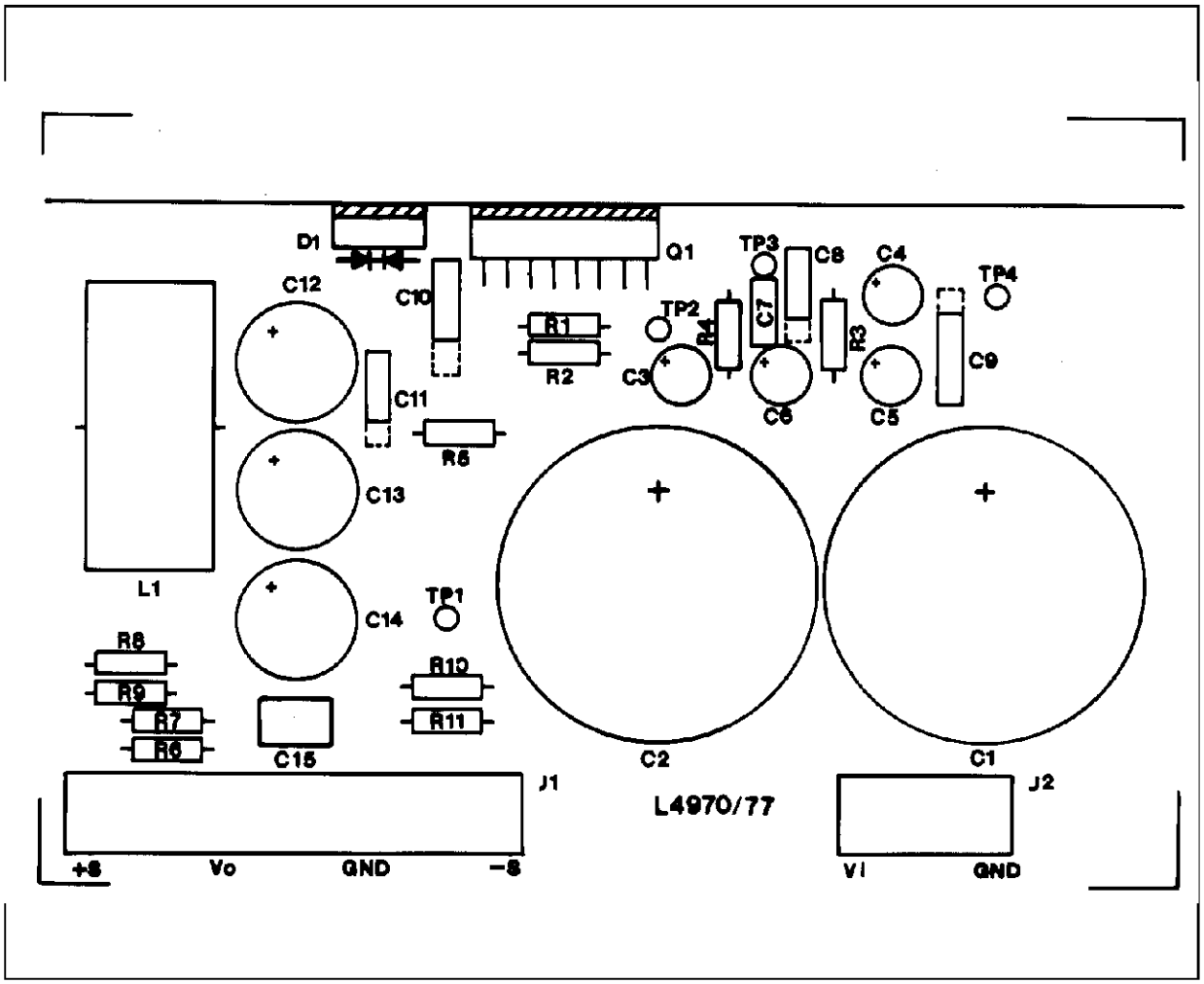


Figure 7: DC Test Circuits

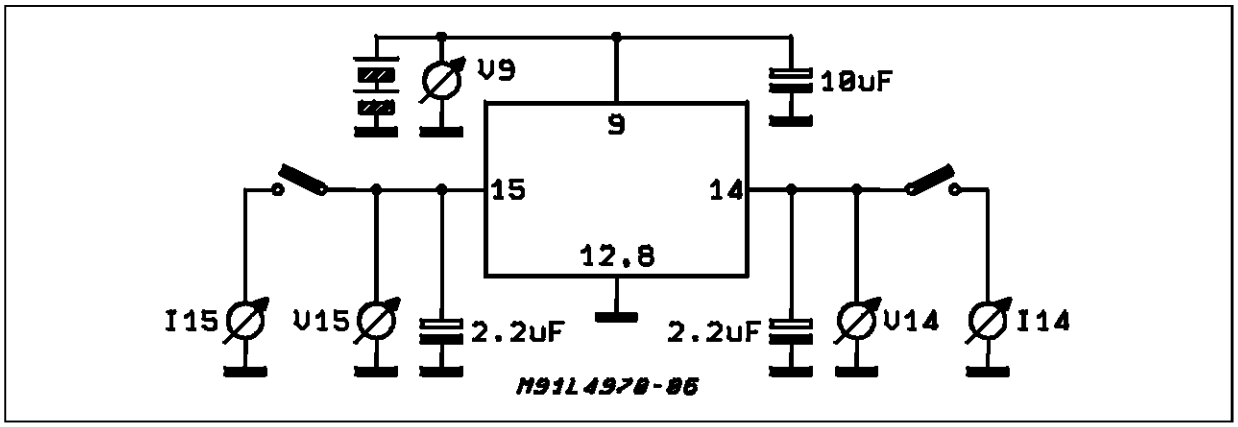


Figure 7A

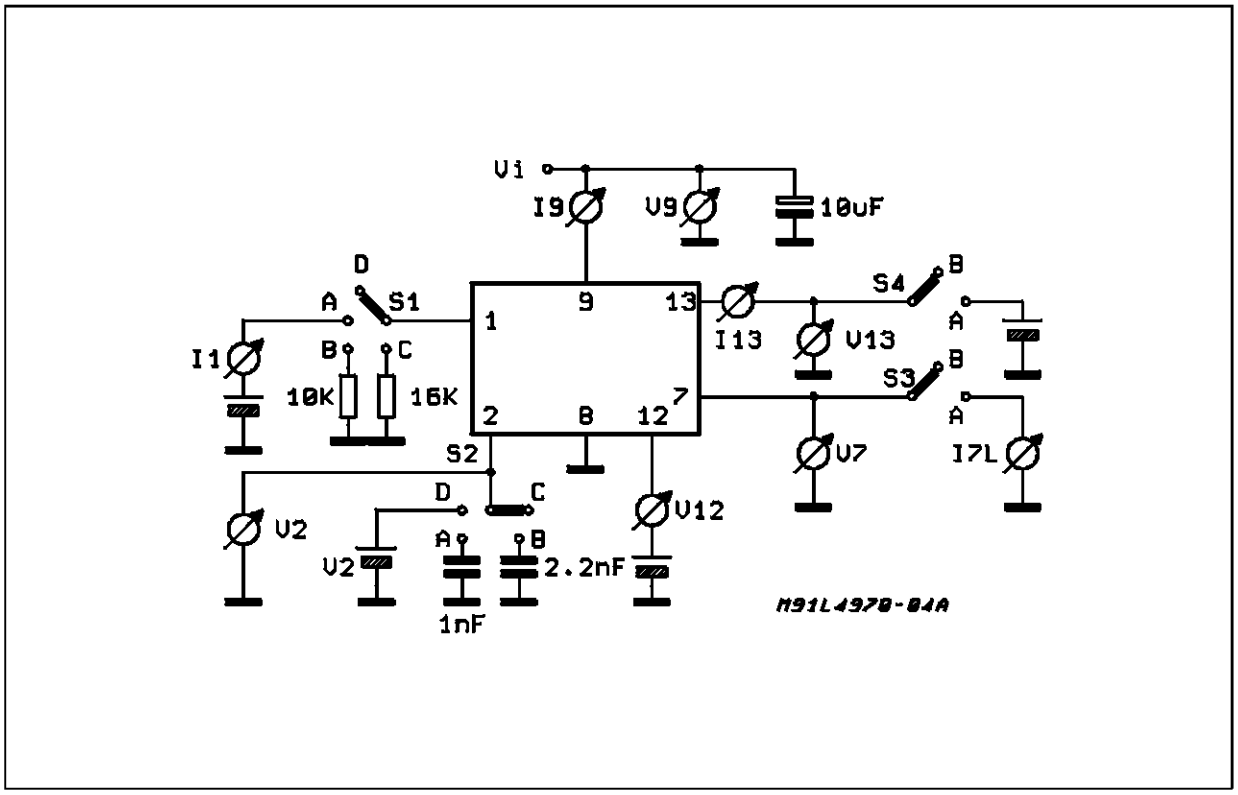


Figure 7B

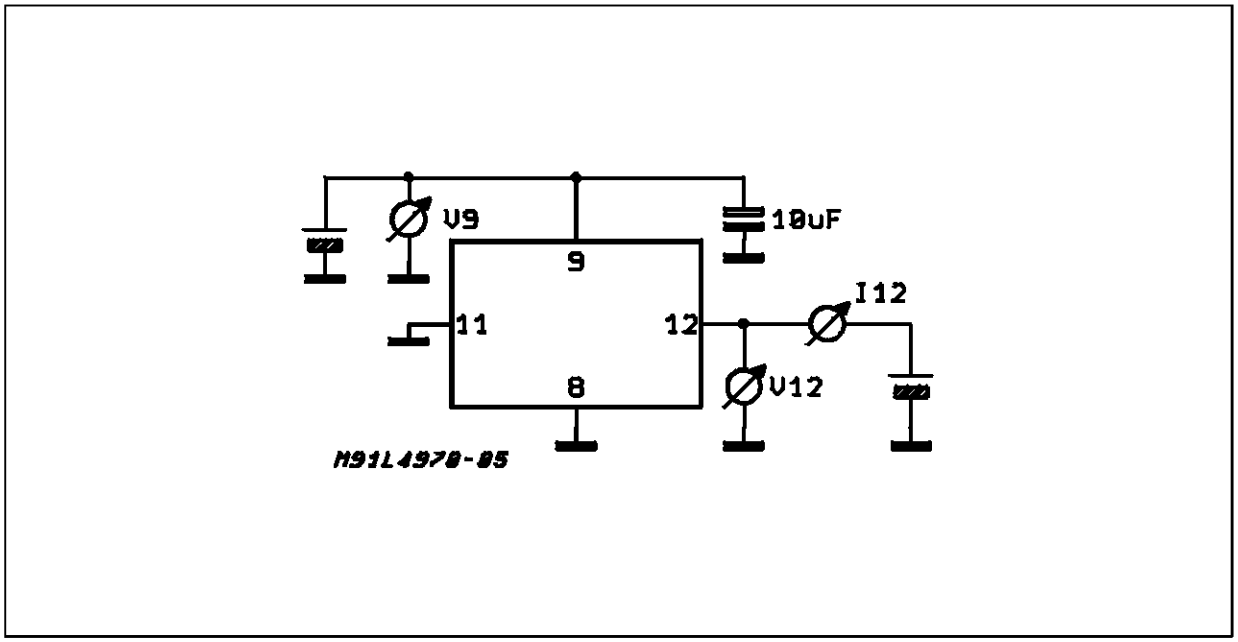


Figure 7D

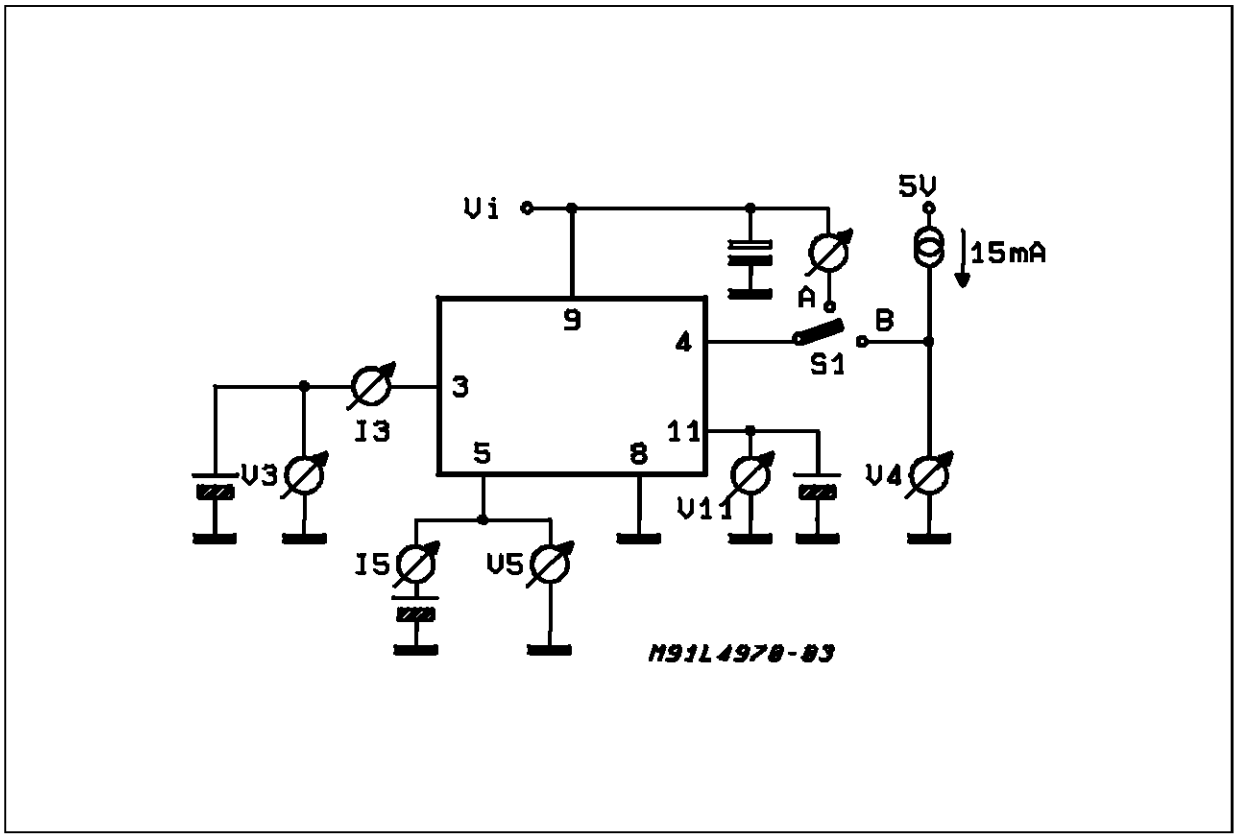


Figure 7C

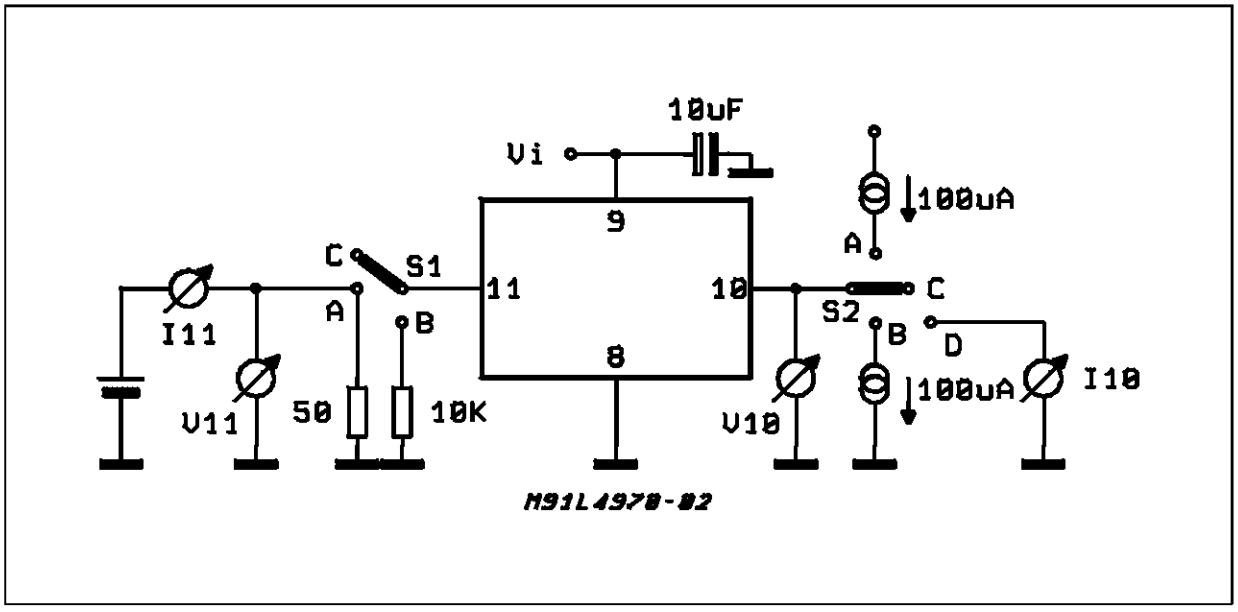


Figure 8: Quiescent Drain Current vs. Supply Voltage (0% duty cycle - see fig. 7A).

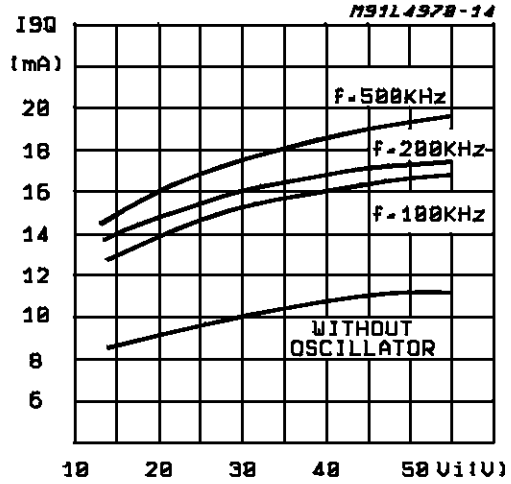


Figure 9: Quiescent Drain Current vs. Junction Temperature (0% duty cycle).

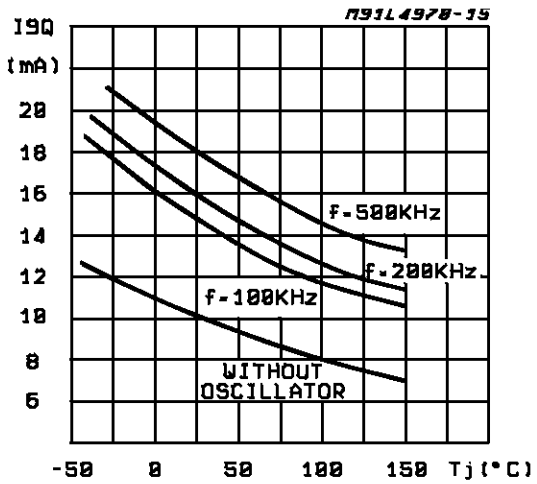


Figure 10: Quiescent Drain Current vs. Duty Cycle

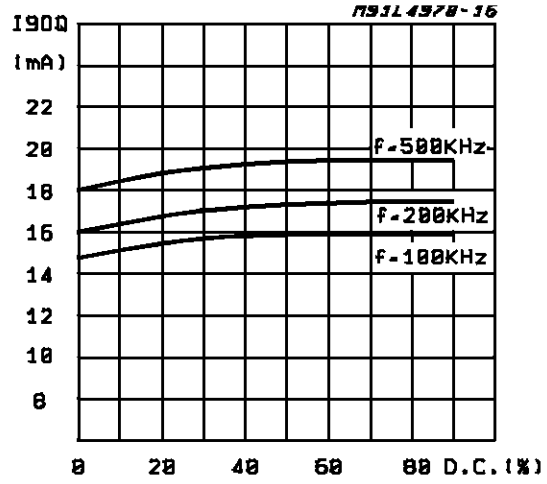


Figure 11: Reference Voltage (pin14) vs. V_i (see fig. 7)

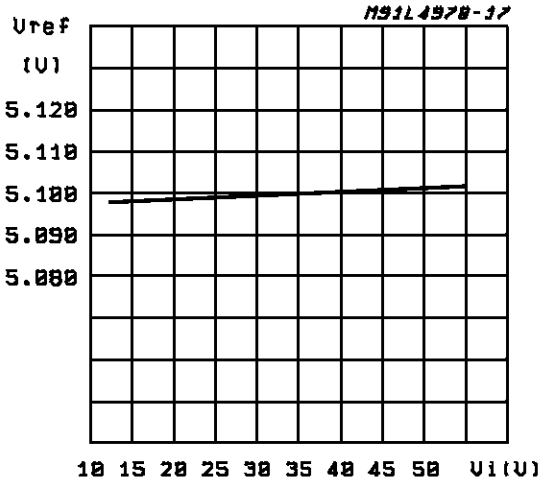


Figure 12: Reference Voltage (pin 14) vs. Junction Temperature (see fig. 7)

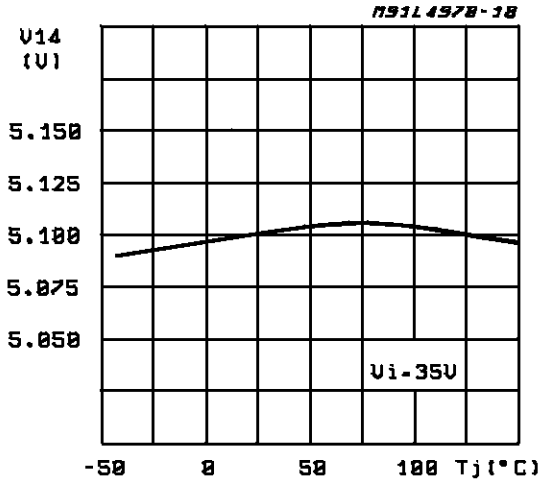


Figure 13: Reference Voltage (pin15) vs. V_i (see fig. 7)

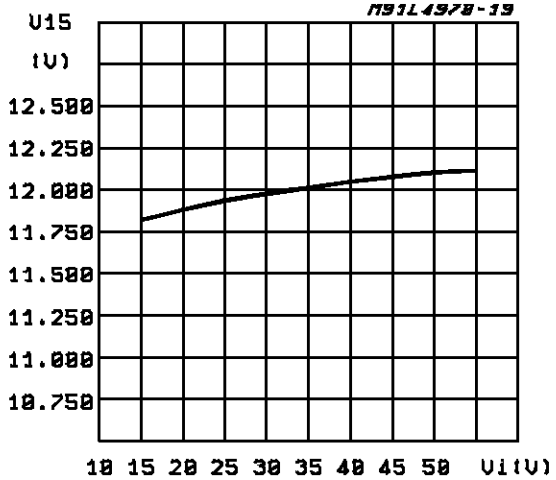


Figure 14: Reference Voltage (pin 15) vs. Junction Temperature (see fig. 7)

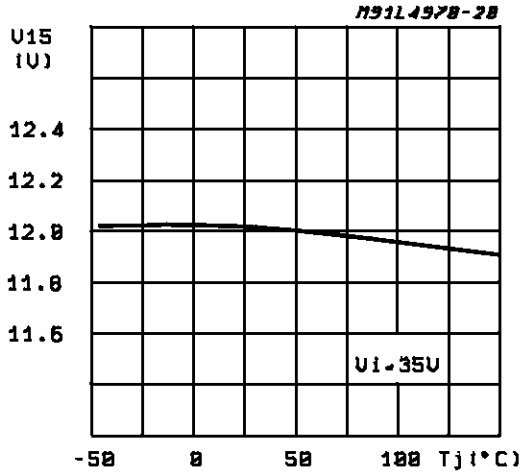


Figure 15: Reference Voltage 5.1V (pin 14) Supply Voltage Ripple Rejection vs. Frequency

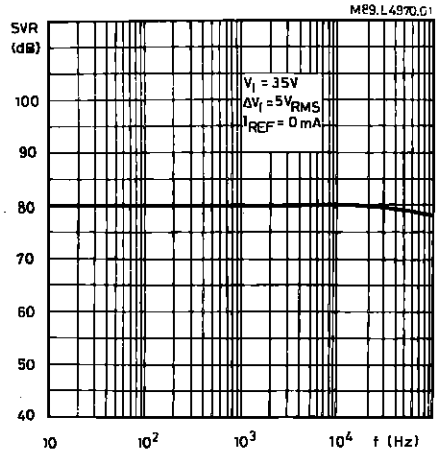


Figure 16: Switching Frequency vs. Input Voltage (see fig. 5)

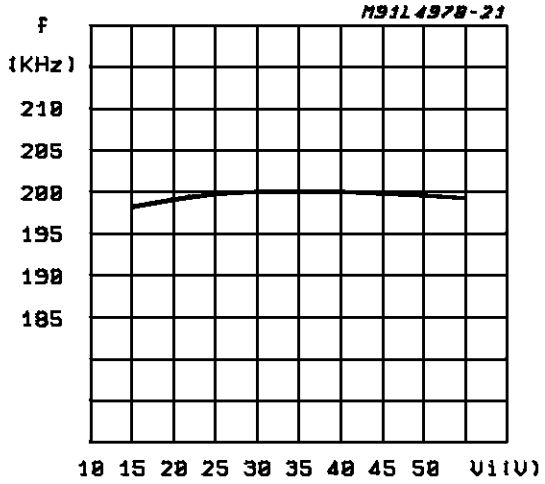


Figure 17: Switching Frequency vs. Junction Temperature (see fig 5)

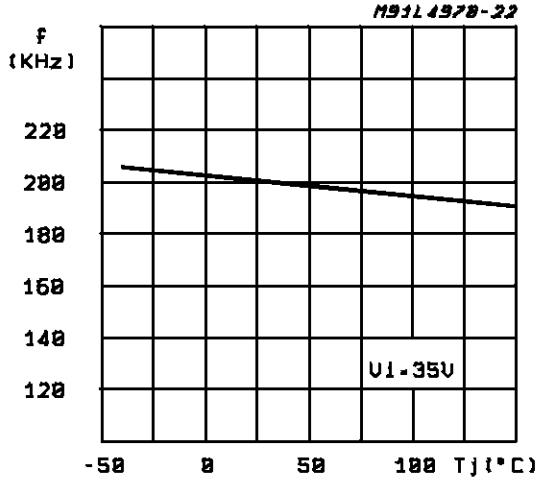


Figure 18: Switching Frequency vs. R4 (see fig. 5)

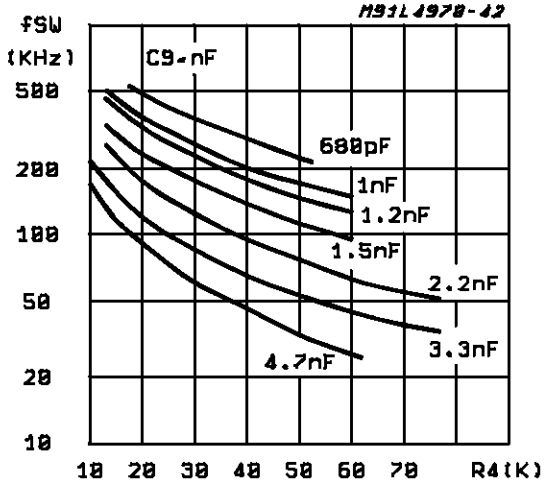


Figure 19: Max. Duty Cycle vs. Frequency

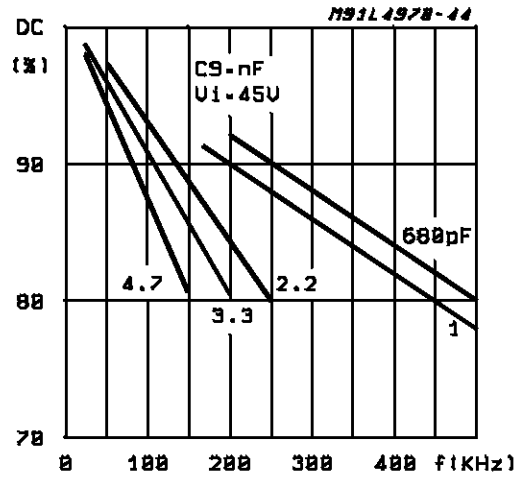


Figure 20: Supply Voltage Ripple Rejection vs. Frequency (see fig. 5)

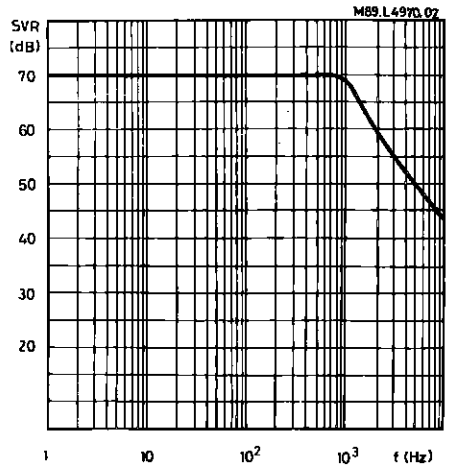


Figure 21: Line Transient Response (see fig. 5)

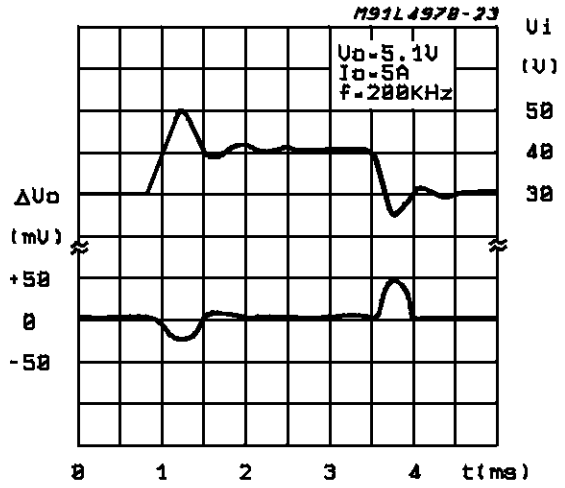


Figure 22: Load Transient Response (see fig. 5)

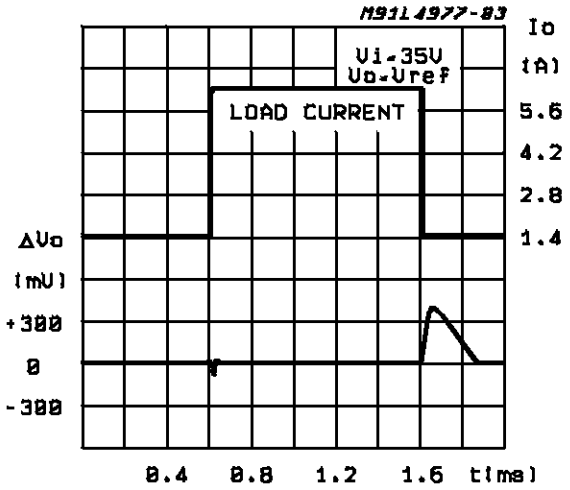


Figure 23: Dropout Voltage Between Pin 9 and Pin 7 vs. Current at Pin 7

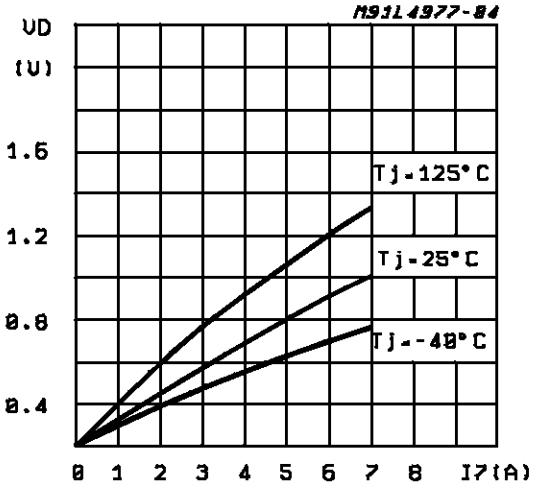


Figure 24: Dropout Voltage Between Pin 9 and Pin 7 vs. Junction Temperature

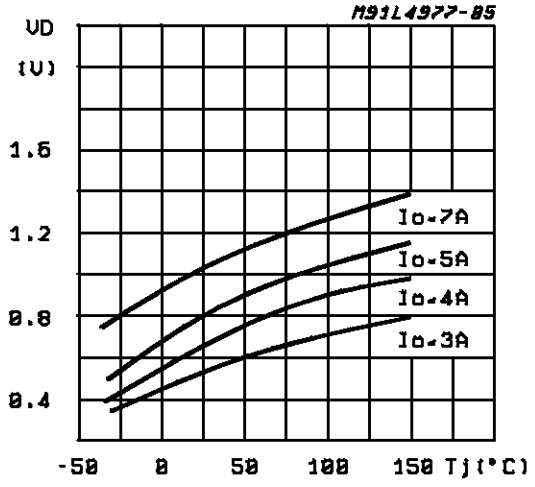


Figure 25: Power Dissipation (device only) vs. Input Voltage

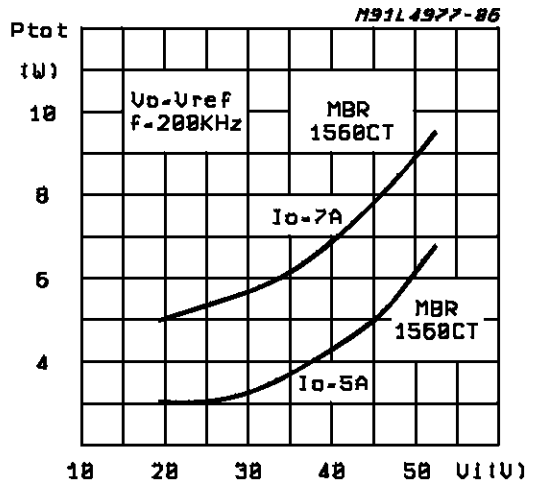


Figure 26: Power Dissipation (device only) vs. Output Voltage

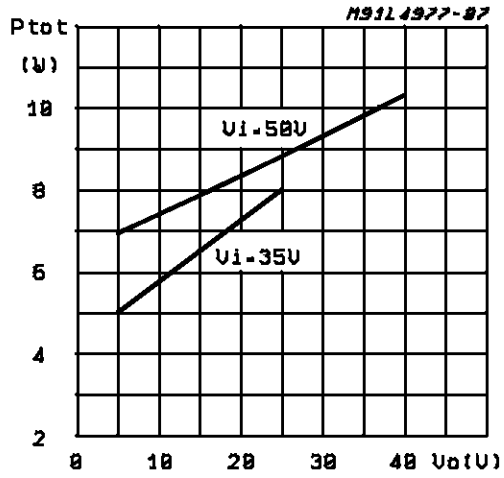


Figure 27: Heatsink Used to Derive the Device's Power Dissipation

$$R_{th}\text{ - Heatsink} = \frac{T_{case} - T_{amb}}{P_d}$$

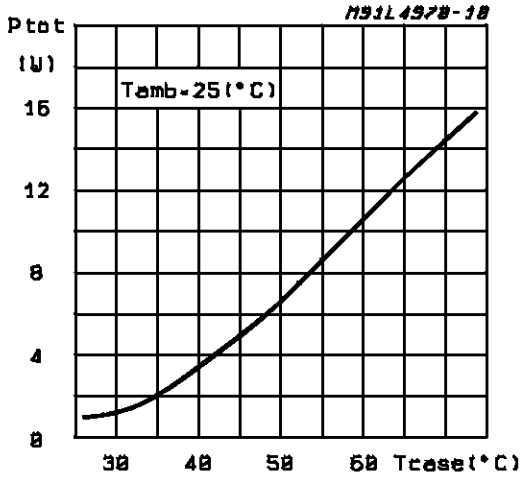


Figure 28: Efficiency vs. Output Current

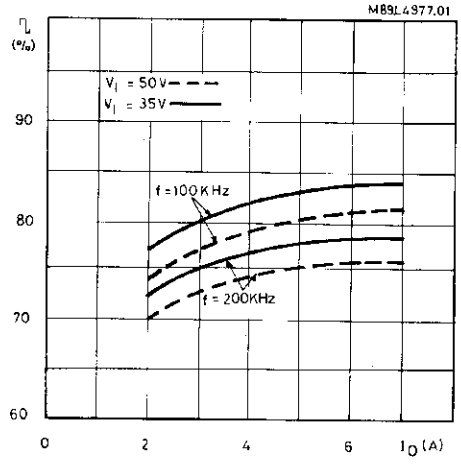


Figure 29: Efficiency vs. Output Voltage

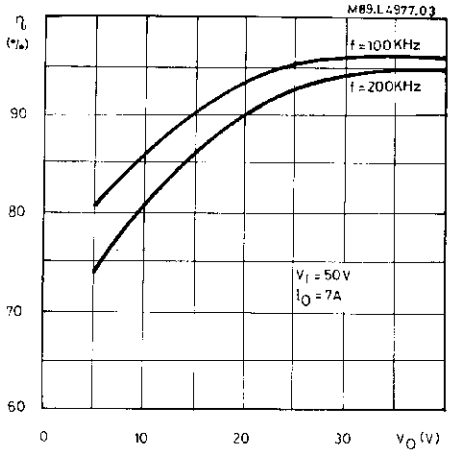


Figure 30: Efficiency vs. Output Voltage

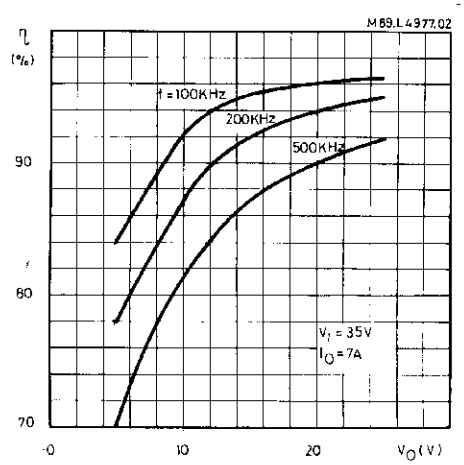


Figure 31: Open Loop Frequency and Phase Response of Error Amplifier (see fig.7C)

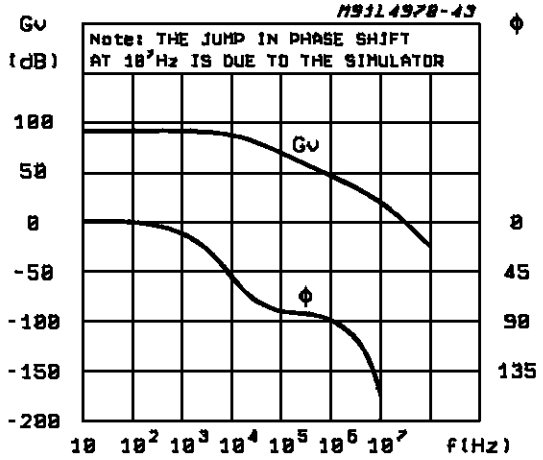


Figure 32: Power Dissipation Derating Curve

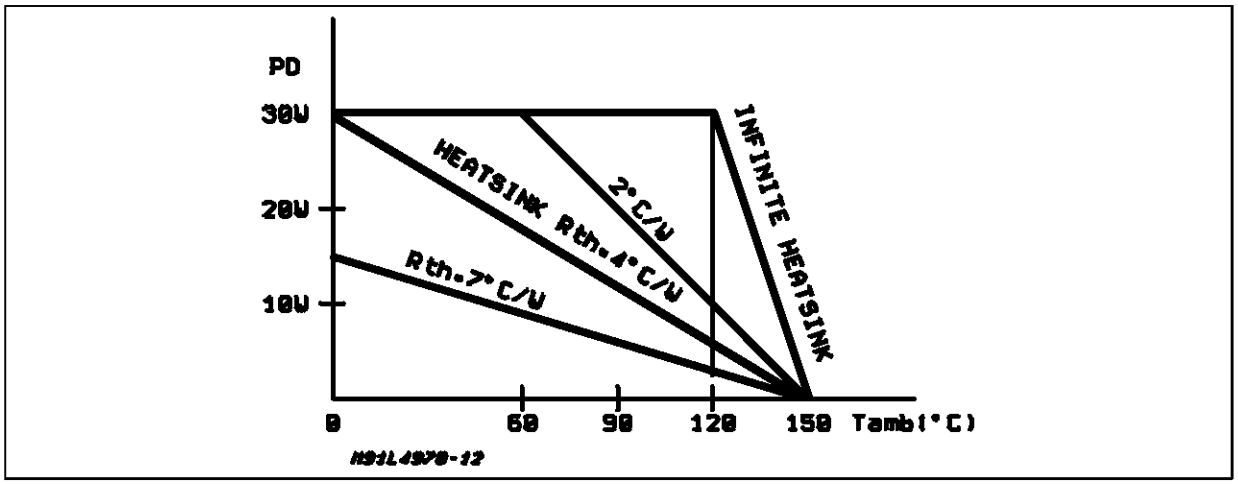


Figure 33: A5.1V/12V Multiple Supply. Note the Synchronization between the L4977A and the L4974A

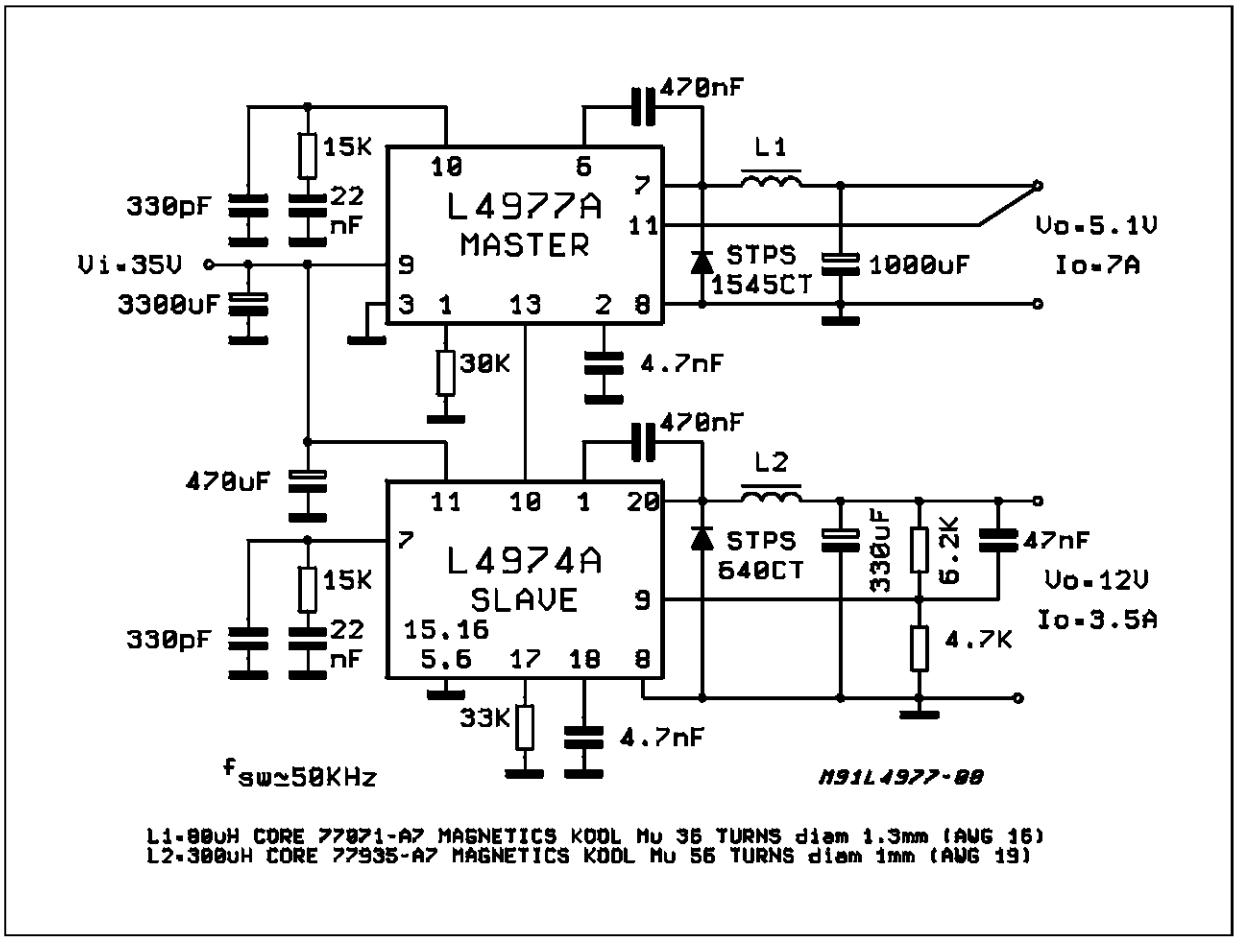


Figure 34: 5.1V / 7A Low Cost Application

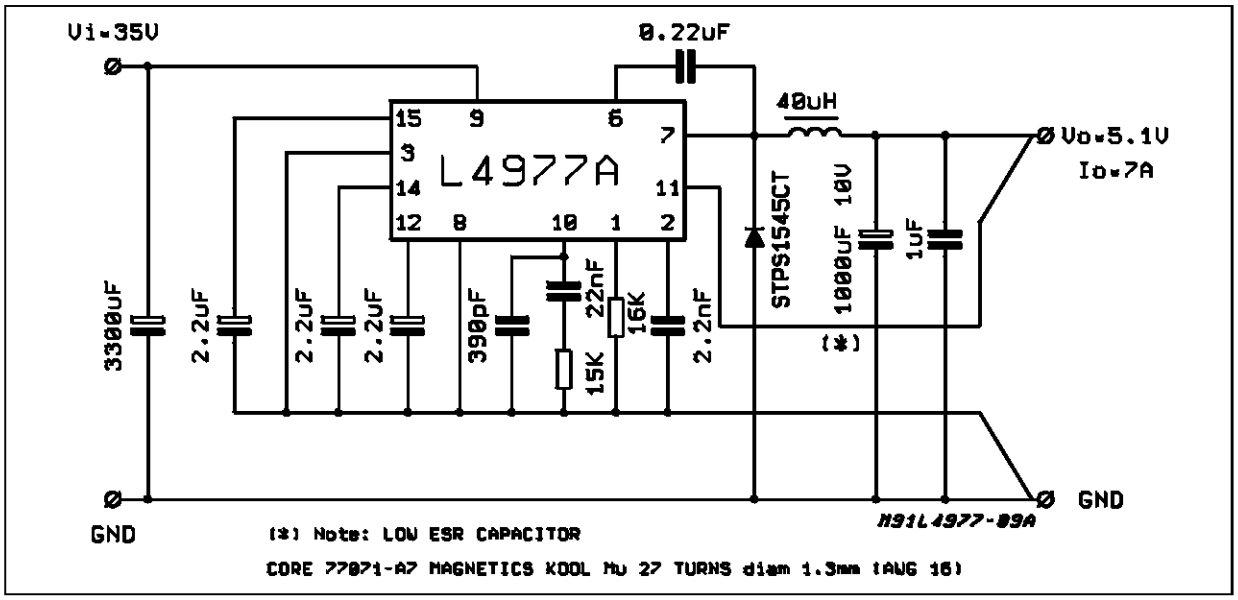


Figure 35: 7A Switching Regulator, Adjustable from 0V to 25V.

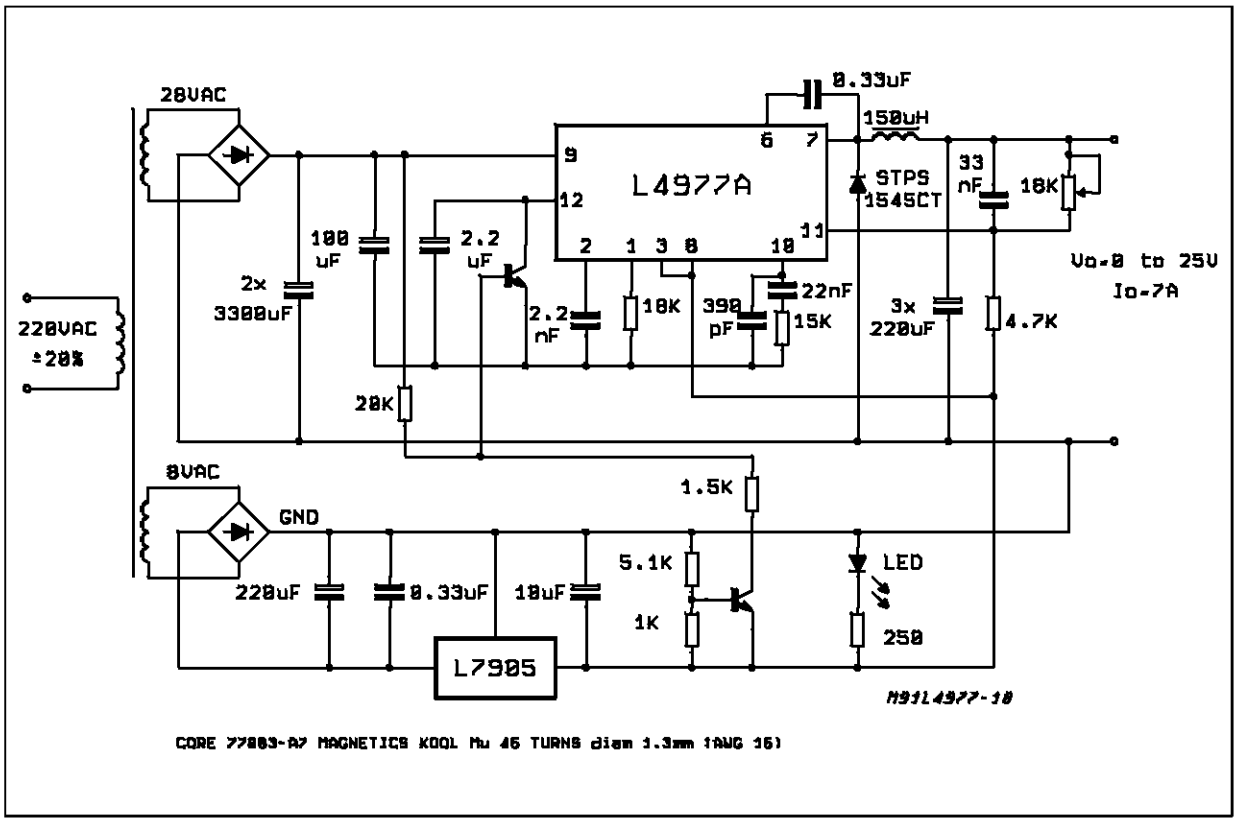
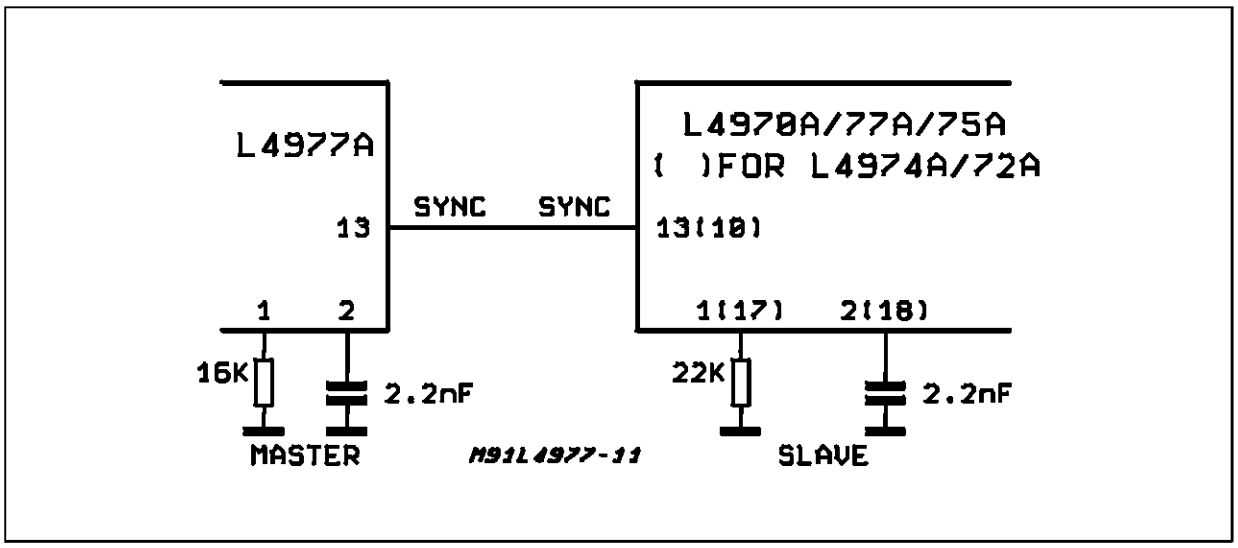
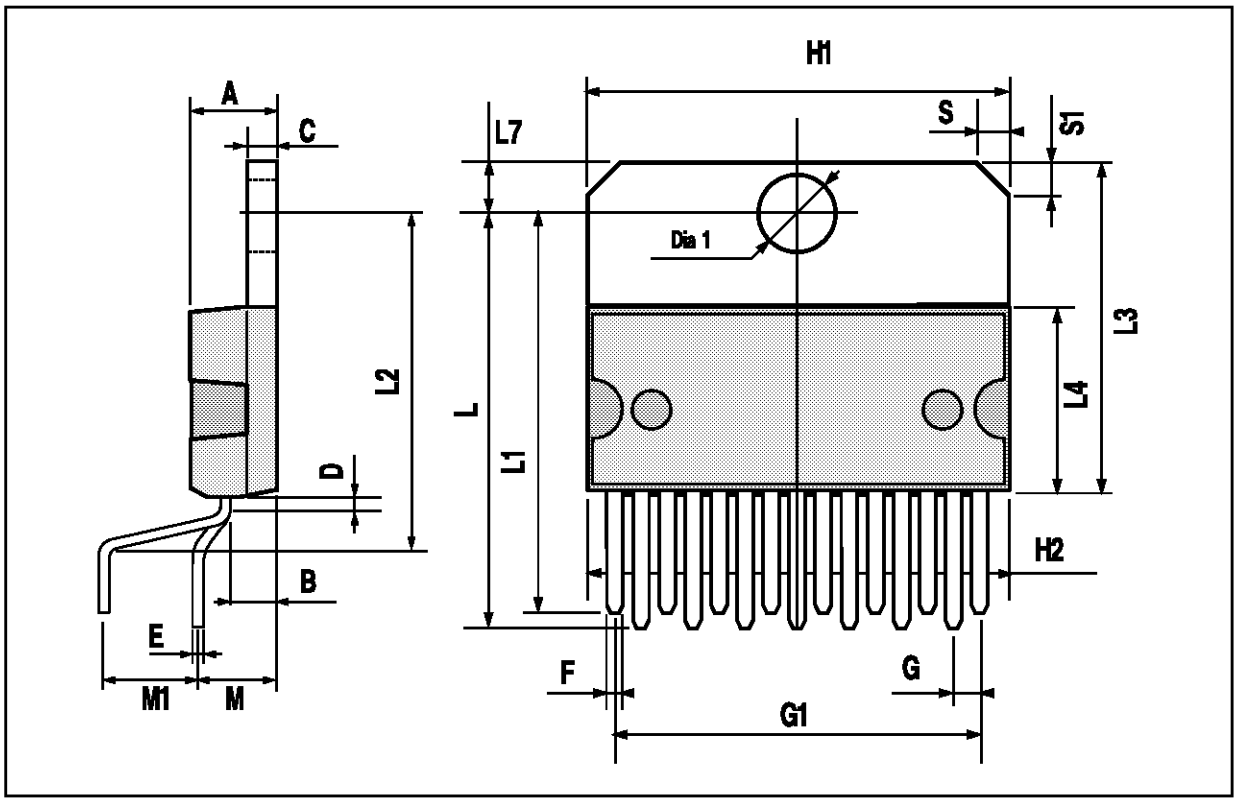


Figure 36: L4977A's Sync. Example



MULTIWATT15 PACKAGE MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			5			0.197
B			2.65			0.104
C			1.6			0.063
D		1			0.039	
E	0.49		0.55	0.019		0.022
F	0.66		0.75	0.026		0.030
G	1.14	1.27	1.4	0.045	0.050	0.055
G1	17.57	17.78	17.91	0.692	0.700	0.705
H1	19.6			0.772		
H2			20.2			0.795
L	22.1		22.6	0.870		0.890
L1	22		22.5	0.866		0.886
L2	17.65		18.1	0.695		0.713
L3	17.25	17.5	17.75	0.679	0.689	0.699
L4	10.3	10.7	10.9	0.406	0.421	0.429
L7	2.65		2.9	0.104		0.114
M	4.2	4.3	4.6	0.165	0.169	0.181
M1	4.5	5.08	5.3	0.177	0.200	0.209
S	1.9		2.6	0.075		0.102
S1	1.9		2.6	0.075		0.102
Dia1	3.65		3.85	0.144		0.152

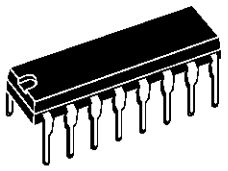


SGS-THOMSON MICROELECTRONICS

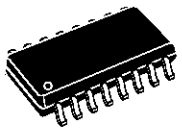
SG2525A/2527A SG3525A/3527A

REGULATING PULSE WIDTH MODULATORS

- 8 TO 35 V OPERATION
- 5.1 V REFERENCE TRIMMED TO ± 1 %
- 100 Hz TO 500 KHz OSCILLATOR RANGE
- SEPARATE OSCILLATOR SYNC TERMINAL
- ADJUSTABLE DEADTIME CONTROL
- INTERNAL SOFT-START
- PULSE-BY-PULSE SHUTDOWN
- INPUT UNDERVOLTAGE LOCKOUT WITH HYSTERESIS
- LATCHING PWM TO PREVENT MULTIPLE PULSES
- DUAL SOURCE/SINK OUTPUT DRIVERS



DIP16

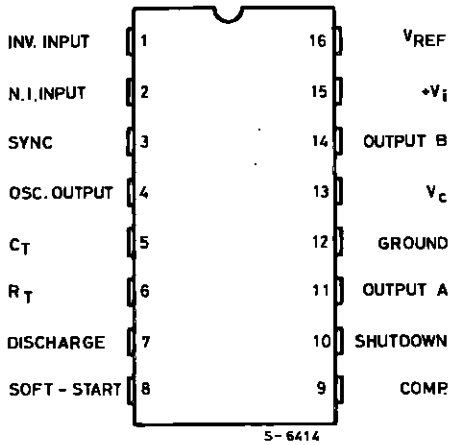


16(Narrow)

DESCRIPTION

The SG3525A/3527Aseries of pulse width modulator integrated circuits are designed to offer improved performance and lowered external parts count when used in designing all types of switching power supplies. The on-chip + 5.1 V reference is trimmed to ± 1 % and the input common-mode range of the error amplifier includes the reference voltage eliminating external resistors. A sync input to the oscillator allows multiple units to be slaved or a single unit to be synchronized to an external system clock. A single resistor between the C_T and the discharge terminals provide a wide range of dead time ad- justment. These devices also feature built-in soft-start circuitry with only an external timing capacitor required. A shutdown terminal controls both the soft-start circuity and the output stages, providing instantaneous turn off through the PWM latch with pulsed shutdown, as well as soft-start recycle with longer shutdown commands. These functions are also controlled by an undervoltage lockout which keeps the outputs off and the soft-start capacitor discharged for sub-normal input voltages. This lockout circuitry includes approximately 500 mV of hysteresis for jitter-free operation. Another feature of these PWM circuits is a latch following the comparator. Once a PWM pulses has been terminated for any reason, the outputs will remain off for the duration of the period. The latch is reset with each clock pulse. The output stages are totem-pole designs capable of sourcing or sinking in excess of 200 mA. The SG3525A output stage features NOR logic, giving a LOW output for an OFF state. The SG3527A utilizes OR logic which results in a HIGH output level when OFF.

PIN CONNECTIONS AND ORDERING NUMBERS (top view)



Type	Plastic DIP	SO16
SG2525A	SG2525AN	SG2525AP
SG2527A	SG2527AN	SG2527AP
SG3525A	SG3525AN	SG3525AP
SG3527A	SG3527AN	SG3527AP

ABSOLUTE MAXIMUM RATINGS

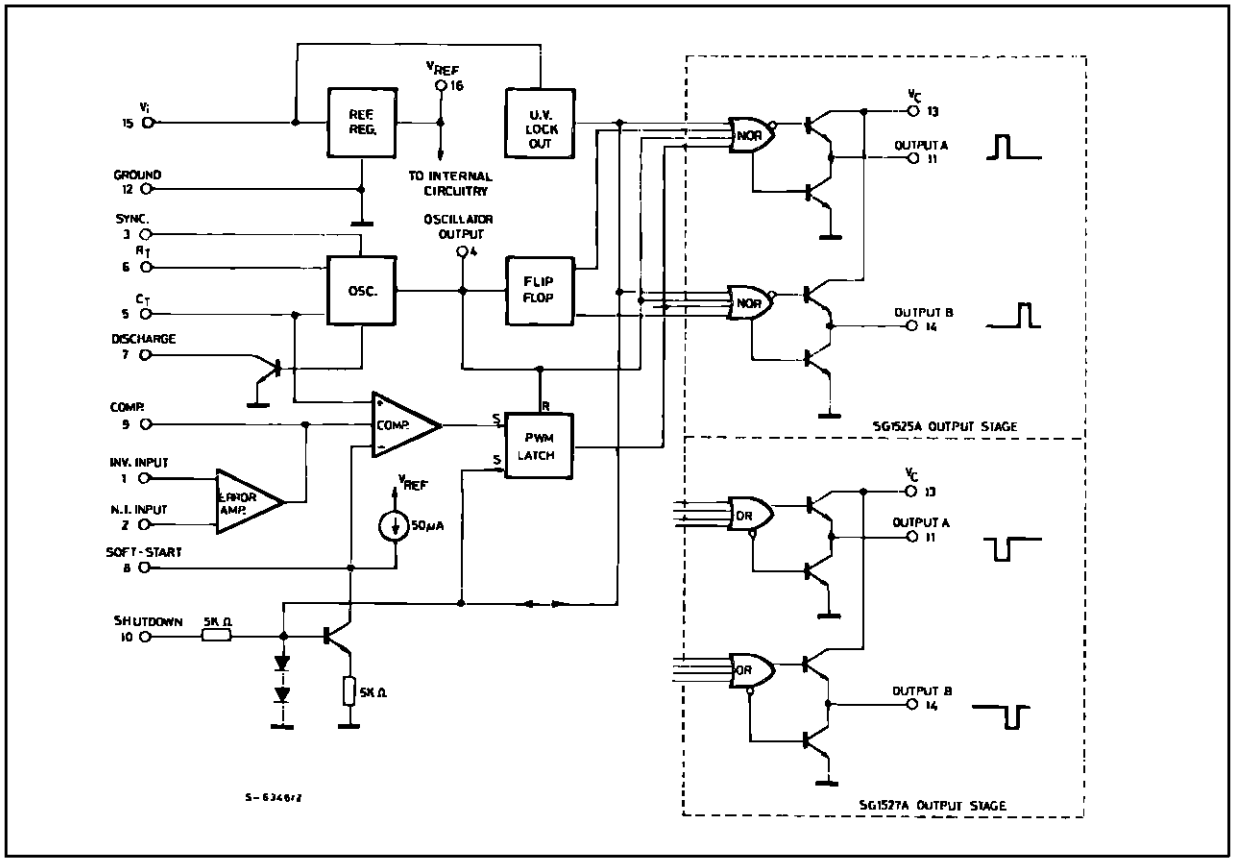
Symbol	Parameter	Value	Unit
V_i	Supply Voltage	40	V
V_C	Collector Supply Voltage	40	V
I_{OSC}	Oscillator Charging Current	5	mA
I_o	Output Current, Source or Sink	500	mA
I_R	Reference Output Current	50	mA
I_T	Current through C_T Terminal Logic Inputs Analog Inputs	5 – 0.3 to + 5.5 – 0.3 to V_i	mA V V
P_{tot}	Total Power Dissipation at T_{amb} = 70 °C	1000	mW
T_j	Junction Temperature Range	– 55 to 150	°C
T_{stg}	Storage Temperature Range	– 65 to 150	°C
T_{op}	Operating Ambient Temperature : **SG2525A/27A** **SG3525A/27A**	— 25 to 85 0 to 70	°C °C

THERMAL DATA

Symbol	Parameter		SO16	DIP16	Unit
$R_{th\ j\text{-}pins}$	Thermal Resistance Junction-pins	Max		50	°C/W
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient	Max		80	°C/W
$R_{th\ j\text{-}alumina}$	Thermal Resistance Junction-alumina (*)	Max	50		°C/W

* Thermal resistance junction-alumina with the device soldered on the middle of an alumina supporting substrate measuring 15× 20 mm ; 0.65 mm thickness with infinite heatsink.

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

(V# i = 20 V, and over operating temperature, unless otherwise specified)

Symbol	Parameter	Test Conditions	SG2525A SG2527A			SG3525A SG3527A			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
REFERENCE SECTION									
V_{REF}	Output Voltage	T_j = 25 °C	5.05	5.1	5.15	5	5.1	5.2	V
ΔV_{REF}	Line Regulation	V_i = 8 to 35 V		10	20		10	20	mV
ΔV_{REF}	Load Regulation	I_L = 0 to 20 mA		20	50		20	50	mV
$\Delta V_{REF}/\Delta T$*	Temp. Stability	Over Operating Range		20	50		20	50	mV
*	Total Output Variation	Line, Load and Temperature	5		5.2	4.95		5.25	V
	Short Circuit Current	V_{REF} = 0 T_j = 25 °C		80	100		80	100	mA
*	Output Noise Voltage	10 Hz ≤f ≤ 10 kHz, T_j = 25 °C		40	200		40	200	µVrms
ΔV_{REF}*	Long Term Stability	T_j = 125 °C, 1000 hrs		20	50		20	50	mV
OSCILLATOR SECTION * *									
*, •	Initial Accuracy	T_j = 25 °C		± 2	± 6		± 2	± 6	%
*, •	Voltage Stability	V_i = 8 to 35 V		± 0.3	± 1		± 1	± 2	%
$\Delta f/\Delta T$*	Temperature Stability	Over Operating Range		± 3	± 6		± 3	± 6	%
f_{MIN}	Minimum Frequency	R_T = 200 KΩ C_T = 0.1 µF			120			120	Hz
f_{MAX}	Maximum Frequency	R_T = 2 KΩ C_T = 470 pF	400			400			KHz
	Current Mirror	I_{RT} = 2 mA	1.7	2	2.2	1.7	2	2.2	mA
*, •	Clock Amplitude		3	3.5		3	3.5		V
*, •	Clock Width	T_j = 25 °C	0.3	0.5	1	0.3	0.5	1	µs
	Sync Threshold		1.2	2	2.8	1.2	2	2.8	V
	Sync Input Current	Sync Voltage = 3.5 V		1	2.5		1	2.5	mA
ERROR AMPLIFIER SECTION (V_{CM} = 5.1 V)									
V_{OS}	Input Offset Voltage			0.5	5		2	10	mV
I_b	Input Bias Current			1	10		1	10	µA
I_{os}	Input Offset Current				1			1	µA
	DC Open Loop Gain	R_L ≥ 10 MΩ	60	75		60	75		dB
*	Gain Bandwidth Product	G_v = 0 dB T_j = 25 °C	1	2		1	2		MHz
*, ⍰	DC Transconduct.	30 KΩ ≤ R_L ≤ 1 MΩ T_j = 25 °C	1.1	1.5		1.1	1.5		ms
	Output Low Level			0.2	0.5		0.2	0.5	V
	Output High Level		3.8	5.6		3.8	5.6		V
CMR	Comm. Mode Reject.	V_{CM} = 1.5 to 5.2 V	60	75		60	75		dB
PSR	Supply Voltage Rejection	V_i = 8 to 35 V	50	60		50	60		dB

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Conditions	SG2525A SG2527A			SG3525A SG3527A			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
PWM COMPARATOR									
	Minimum Duty-cycle				0			0	%
	Maximum Duty-cycle		45	49		45	49		%
•	Input Threshold	Zero Duty-cycle	0.7	0.9		0.7	0.9		V
		Maximum Duty-cycle		3.3	3.6		3.3	3.6	V
*	Input Bias Current			0.05	1		0.05	1	µA
SHUTDOWN SECTION									
	Soft Start Current	V_{SD} = 0 V, V_{SS} = 0 V	25	50	80	25	50	80	µA
	Soft Start Low Level	V_{SD} = 2.5 V		0.4	0.7		0.4	0.7	V
	Shutdown Threshold	To outputs, V_{SS} = 5.1 V T_j = 25 °C	0.6	0.8	1	0.6	0.8	1	V
	Shutdown Input Current	V_{SD} = 2.5 V		0.4	1		0.4	1	mA
*	Shutdown Delay	V_{SD} = 2.5 V T_j = 25 °C		0.2	0.5		0.2	0.5	µs
OUTPUT DRIVERS (each output) (V_C = 20 V)									
	Output Low Level	I_{sink} = 20 mA		0.2	0.4		0.2	0.4	V
		I_{sink} = 100 mA		1	2		1	2	V
	Output High Level	I_{source} = 20 mA	18	19		18	19		V
		I_{source} = 100 mA	17	18		17	18		V
	Under-Voltage Lockout	V_{comp} and V_{ss} = High	6	7	8	6	7	8	V
I_C	Collector Leakage	V_C = 35 V			200			200	µA
t_r*	Rise Time	C_L = 1 nF, T_j = 25 °C		100	600		100	600	ns
t_f*	Fall Time	C_L = 1 nF, T_j = 25 °C		50	300		50	300	ns
TOTAL STANDBY CURRENT									
I_S	Supply Current	V_i = 35 V		14	20		14	20	mA

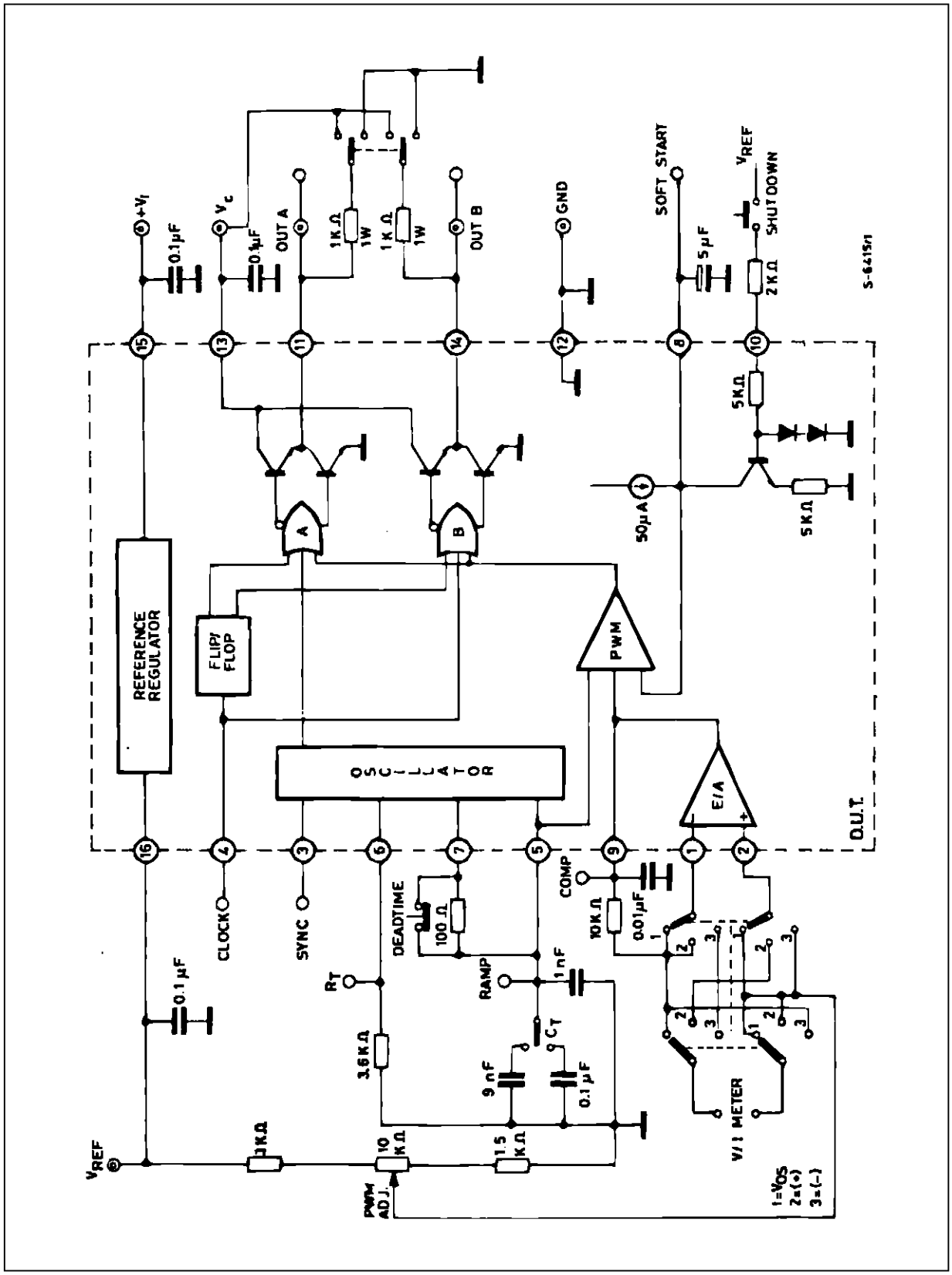
* These parameters, although guaranteed over the recommended operating conditions, are not 100 % tested in production.

• Tested at f_{osc} = 40 KHz (R_T = 3.6 KΩ, C_T = 0.1 µF, R_D = 0 Ω). Approximate oscillator frequency is defined by :

$$f = \frac{1}{C_T(0.7\ R_T + 3\ R_D)}$$

■ DC transconductance (g_M) relates to DC open-loop voltage gain (G_v) according to the following equation : $G_v = g_M\ R_L$ where R_L is the resistance from pin 9 to ground. The minimum g_M specification is used to calculate minimum G_v when the error amplifier output is loaded.

TEST CIRCUIT



RECOMMENDED OPERATING CONDITIONS (•)

Parameter	Value
Input Voltage (V_i)	8 to 35 V
Collector Supply Voltage (V_C)	4.5 to 35 V
Sink/Source Load Current (steady state)	0 to 100 mA
Sink/Source Load Current (peak)	0 to 400 mA
Reference Load Current	0 to 20 mA
Oscillator Frequency Range	100 Hz to 400 KHz
Oscillator Timing Resistor	2 KΩ to 150 KΩ
Oscillator Timing Capacitor	0.001 µF to 0.1 µF
Dead Time Resistor Range	0 to 500 Ω

(•) Range over which the device is functional and parameter limits are guaranteed.

Figure 1 : Oscillator Charge Time vs. R_T and C_T.

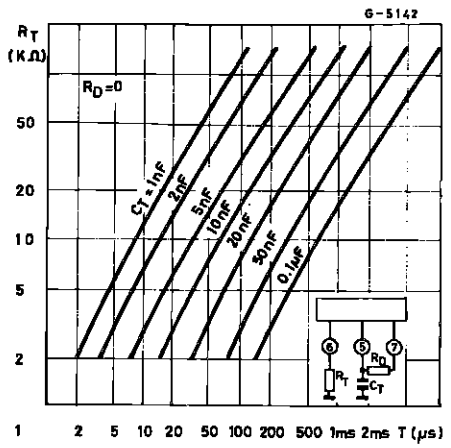


Figure 2 : Oscillator Discharge Time vs. R_D and C_T.

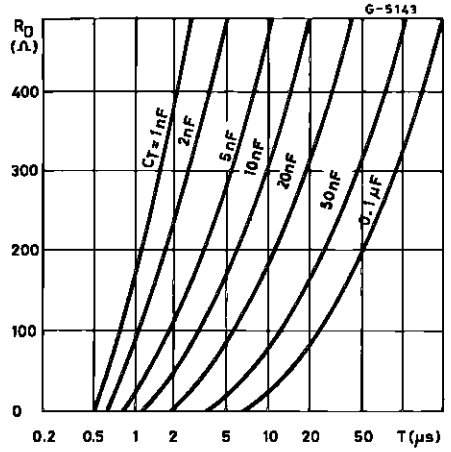


Figure 3 : SG1525A Output Saturation Characteristics.

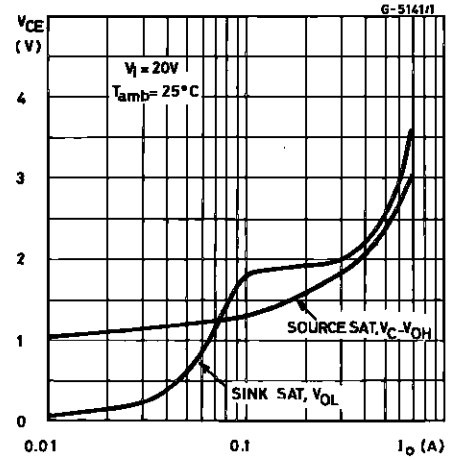


Figure 4 : Error Amplifier Voltage Gain and Phase vs. Frequency.

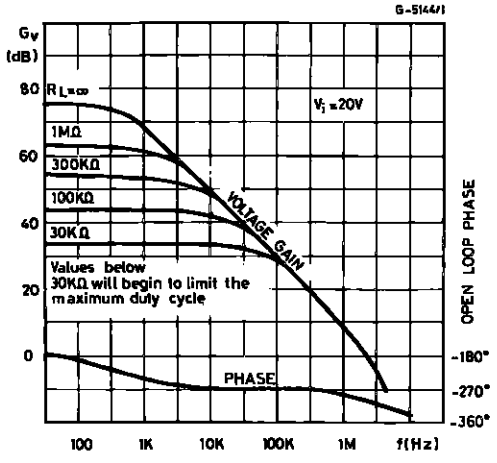
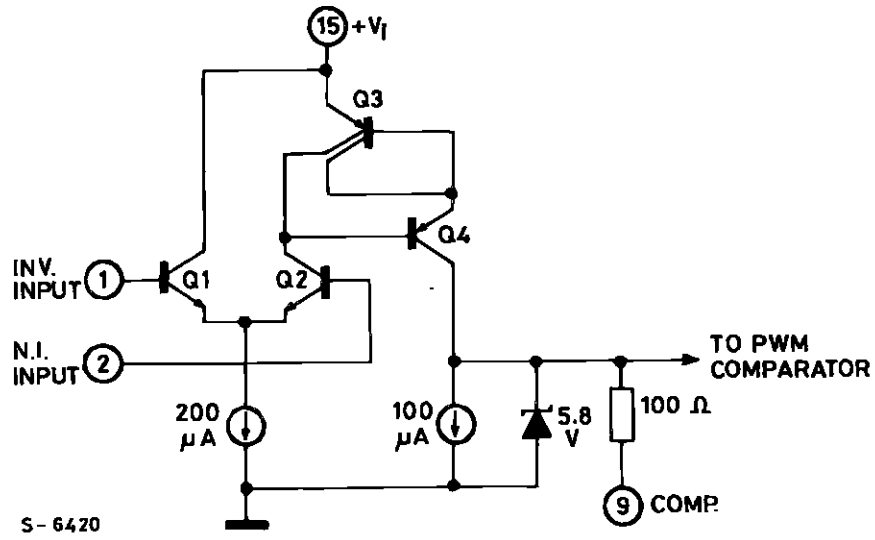


Figure 5 : SG1525A Error Amplifier.



PRINCIPLES OF OPERATION

SHUTDOWN OPTIONS (see Block Diagram)

Since both the compensation and soft-start terminals (Pins 9 and 8) have current source pull-ups, either can readily accept a pull-down signal which only has to sink a maximum of 100 µA to turn off the outputs. This is subject to the added requirement of discharging whatever external capacitance may be attached to these pins.

An alternate approach is the use of the shutdown circuitry of Pin 10 which has been improved to enhance the available shutdown options. Activating this circuit by applying a positive signal on Pin 10 performs two functions : the PWM latch is immediately set providing the fastest turn-off signal to the outputs ; and a 150 µA current sink begins to discharge the external soft-start capacitor. If the shutdown command is short, the PWM signal is terminated without significant discharge of the soft-start capacitor, thus, allowing, for example, a convenient implementation of pulse-by-pulse current limiting. Holding Pin 10 high for a longer duration, however, will ultimately discharge this external capacitor, recycling slow turn-on upon release.

Pin 10 should not be left floating as noise pickup could conceivably interrupt normal operation.

Figure 6 : SG1525A Oscillator Schematic.

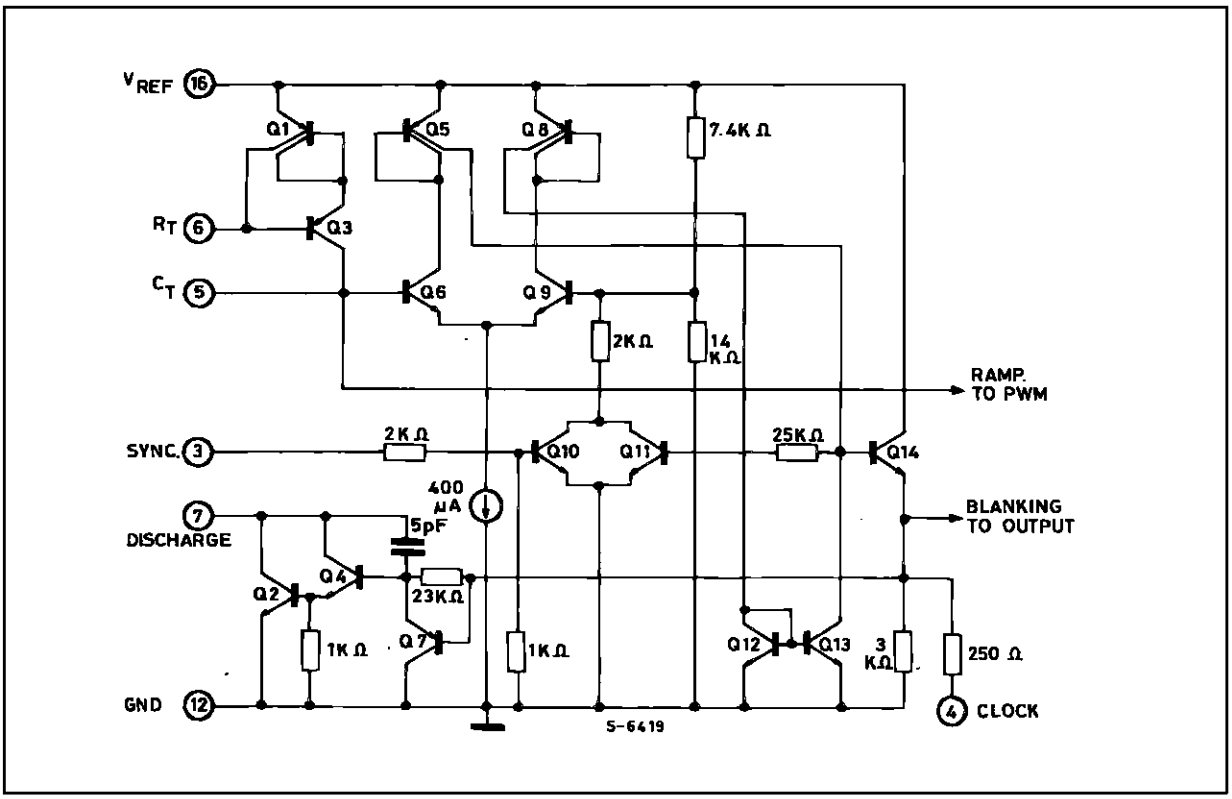


Figure 7 : SG1525A Output Circuit (1/2 circuit shown).

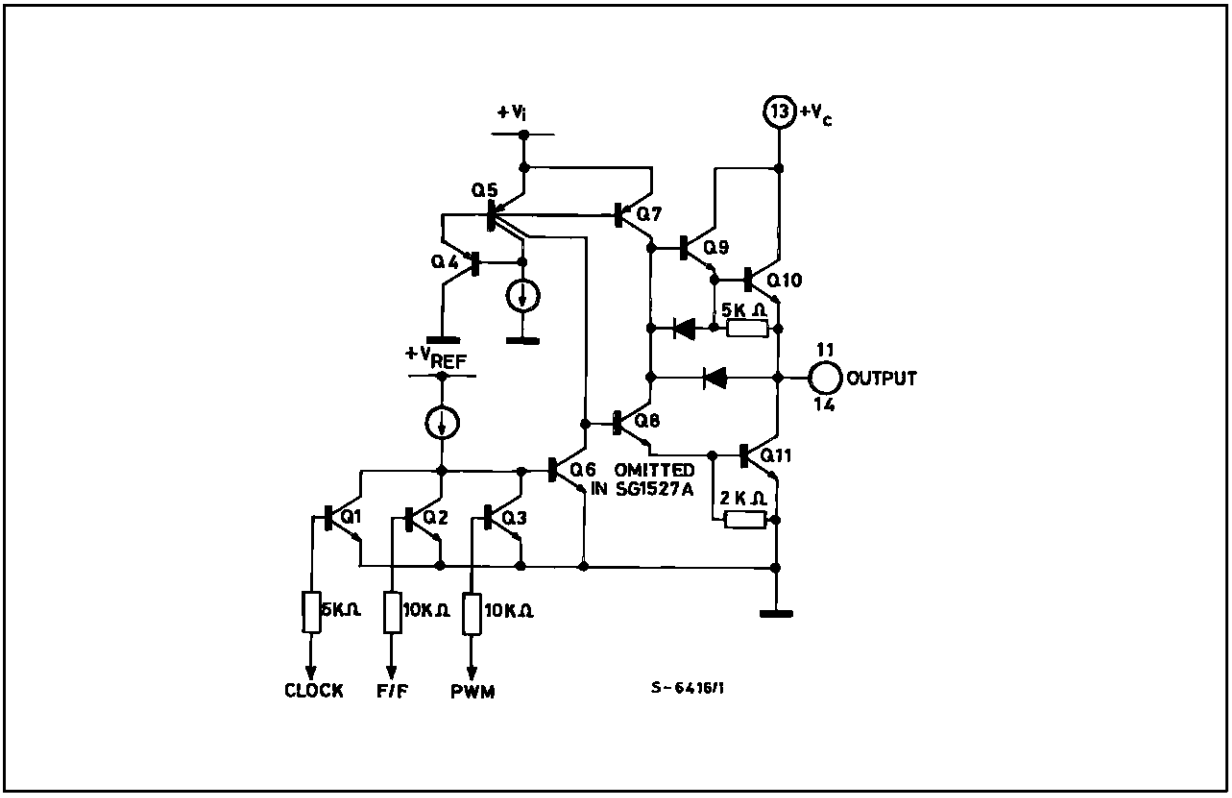
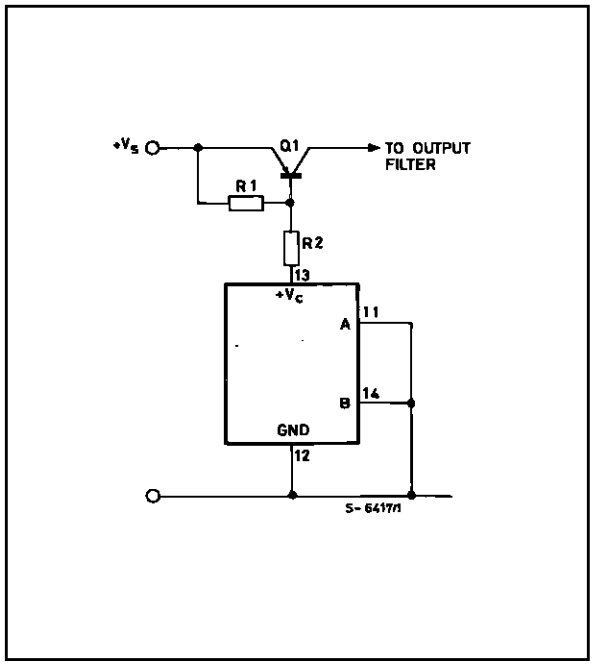
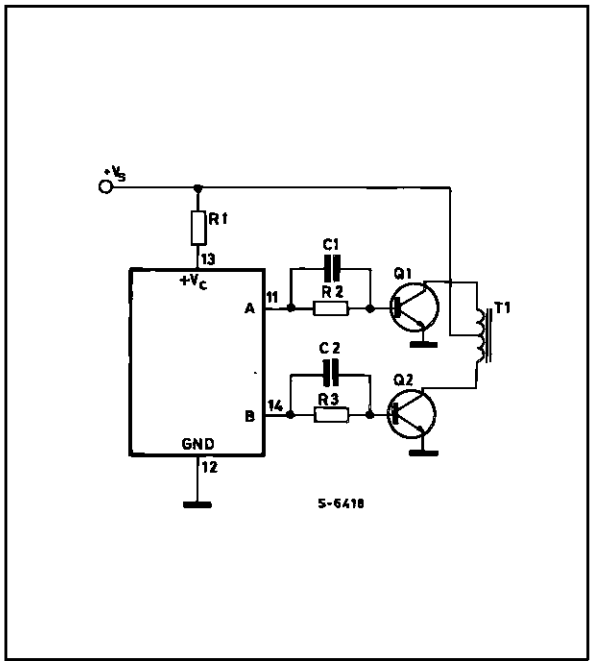


Figure 8.



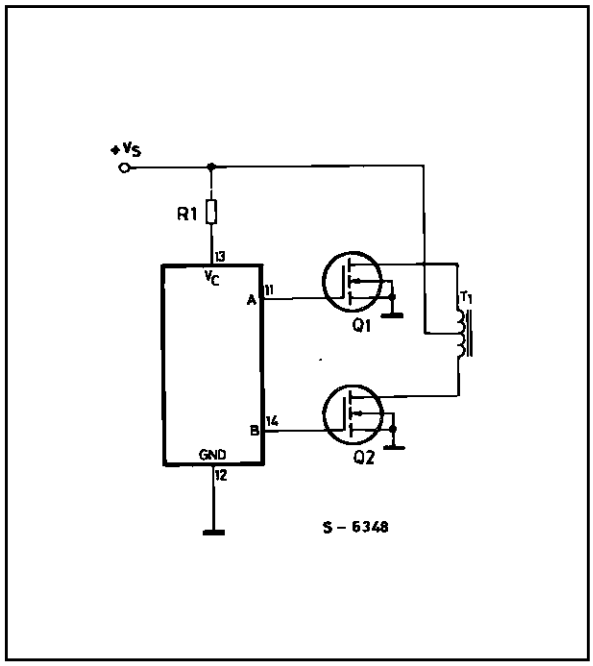
For single-ended supplies, the driver outputs are grounded. The V_C terminal is switched to ground by the totem-pole source transistors on alternate oscillator cycles.

Figure 9.



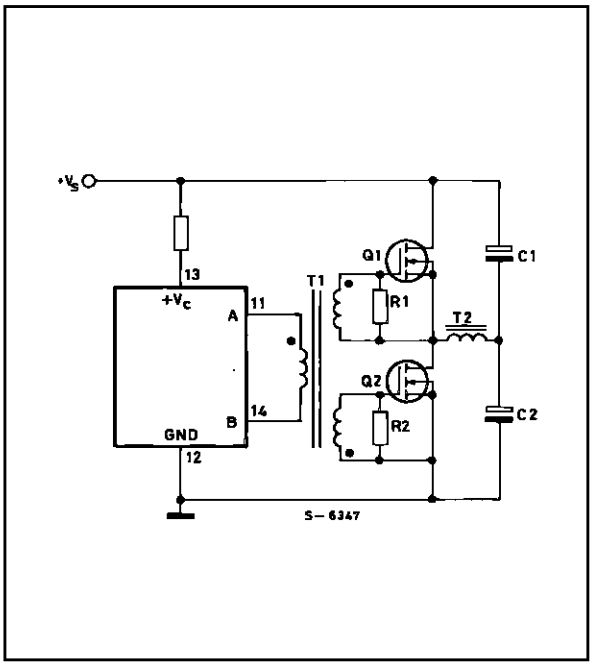
In conventional push-pull bipolar designs, forward base drive is controlled by R_1 - R_3. Rapid turn-off times for the power devices are achieved with speed-up capacitors C_1 and C_2.

Figure 10.



The low source impedance of the output drivers provides rapid charging of Power Mos input capacitance while minimizing external components.

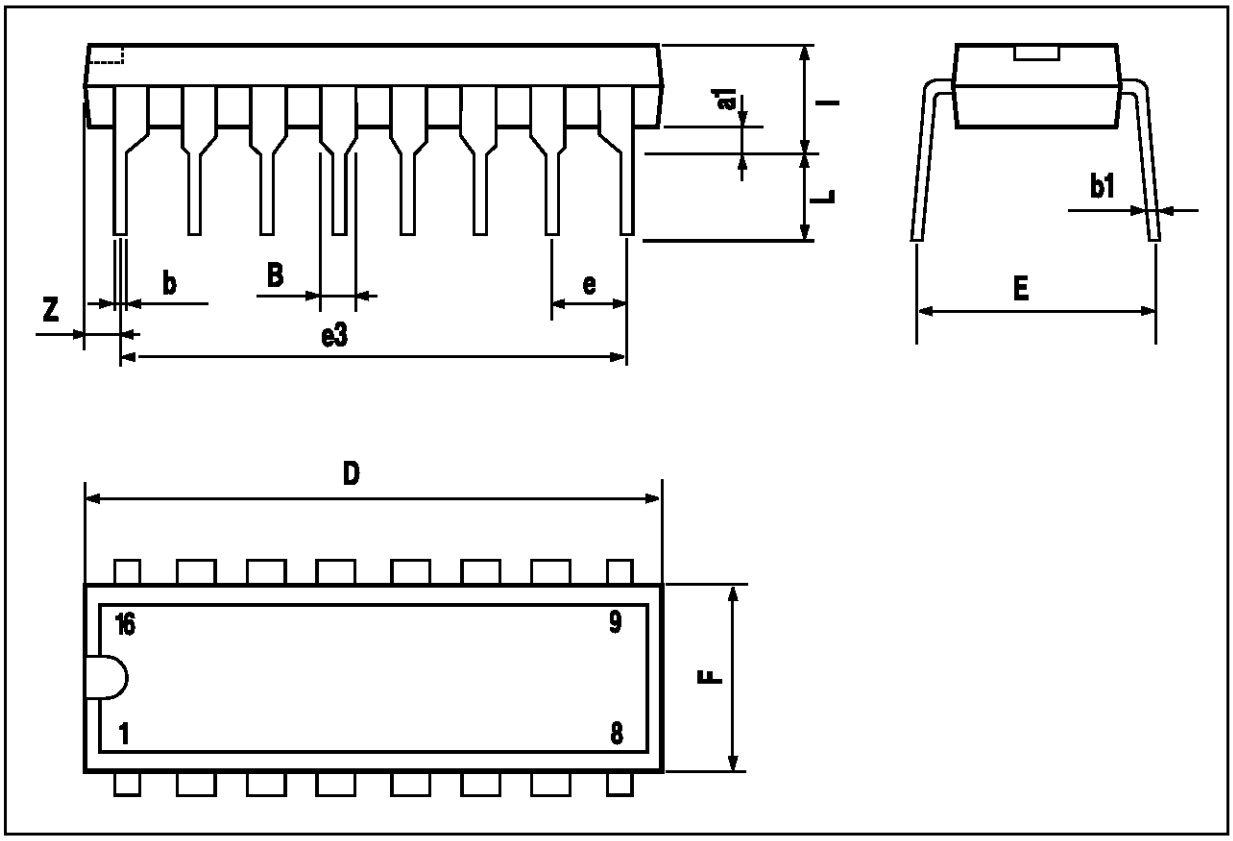
Figure 11.



Low power transformers can be driven directly by the SG1525A. Automatic reset occurs during dead time, when both ends of the primary winding are switched to ground.

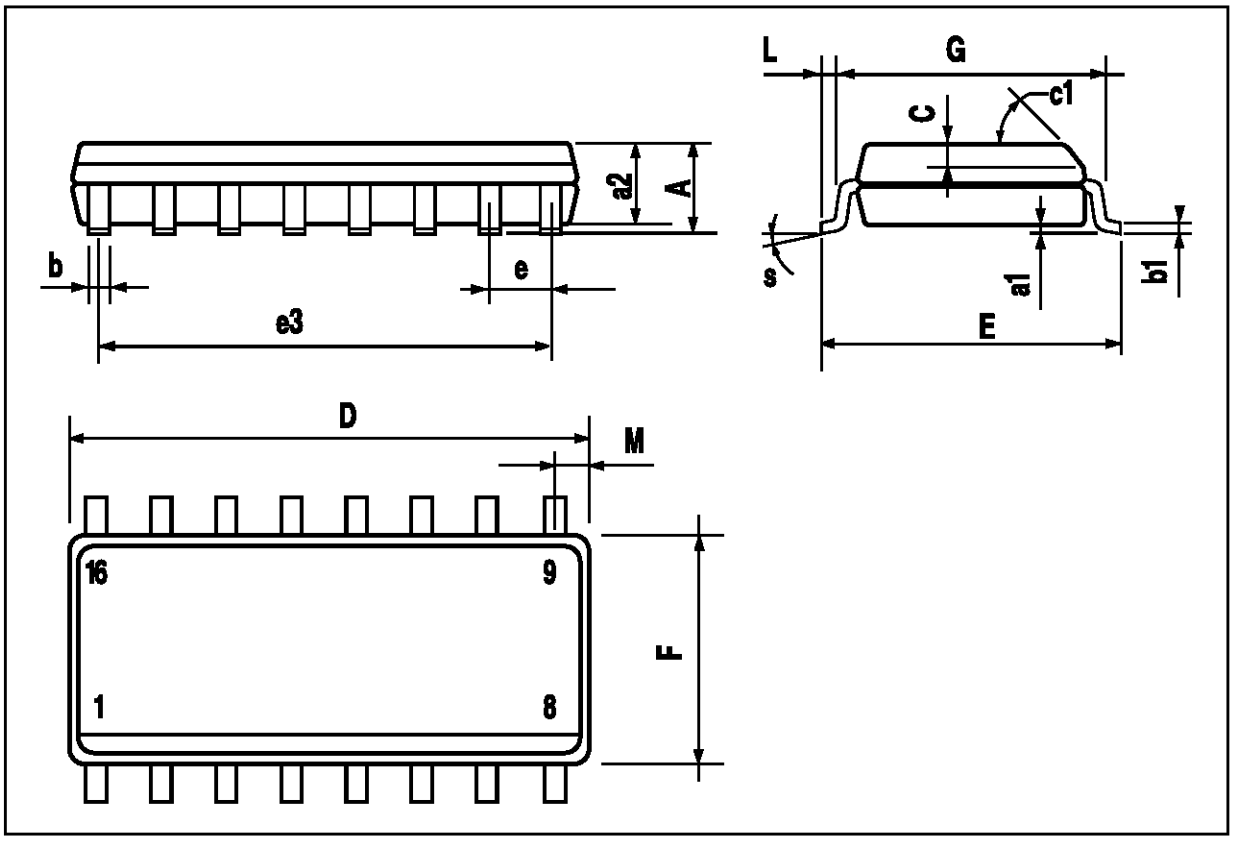
DIP16 PACKAGE MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
a1	0.51			0.020		
B	0.77		1.65	0.030		0.065
b		0.5			0.020	
b1		0.25			0.010	
D			20			0.787
E		8.5			0.335	
e		2.54			0.100	
e3		17.78			0.700	
F			7.1			0.280
I			5.1			0.201
L		3.3			0.130	
Z			1.27			0.050



SO16 NARROW PACKAGE MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.75			0.069
a1	0.1		0.25	0.004		0.009
a2			1.6			0.063
b	0.35		0.46	0.014		0.018
b1	0.19		0.25	0.007		0.010
C		0.5			0.020	
c1	45° (typ.)					
D	9.8		10	0.386		0.394
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		8.89			0.350	
F	3.8		4.0	0.150		0.157
L	0.4		1.27	0.150		0.050
M			0.62			0.024
S	8° (max.)					

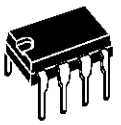


SGS-THOMSON MICROELECTRONICS

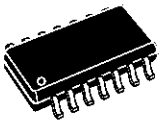
UC2842/3/4/5
UC3842/3/4/5

CURRENT MODE PWM CONTROLLER

- OPTIMIZED FOR OFF-LINE AND DC TO DC CONVERTERS
- LOW START-UP CURRENT (< 1 mA)
- AUTOMATIC FEED FORWARD COMPENSATION
- PULSE-BY-PULSE CURRENT LIMITING
- ENHANCED LOAD RESPONSE CHARACTERISTICS
- UNDER-VOLTAGE LOCKOUT WITH HYSTERESIS
- DOUBLE PULSE SUPPRESSION
- HIGH CURRENT TOTEM POLE OUTPUT
- INTERNALLY TRIMMED BANDGAP REFERENCE
- 500 KHz OPERATION
- LOW R_O ERROR AMP



Minidip



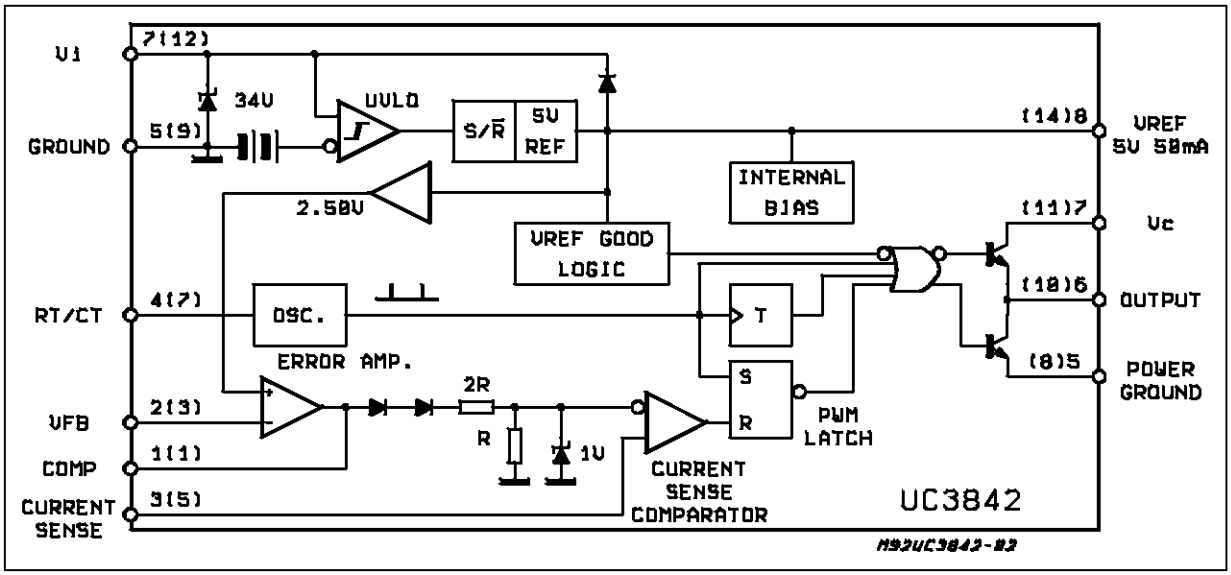
SO14

DESCRIPTION

The UC3842/3/4/5 family of control ICs provides the necessary features to implement off-line or DC to DC fixed frequency current mode control schemes with a minimal external parts count. Internally implemented circuits include under voltage lockout featuring start-up current less than 1 mA, a precision reference trimmed for accuracy at the error amp input, logic to insure latched operation, a PWM comparator which also provides current limit control, and a totem pole output stage designed to source or sink high peak current. The output stage, suitable for driving N-Channel MOSFETs, is low in the off-state.

Differences between members of this family are the under-voltage lockout thresholds and maximum duty cycle ranges. The UC3842 and UC3844 have UVLO thresholds of 16V (on) and 10V (off), ideally suited off-line applications The corresponding thresholds for the UC3843 and UC3845 are 8.5 V and 7.9 V. The UC3842 and UC3843 can operate to duty cycles approaching 100%. A range of the zero to < 50 % is obtained by the UC3844 and UC3845 by the addition of an internal toggle flip flop which blanks the output off every other clock cycle.

BLOCK DIAGRAM (toggle flip flop used only in U3844 and UC3845)



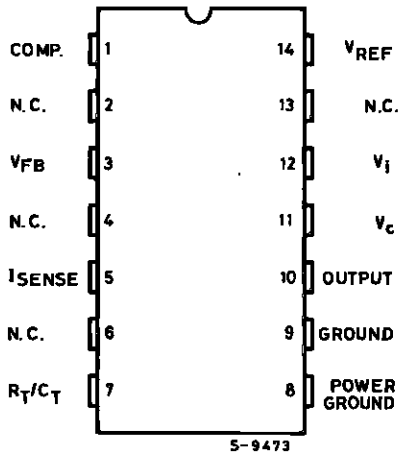
ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_i	Supply Voltage (low impedance source)	30	V
V_i	Supply Voltage (Ii < 30mA)	Self Limiting	
I_O	Output Current	±1	A
E_O	Output Energy (capacitive load)	5	µJ
	Analog Inputs (pins 2, 3)	– 0.3 to 6.3	V
	Error Amplifier Output Sink Current	10	mA
P_{tot}	Power Dissipation at $T_{amb} \leq 50$ °C (minidip, DIP-14)	1	W
P_{tot}	Power Dissipation at Tamb ≤ 25 °C (SO14)	725	mW
T_{stg}	Storage Temperature Range	– 65 to 150	°C
T_L	Lead Temperature (soldering 10s)	300	°C

* All voltages are with respect to pin 5, all currents are positive into the specified terminal.

PIN CONNECTIONS (top views)

SO14



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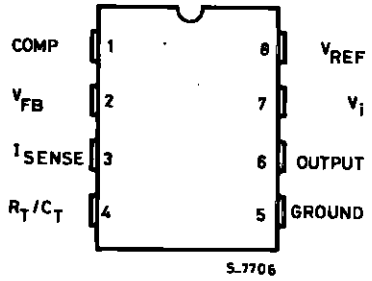


ORDERING NUMBERS

Type	Minidip	SO14
UC2842	UC2842N	UC2842D
UC3843	UC2843N	UC2843D
UC2844	UC2844N	UC2844D
UC2845	UC2845N	UC2845D
UC3842	UC3842N	UC3842D
UC3843	UC3843N	UC3843D
UC3844	UC3844N	UC3844D
UC3845	UC3845N	UC3845D

THERMAL DATA

Symbol	Description		Minidip	SO14	Unit
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient.	max.	100	165	°C

ELECTRICAL CHARACTERISTICS (Unless otherwise stated, these specifications apply for $-25 \le T_{amb} \le 85°C$ for UC2824X; $0 \le T_{amb} \le 70°C$ for UC384X; $V_i = 15V$ (note 5); $R_T = 10K$; $C_T = 3.3nF$)

Symbol	Parameter	Test Conditions	UC284X			UC384X			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
REFERENCE SECTION									
V_{REF}	Output Voltage	$T_j = 25°C$ $I_o = 1mA$	4.95	5.00	5.05	4.90	5.00	5.10	V
ΔV_{REF}	Line Regulation	$12V \le V_i \le 25V$		6	20		6	20	mV
ΔV_{REF}	Load Regulation	$1 \le I_o \le 20mA$		6	25		6	25	mV
$\Delta V_{REF}/\Delta T$	Temperature Stability	(Note 2)		0.2	0.4		0.2	0.4	mV/°C
	Total Output Variant	Line, Load, Temperature (2)	4.9		5.1	4.82		5.18	V
e_N	Output Noise Voltage	$10Hz \le f \le 10KHz$ $T_j = 25°C$ (2)		50			50		µV
	Long Term Stability	$T_{amb} = 125°C$, 1000Hrs (2)		5	25		5	25	mV
I_{SC}	Output Short Circuit		-30	-100	-180	-30	-100	-180	mA
OSCILLATOR SECTION									
f_s	Initial Accuracy	$T_j = 25°C$ (6)	47	52	57	47	52	57	KHz
	Voltage Stability	$12 \le V_i \le 25V$		0.2	1		0.2	1	%
	Temperature Stability	$T_{MIN} \le T_{amb} \le T_{MAX}$ (2)		5			5		%
V_4	Amplitude	V_{PIN4} Peak to Peak		1.7			1.7		V
ERROR AMP SECTION									
V_2	Input Voltage	$V_{PIN1} = 2.5V$	2.45	2.50	2.55	2.42	2.50	2.58	V
I_b	Input Bias Current			-0.3	-1		-0.3	-2	µA
	A_{VOL}	$2 \le V_o \le 4V$	65	90		65	90		dB
B	Unity Gain Bandwidth	(2)	0.7	1		0.7	1		MHz
SVR	Supply Voltage Rejection	$12V \le V_i \le 25V$	60	70		60	70		dB
I_o	Output Sink Current	$V_{PIN2} = 2.7V$ $V_{PIN1} = 1.1V$	2	6		2	6		V
I_o	Output Source Current	$V_{PIN2} = 2.3V$ $V_{PIN1} = 5V$	-0.5	-0.8		-0.5	-0.8		mA
	V_{OUT} High	$V_{PIN2} = 2.3V$; $R_L = 15K\Omega$ to Ground	5	6		5	6		V
	V_{OUT} Low	$V_{PIN2} = 2.7V$; $R_L = 15K\Omega$ to Pin 8		0.7	1.1		0.7	1.1	V
CURRENT SENSE SECTION									
G_V	Gain	(3 & 4)	2.85	3	3.15	2.8	3	3.2	V/V
V_3	Maximum Input Signal	$V_{PIN1} = 5V$ (3)	0.9	1	1.1	0.9	1	1.1	V
SVR	Supply Voltage Rejection	$12 \le V_i \le 25V$ (3)		70			70		dB
I_b	Input Bias Current			-2	-10		-2	-10	µA
	Delay to Output			150	300		150	300	ns
OUTPUT SECTION									
I_{OL}	Output Low Level	$I_{SINK} = 20mA$		0.1	0.4		0.1	0.4	V
		$I_{SINK} = 200mA$		1.5	2.2		1.5	2.2	V
I_{OH}	Output High Level	ISOURCE = 20mA	13	13.5		13	13.5		V
		$I_{SOURCE} = 200mA$	12	13.5		12	13.5		V
t_r	Rise Time	$T_j = 25°C$ $C_L = 1nF$ (2)		50	150		50	150	ns
t_f	Fall Time	$T_j = 25°C$ $C_L = 1nF$ (2)		50	150		50	150	ns

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Conditions	UC284X			UC384X			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
UNDER-VOLTAGE LOCKOUT SECTION									
	Start Threshold	X842/4	15	16	17	14.5	16	17.5	V
		X843/5	7.8	8.4	9.0	7.8	8.4	9	V
	Min Operating Voltage After Turn-on	X842/4	9	10	11	8.5	10	11.5	V
		X843/5	7.0	7.6	8.2	7.0	7.6	8.2	V
PWM SECTION									
	Maximum Duty Cycle	X842/3	93	97	100	93	97	100	%
		X844/5	46	48	50	47	48	50	%
	Minimum Duty Cycle				0			0	%
TOTAL STANDBY CURRENT									
I_{st}	Start-up Current			0.5	1		0.5	1	mA
I_i	Operating Supply Current	$V_{PIN2} = V_{PIN3} = 0V$		11	20		11	20	mA
V_{iz}	Zener Voltage	$I_i = 25mA$		34			34		V

Notes : 2. These parameters, although guaranteed, are not 100% tested in production.

3. Parameter measured at trip point of latch with $V_{PIN2} = 0$.

4. Gain defined as :

$$A = \frac{\Delta V_{PIN1}}{\Delta V_{PIN3}} ; 0 \leq V_{PIN3} \leq 0.8\,V$$

5. Adjust V_i above the start threshold before setting at 15 V.

6. Output frequency equals oscillator frequency for the UC3842 and UC3843.
Output frequency is one half oscillator frequency for the UC3844 and UC3845.

Figure 1 : Error Amp Configuration.

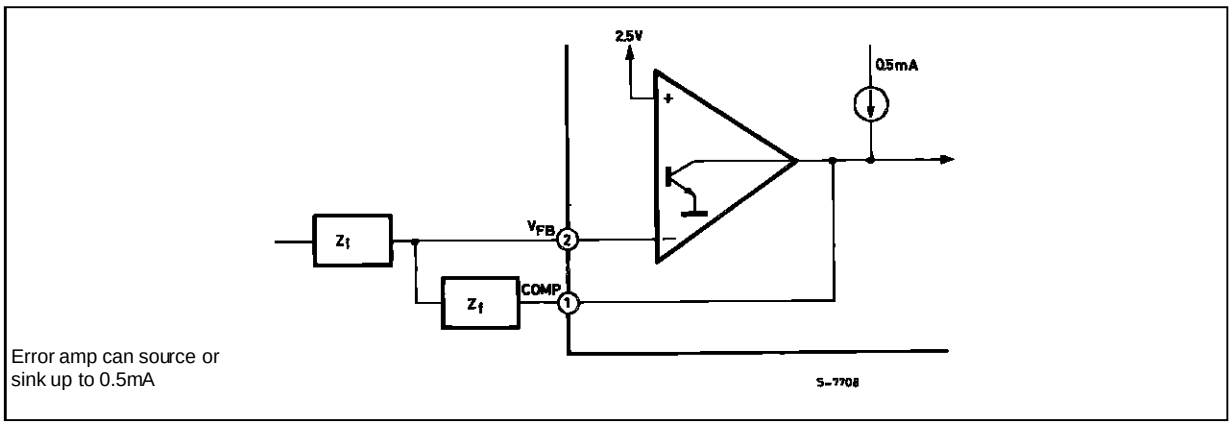
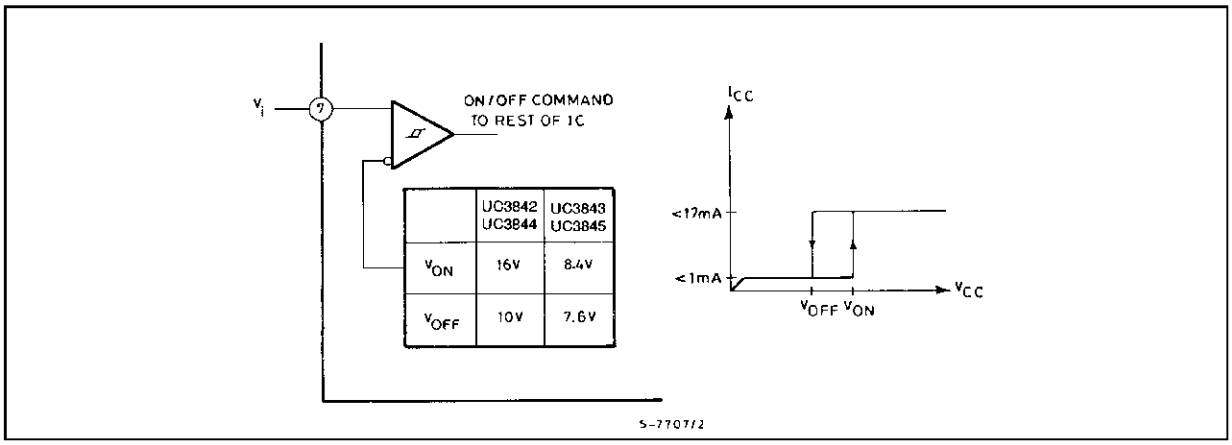
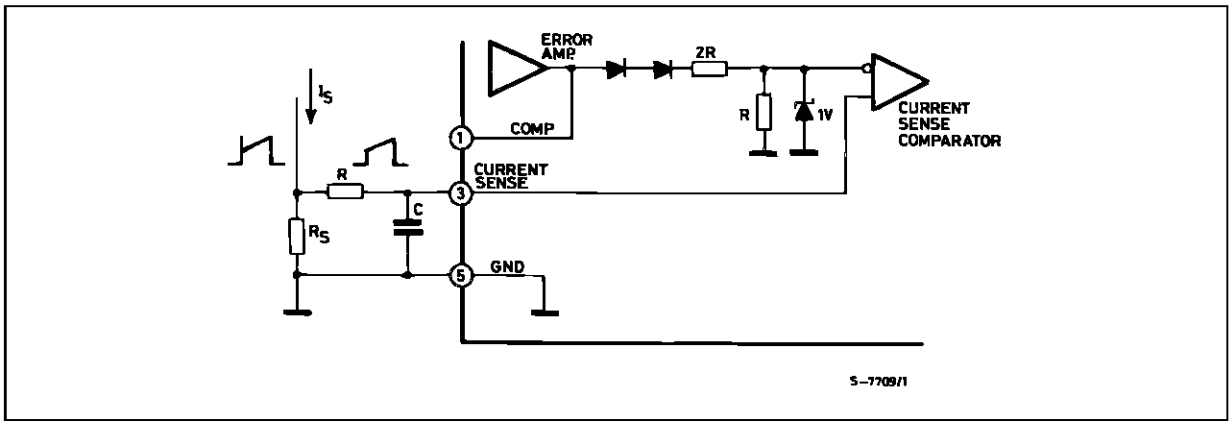


Figure 2 : Under Voltage Lockout.



During Under-Voltage Lockout, the output driver is biased to sink minor amounts of current. Pin 6 should be shunted to ground with a bleeder resistor to prevent activating the power switch with extraneous leakage currents.

Figure 3 : Current Sense Circuit .



Peak current (i_S) is determined by the formula

$$I_{S\,max} \approx \frac{1.0\,V}{R_S}$$

A small RC filter may be required to suppress switch transients.

Figure 4.

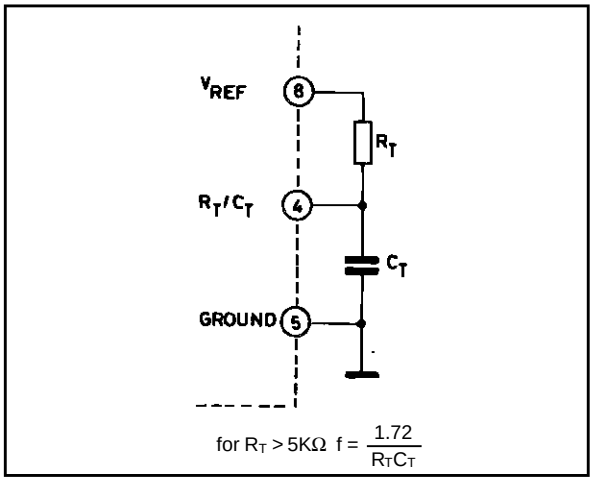


Figure 5 : Deadtime vs. C_T ($R_T > 5K\Omega$).

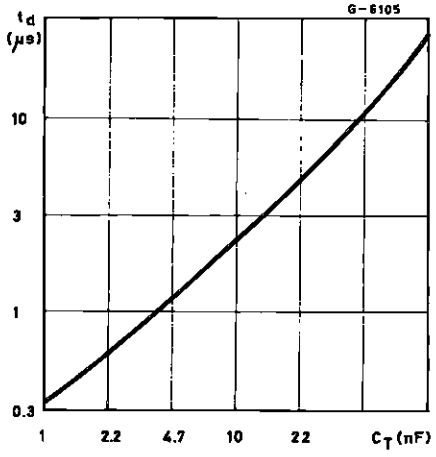


Figure 6 : Timing Resistance vs. Frequency.

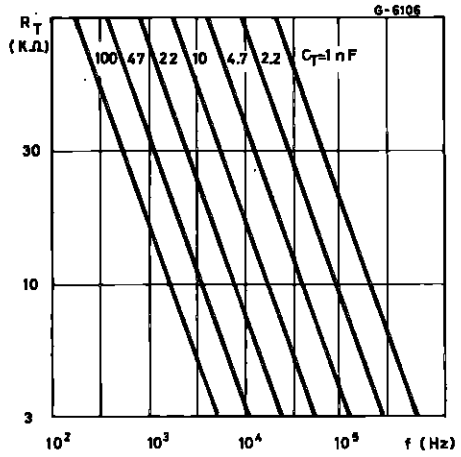


Figure 7 : Output Saturation Characteristics.

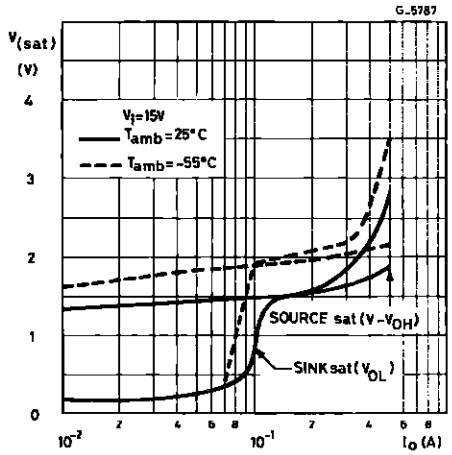


Figure 8 : Error Amplifier Open-loop Frequency Response.

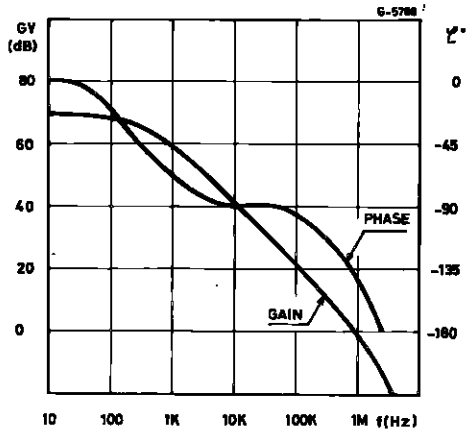
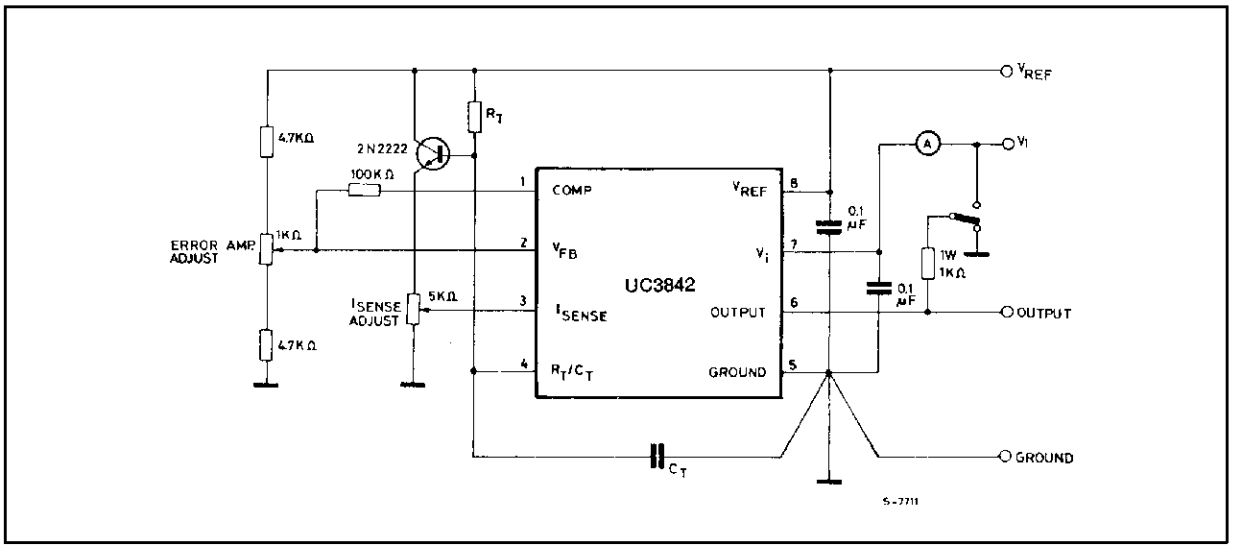
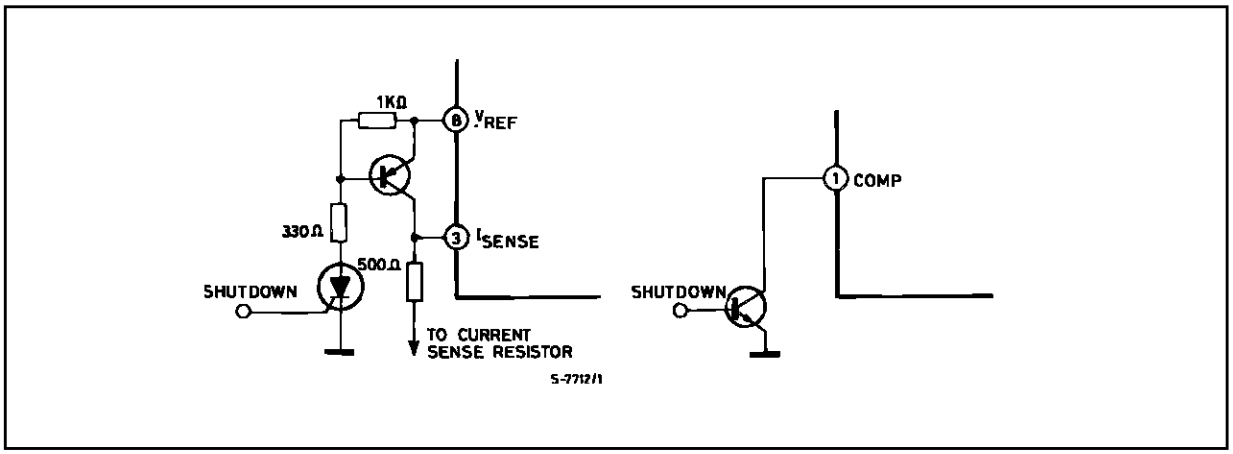


Figure 9 : Open Loop Test Circuit.



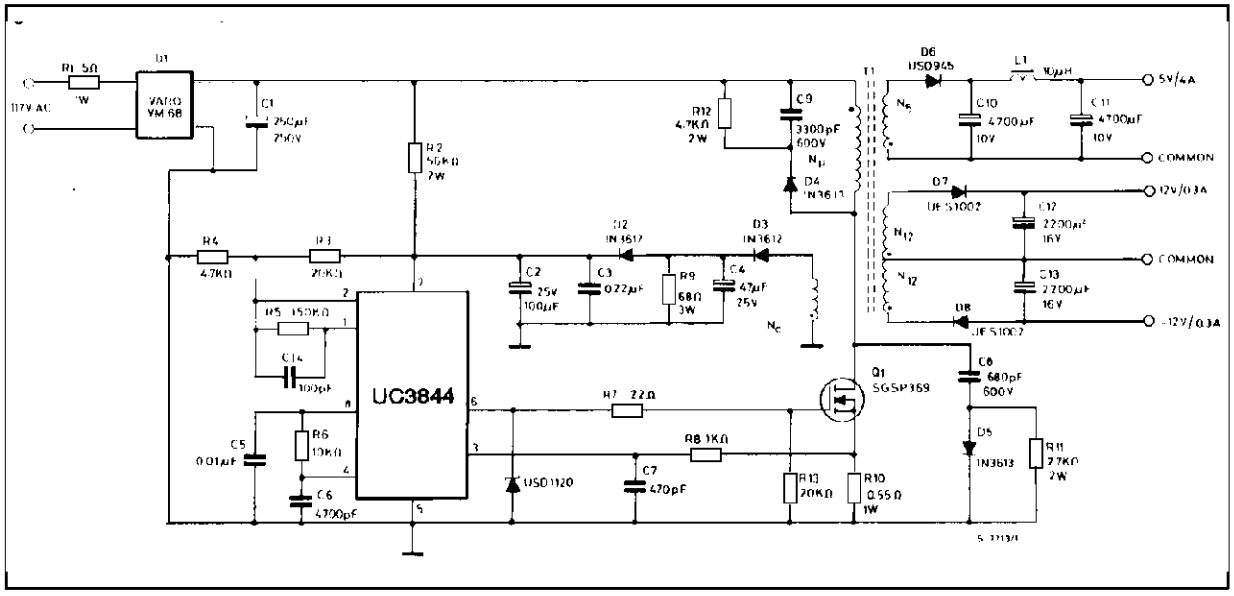
High peak currents associated with capacitive loads necessitate careful grounding techniques. Timing and bypass capacitors should be connected close to pin 5 in a single point ground. The transistor and 5 KΩ potentiometer are used to sample the oscillator waveform and apply an adjustable ramp to pin 3.

Figure 10 : Shutdown Techniques.



Shutdown of the UC2842 can be accomplished by two methods ; either raise pin 3 above 1V or pull pin 1 below a voltage two diode drops above ground. Either method cause the output of the PWM comparator to be high (refer to block diagram). The PWM latch is reset dominant so that the output will remain low until the next clock cycle after the shutdown condition at pins 1 and/or 3 is removed. In one example, an externally latched shutdown may be accomplished by adding an SCR which will be reset by cycling V_i below the lower UVLO threshold. At this point the reference turns off, allowing the SCR to reset.

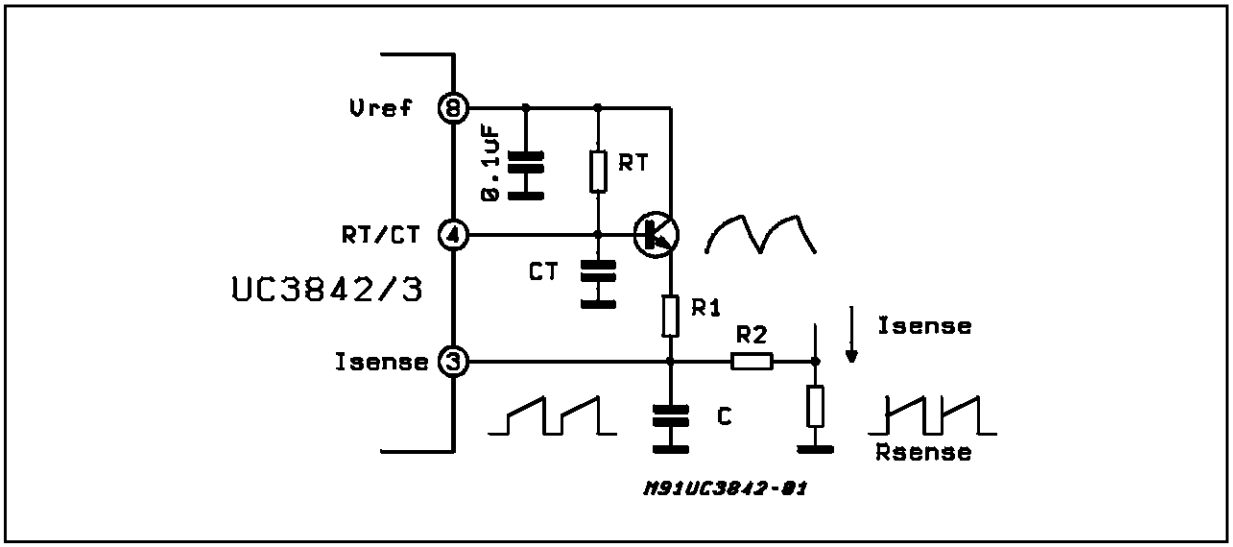
Figure 11 : Off-line Flyback Regulator.



Power Supply Specifications

1. Input Voltage : 95 VAC to 130 VAC (50 Hz/60 Hz)
2. Line Isolation : 3750 V
3. Switching Frequency : 40 KHz
4. Efficiency @ Full Load : 70 %
5. Output Voltage :
   A. + 5 V, ± 5 % : 1 A to 4 A load
   Ripple voltage : 50 mV P-P Max.
   B. + 12 V, ± 3 % : 0.1 A to 0.3 A load
   Ripple voltage : 100 mV P-P Max.
   C. – 12 V, ± 3 % : 0.1 A to 0.3 A load
   Ripple voltage : 100 mV P-P Max.

Figure 12 : Slope Compensation.

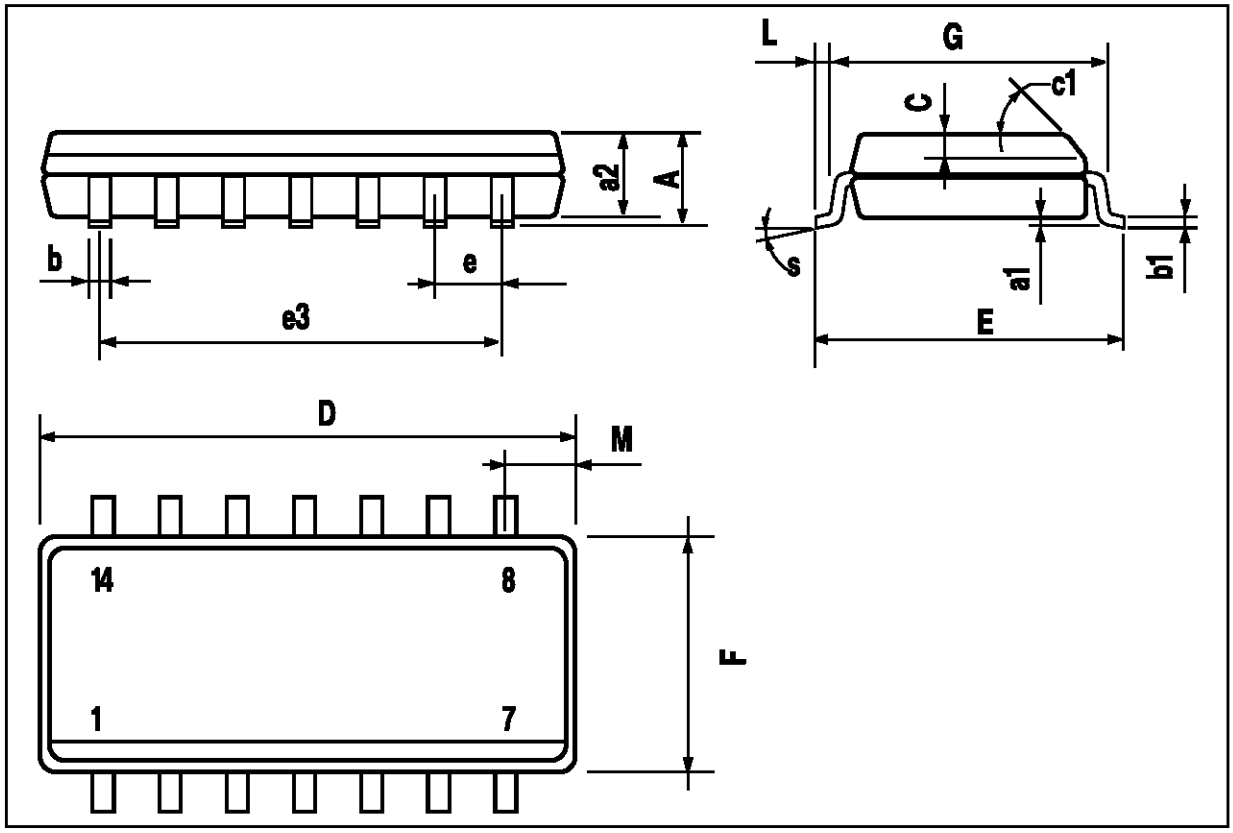


A fraction of the oscillator ramp can be resistively summed with the current sense signal to provide slope compensation for converters requiring duty cycles over 50 %.

Note that capacitor, C, forms a filter with R_2 to supress the leading edge switch spikes.

SO14 PACKAGE MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.75			0.069
a1	0.1		0.25	0.004		0.009
a2			1.6			0.063
b	0.35		0.46	0.014		0.018
b1	0.19		0.25	0.007		0.010
C		0.5			0.020	
c1	45 (typ.)					
D	8.55		8.75	0.336		0.344
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		7.62			0.300	
F	3.8		4.0	0.15		0.157
L	0.4		1.27	0.016		0.050
M			0.68			0.027
S	8 (max.)					



DIP14 PACKAGE MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A		3.32			0.131	
a1	0.51			0.020		
B	1.15		1.65	0.045		0.065
b	0.356		0.55	0.014		0.022
b1	0.204		0.304	0.008		0.012
D			10.92			0.430
E	7.95		9.75	0.313		0.384
e		2.54			0.100	
e3		7.62			0.300	
e4		7.62			0.300	
F			6.6			0.260
I			5.08			0.200
L	3.18		3.81	0.125		0.150