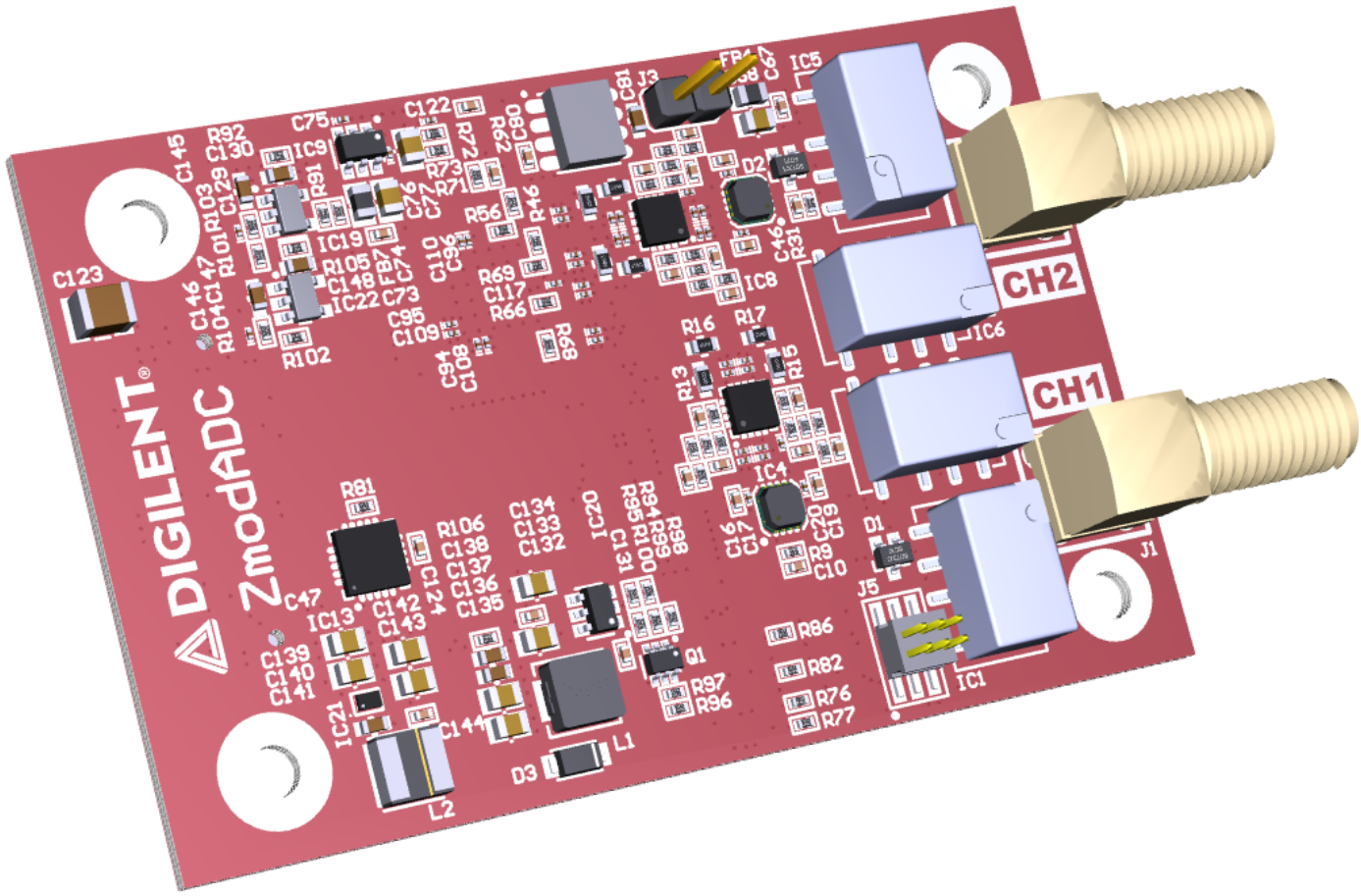
Zmod ADC Reference Manual

The Digilent Zmod ADC () is an open-source hardware SYZYGY™ [1]compatible pod containing a dual-channel ADC () and the associated front end. The Zmod ADC () is intended to be used with any SYZYGY™ compatible carrier board having the required capabilities.



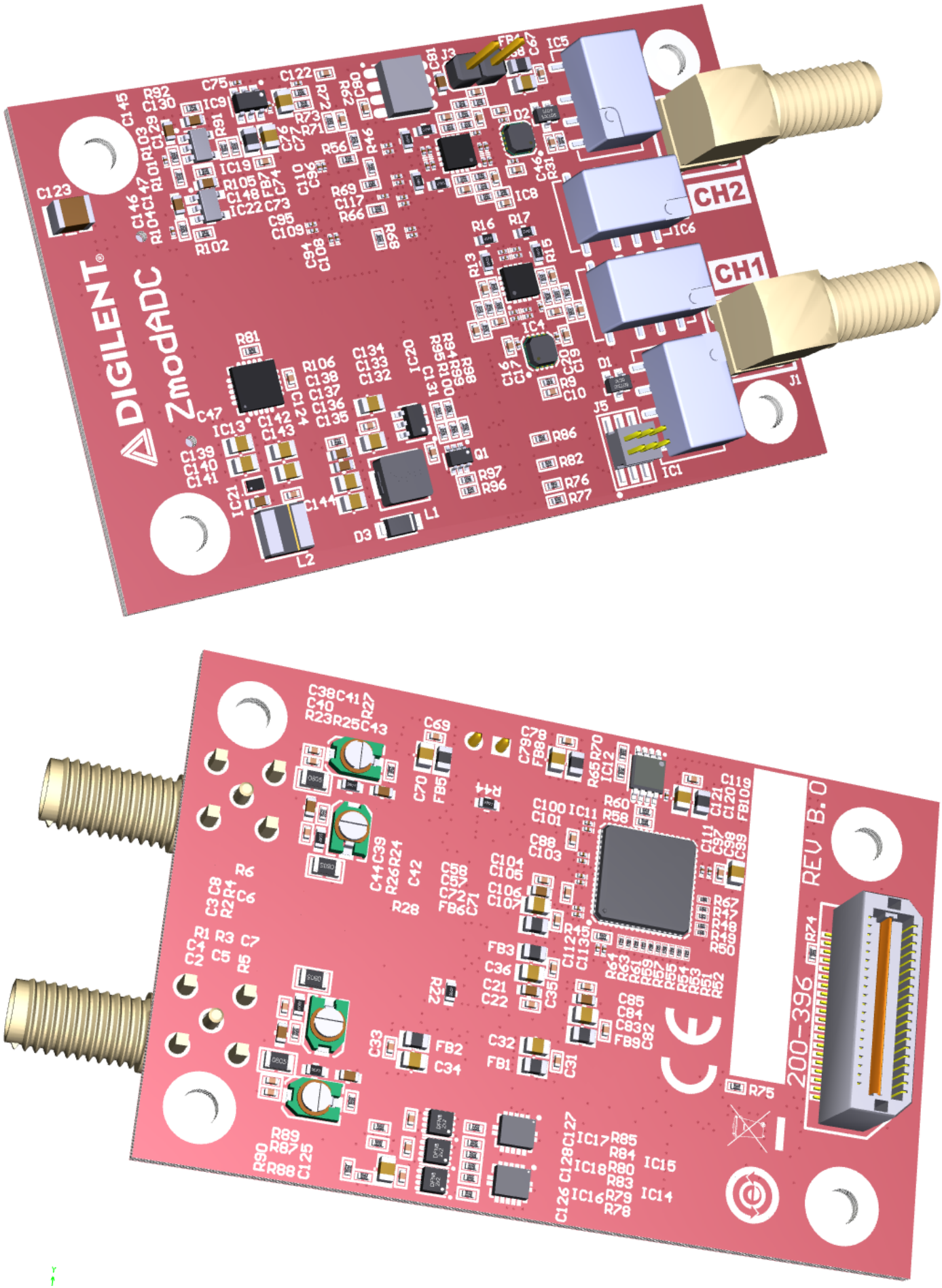


Figure 1. Zmod ADC top and bottom views. []

The analog inputs can be connected to a circuit using SMA cables. Driven by the SYZYGY™ carrier, the Zmod ADC () can acquire two simultaneous signals (1MΩ, ±25V, single-ended, 14-bit, 100MS/s, 70MHz+ bandwidth).

The Zmod ADC () was designed to be a piece in a modular, HW and SW open-source ecosystem. Combined with a SYZYGY™ carrier, other SYZYGY™ compatible pods, Zmod ADC () can be used for a variety of applications: data acquisition systems, closed loop controllers, scopes, etc.

Features

- Channels: 2
- Channel type: single ended
- Resolution: 14-bit
- Input range: ±1V (Low Range) or ±25V (High Range)
- Absolute Resolution: 0.13mV (Low Range) or 3.21mV (High Range)
  Accuracy: ±0.2% of Range
  Sample rate (real time): 100MS/s
  Input impedance: 1MΩ||18pF
  Analog bandwidth: 70 MHz ()+ @ 3dB, 30 MHz () @ 0.5dB, 20 MHz () @ 0.1dB
  Input protected to: ±50V

1. Architectural Overview and Block Diagram

This document describes the Zmod ADC ()'s circuits, with the intent of providing a better understanding of its electrical functions, operations, and a more detailed description of the hardware's features and limitations. It is not intended to provide enough information to enable complete duplication of the Zmod ADC (), but can help users to design custom configurations for programmable parts in the design.

Zmod ADC ()'s block diagram is presented in Fig. 2 below. The core of the Analog Zmod ADC () is the dual channel, high speed, low power, 14-bit, 105MS/s ADC (), AD9648. The carrier board is responsible to configure the internal registers of the ADC () circuit, provide the acquisition clock and receive the data.

The **Analog Input** block is also called the **Scope**, because of similar structure and behavior to such a front end. The signals in this circuitry use a "SC" indexes to indicate they are related to the scope block. Signals and equations also use certain naming conventions. Analog voltages are prefixed with a "V" (for voltage), and suffixes and indexes are used in various ways: to specify the location in the signal path (IN, MUX, BUF, ADC (), etc.); to indicate the related instrument (SC, etc.); to indicate the channel (1 or 2); and to indicate the type of signal (P, N, or diff). Referring to the block diagram in Fig. 2 below:

- **Input Divider and Gain Selection**: high bandwidth input adapter/divider. High or low-gain can be selected by the FPGA
  Buffer: high impedance buffer
  Driver: provides appropriate signal levels and protection to the ADC ().
  Scope Reference: generates and buffers reference voltages for the scope stages
  ADC (): the analog-to-digital converter for both scope channels.

The **Power Supplies and Control** block generates all internal supply voltages.

The **MCU** works as a I2C memory for two different purposes:

The **DNA** includes the standard SYZYGY™ (https://syzygyfpga.io) pod identification information.

- The **Calibration Memory** stores all calibration parameters. Except for the "Probe Calibration" trimmers in the scope Input divider, the Zmod ADC () includes no analog calibration circuitry. Instead, a calibration operation is performed at manufacturing (or by the user), and parameters are stored in memory. The application software uses these parameters to correct the acquired data and the generated signals

In the sections that follow, schematics are not shown separately for identical blocks. For example, the Scope Input Divider and Gain Selection schematic is only shown for channel 1 since the schematic for channel 2 is identical. Indexes are omitted where not relevant. As examples, in equation 1 below, $V_{SCOPE-SMA}$ does not contain the channel index (because the equation applies to both channels 1 and 2).

2. Scope

2.1. Scope Input Divider and Gain Selection

Fig. 3 shows the scope input divider and gain selection stage.

C_5 and C_6 are capacitive trimmers, 3…10pF, -0/+50% tolerance. The worse case range is 4.5…10pF. All other capacitors are 1% tolerance, all the resistors are 0.1%.

The IC1 relay switches between two symmetrical R-C dividers. Each of them provide:

- Scope input impedance = 1MOhm || 18pF
- Two different attenuations for high-gain/low-gain (25:1)
- Controlled capacitance, much higher than the parasitical capacitance of subsequent stages
- Constant attenuation over a large frequency range (trimmer adjusted)

The maximum voltage rating for scope inputs is limited to:

$$-50V < V_{SCOPE-SMA} < 50V \tag{1}$$

The DC low gain is:

$$\frac{V_{SC-LG}}{V_{SCOPE-SMA}} = \frac{R_5}{R_1 + R_3 + R_5} = 0.04 \tag{2}$$

The High Range (at low gain):

$$-25V \leq V_{SCOPE-SMA} \leq 25V \tag{3}$$

The high gain is:

$$\frac{V_{SC-HG}}{V_{SCOPE-SMA}} = \frac{R_4 + R_6}{R_2 + R_4 + R_6} = 0.96 \tag{4}$$

The Low Range (at high gain):

$$-1V \leq V_{SCOPE-SMA} \leq 1V \tag{5}$$

The two dividers are designed to have the same equivalent impedance (both active and reactive):

$$R_{ech} = R_1 + R_3 + R_5 = R_2 + R_4 + R_6 = 1Mohm \tag{6}$$

Experiments shown that there are significant parasitic capacities of the layout and buffer input stage: C_{PH} (high gain divider), parallel to C_6, and C_{PL} (low gain divider), parallel to C_7. The trimmers should compensate for these parasitic capacities and adjust for perfect matching:

$$C_3 * R_2 = (C_{PH} + C_6) * (R_4 + R_6) \tag{7}$$

$$(C_{PH} + C_6) = \frac{C_3 * R_2}{R_4 + R_6} = 18pF \tag{8}$$

$$(C_4 + C_5) * (R_1 + R_3) = (C_{PL} + C_7) * R_5 \tag{9}$$

$$(C_{PL} + C_7) = (C_4 + C_5) * \frac{(R_1 + R_3)}{R_5} \tag{10}$$

With the chosen values, the correct adjustment results in about mid-position of trimmers C_5 and C_6:

$$C_5 = C_6 = 7pF \tag{11}$$

which solves the parasitic capacities as:

$$C_{PH} = 11pF \tag{12}$$

$$C_{PL} = 8.8pF \tag{13}$$

The Low Gain and High Gain dividers have very close equivalent capacitance, within the tolerances and model approximations:

$$C_{HGech} = \frac{C_3 * R_2}{R_2 + R_4 + R_6} = C_{ech} = 17.28pF \tag{14}$$

$$C_{LGech} = \frac{(C_7 + C_{PL}) * R_5}{R_1 + R_3 + R_5} = 16.03p \tag{15}$$

Experiments show that the equivalent capacitances are even closer than the values above, about 18pF. The computing error mainly derives from trimmer position approximation.

$$C_{ech} = 18p \tag{16}$$

The IC2 relay shorts the C1 capacitor when DC coupling is desired. Otherwise, C1 forms a High Pass filter with the selected divider, for AC coupling, with the corner frequency:

$$f_c = \frac{1}{2 * \pi * R_{ech} * (C_{ech} + C_1)} \approx \frac{1}{2 * \pi * R_{ech} * C_1} = 10.6Hz \tag{17}$$

IC1 and IC2 in Fig. 3, are HFD4/4.5L latching relays possible replacement: IM42GR
The schematic shows the “reset” position. A relay is “set” when a positive voltage is applied at the coil terminals and it is “reset” when a negative voltage is applied (see the polarity on the schematic symbol). The relay keeps state when no current flows trough the coil (the terminals are driven at the same voltage or at least one of the terminals is “open”). The nominal coil voltage is 4.5V.

The IC16, IC17 and IC18 in Fig. 4 are A3910EEETR-T drivers for the relays.
They feature:

- Low RDS(on) outputs
- Standby mode with zero current drain
- Small 2 × 2 DFN package
- Crossover Current protection
- Thermal Shutdown protection

Normally, all of them have both HIN and LIN inputs “low” or both “High” driving the “OUT” pins “High Z”. To “set” a relay, OUT2 of IC16 is set “Low” (HIN=“Low”, LIN=“High”) and the corresponding OUT pin of IC17 or IC18 is set “High” (HIN=“High”, LIN=“Low”). All other OUT pins are set “High Z”. To “reset” a relay, OUT2 of IC16 is set “High” (HIN=“High”, LIN=“Low”) and the corresponding OUT pin of IC17 or IC18 is set “Low” (HIN=“Low”, LIN=“High”). All other OUT pins are set “High Z”.

Figure 4. Relay Drivers. []

IC14 and IC15 in Fig. 5 are 74LVC07ABQ open-drain gates used as level translators from VADJ = 1.8V to VCC5V0 = 5V.

5 V tolerant inputs and outputs (open-drain) for interfacing with 5 V logic
Wide supply voltage range from 1.2 V to 5.5 V

- CMOS low power consumption
- Direct interface with TTL levels
- Inputs accept voltages up to 5 V
- Complies with JEDEC standard:
- JESD8-7A (1.65 V to 1.95 V)
- JESD8-5A (2.3 V to 2.7 V)
- JESD8-C/JESD36 (2.7 V to 3.6 V)
- ESD protection:
- HBM JESD22-A114F exceeds 2000 V
- MM JESD22-A115-B exceeds 200 V
- CDM JESD22-C101E exceeds 1000 V
- Specified from -40 °C to +85 °C and -40 °C to +125 °C

2.2. Scope Buffer

A non-inverting ADA4817 stage provides very high impedance as load for the input divider.

- High speed
  - −3 dB bandwidth (G = 1, RL = 100 Ω): 1050 MHz ()
  - Slew rate: 870 V/µs
  - 0.1% settling time: 9 ns
- Input bias current: 2 pAtypical
- Input capacitance
  - Common-mode capacitance: 1.3 pF typical
  - Differential mode capacitance: 0.1 pF typical
- Low input noise
  - Voltage noise: 4 nV/√Hz at 100 kHz ()
  - Current noise: 2.5 fA/√Hz at 100 kHz ()
- Low distortion: −90 dBc at 10 MHz () (G = 1, RL = 1 kΩ)
- Linear output current: 40 mA
- Supply quiescent current per amplifier: 19 mAtypical
- Powered down supply quiescent current per amplifier: 1.5 mAtypical

The ADA4817 is supplied +4.5V/-2.5V.

The maximum input voltage swing is:

$$-2.5V < V_{SC-HLG} < 1.7V \tag{18}$$

The maximum output voltage swing is:

$$-1.3V < V_{BUFF} < 3.1V \tag{19}$$

The gain is:

$$\frac{V_{BUFF}}{V_{SC-HLG}} = 1 \tag{20}$$

The actual input and output range (for nominal usage) is:

$$-1V < V_{SC-HLG} = V_{BUFF} < 1V \tag{21}$$

The ADA4817 data sheet does not include any explicit or implicit mention of input protection diodes, nor about the maximum current supported by such diodes, so external D1 was added in the schematic for safety. However, the leakage current of D1 adds significant error and experiments proved that the input protection diodes do exist within the ADA4817, so D1 is a “No Load”.

The Zmod ADC () is specified to resist to accidental input voltages up to +/-50V. In these cases, the buffer input voltage is limited by the protection diodes at 0.6V above the AVCC4V5 or below AVCC-2V5. The protection current is limited by R2 (at High Gain) or R1+R3 (at Low Gain) (see the input divider

$$\frac{SCOPE-SMA - V_{AVCC-2V5}}{} = \frac{-50V + 2.5V}{40.2kohm} = -1.18mA \tag{22}$$

2.3. Scope Reference

In Fig. 7, a low noise reference, ADR3412ARJZ and an ADA4841-2 OpAmp are used to generate 1V reference voltage for the ADC ().

ADR3412ARJZ features:

- Initial accuracy: ±0.1% (maximum)
- Maximum temperature coefficient: 8 ppm/°C
- Operating temperature range: −40°C to +125°C
- Output current: +10 mA source/−3 mA sink
- Low quiescent current: 100 µA (maximum)
- Low dropout voltage: 250 mV at 2 mA
- Output noise (0.1

The ADC () reference voltage is:

$$V_{REFADC} = V_{REF1V2SC} * \frac{R_{73}}{R_{71} + R_{73}} = 1V \tag{23}$$

An ADA4841-2 OpAmp buffers the VCM voltage generated by the ADC () to feed the ADC () buffer, in Fig. 8.

ADA4841-2

Low power: 1.1 mA/amp

- Low wideband noise
  - 2.1 nV/√Hz
  - 1.4 pA/√Hz
- Low 1/f noise
  - 7 nV/√Hz @ 10 Hz ()
  - 13 pA/√Hz @ 10 Hz ()
- Low distortion: −105 dBc @ 100 kHz (), VO = 2 V p-p
- High speed
  - 80 MHz (), −3 dB bandwidth (G = +1)
  - 12 V/µs slew rate
  - 175 ns settling time to 0.1%
- Low offset voltage: 0.3 mV maximum
- Rail-to-rail output
- Power down
- Wide supply range: 2.7 V to 12 V

The ADC () VCM voltage is:

$$V_{CMSC} = V_{VCMADC} = V_{VCMADC0V9} * (1 + \frac{R_{65}}{R_{70}}) = 1.2V \tag{24}$$

An LT1461-2.5 reference generates a voltage used for rising the input common mode voltage of the ADC () buffer, in Fig. 10.

LT1461-2.5

- Trimmed to High Accuracy: 0.04% Max
- Low Drift: 3ppm/°C Max
- Low Supply Current: 50µA Max
- High Output Current: 50mA Min
- Low Dropout Voltage: 300mV Max
- Excellent Thermal Regulation
- Power Shutdown
- Thermal Limiting
- All Parts Guaranteed Functional from –40°C to 125°C
- Voltage Options: 2.5V, 3V, 3.3V, 4.096V and 5V

2.4. Scope Driver

IC2, LTC6406 in Fig. 10 is the ADC () dirver.

- Low Noise: 1.6nV/√Hz RTI
- Low Power: 18mA at 3V

- Low Distortion (HD2/HD3):
  - –80dBc/–69dBc at 50MHz, 2VP-P
  - –104dBc/–90dBc at 20MHz, 2VP-P
- Rail-to-Rail Differential Input
- 2.7V to 3.5V Supply Voltage Range
- Fully Differential Input and Output
- Adjustable Output Common Mode Voltage
- 800MHz –3dB Bandwidth with AV = 1
- Gain-Bandwidth Product: 3GHz
- Low Power Shutdown
- Available in 8-Lead MSOP and Tiny 16-Lead
- 3mm × 3mm × 0.75mm QFN Packages

It is used for:

- Driving the differential inputs of the ADC () (with low impedance outputs)
  Providing the common mode voltage for the ADC ()
  ADC () protection: IC2 is supplied 3V, while the ADC () inputs only support -0.1…2.1V.

The input common mode voltage range is rail-to-rail:

$$0V \leq V_{+LTC6406} = V_{-LTC6406} \leq 3V \tag{25}$$

The actual input common mode voltage is:

The driver gain is:

$$G_{drv} = \frac{V_{OUTdiff}}{V_{BUFF}} = \frac{R_{11}}{R_{12}} = \frac{R_{19}}{R_{14}} = 1.27 \tag{26}$$

The output divider gain:

$$G_{div} = \frac{V_{ADCdiff}}{V_{OUTdiff}} = \frac{R_{16}}{R_{13} + R_{16}} = \frac{R_{17}}{R_{15} + R_{17}} = 0.746 \tag{27}$$

The nominal Driver input voltage range is:

$$-1V < V_{BUFF} < 1V \tag{28}$$

The nominal Driver output voltage range is:

$$-1.27V < V_{OUT\ diff} < 1.27V \tag{29}$$

With a unity common mode gain, the driver output common mode voltage is:

$$V_{CMOUT} = (V_{OUT+} + V_{OUT-})/2 = V_{CMSC} = 1.2V \tag{30}$$

The nominal Buffer output single ended voltage range is:

$$V_{CMOUT} - V_{OUT\ diff}/2 = 1.2V - 1.27/2 = 0.565V < V_{OUT+}, V_{OUT-} < V_{CMOUT} + V_{OUT\ diff}/2 = 1.2V + 1.27/2 = 1.835V \tag{31}$$

The maximum nominal driver single ended current is:

$$I_{OUT\ max} = \frac{V_{OUT\ max}}{R_{13} + R_{16}} = \frac{1.835V}{394ohm} = 4.65mA \tag{32}$$

which is below the data sheet limit of 5mA, for covering the driver single ended voltage range above.

For passing at the ADC () input, the voltages above are multiplied by the resistive divider gain of G_{div}.

The nominal differential ADC () input voltage range is:

$$-1V < V_{ADC\ diff} < 1V \tag{33}$$

The output divider common mode voltage is close to the recommended 0.9V:

$$V_{CMADC} = (V_{ADCP} + V_{ADCN})/2 = 0.895V \tag{34}$$

The ADC () input single ended voltage range is:

$$0.395V < V_{ADCP}, V_{ADCN} < 1.395V \tag{35}$$

For the ADC () input protection, the maximum driver single ended voltage should be considered. The driver amplifier datasheet only specifies the linear output voltage range. There is no information about the worst case saturated output voltages. Based on the data sheet and measurements, the driver maximum saturated single ended voltage was estimated to:

$$V_{OUT\ max\ sat} < 2.5V \tag{36}$$

Resulting a stress value at the ADC () input:

$$V_{ADC\ max\ sat} = V_{OUT\ max\ sat} * G_{div} = 1.865V \tag{37}$$

which is less than the allowed voltage at the ADC () input = 2.1V.

2.5. Scope ADC

The Zmod ADC () uses a dual channel, high speed, low power, 14-bit, 105MS/s ADC () (Analog part number AD9648, as shown in Fig. 11.

The important features of AD9648:

- SNR = 74.5dBFS @70 MHz ()
- SFDR =91dBc @70 MHz ()
- Low power: 78mW/channel ADC () core@ 125MS/s
- Differential analog input with 650 MHz () bandwidth
- IF sampling frequencies to 200 MHz ()
- On-chip voltage reference and sample-and-hold circuit
- 2 V p-p differential analog input
- DNL = ±0.35 LSB
- Serial port control options
- Offset binary, gray code, or two's complement data format
- Optional clock duty cycle stabilizer
- Integer 1-to-8 input clock divider
- Data output multiplex option
- Built-in selectable digital test pattern generation
- Energy-saving power-down modes
- Data clock out with programmable clock and data alignment

The differential inputs are driven via a low-pass filter comprised of C114 together with R13, R15, R16, R17 in the buffer stage. The differential clock is AC-coupled and the line is impedance matched. The clock is internally divided by 4 to operate the ADC () at a constant 100 MHz () sampling rate. The ADC () generates the common mode reference voltage (VCM_SC) to be used in the buffer stage.

The digital stage of the ADC () and the corresponding FPGA bank are supplied at 1.8V by the SYZYGY™ voltage V_{adj}.

The multiplexed mode is used, to combine the two channels on a single data bus and minimize the number of used FPGA pins. CLKOUT_SC is provided to the FPGA for synchronizing data.

2.6. Scope Signal Scaling

Combining Gain equations 2, 4, 20, 26, and 27 from previous chapters, the total scope gains are:

$$Low\ gain = \frac{V_{ADC\ diff}}{V_{SCOPE-SMA}} = 0.038 \tag{38}$$

$$High\ gain = \frac{V_{ADC\ diff}}{V_{SCOPE-SMA}} = 0.91 \tag{39}$$

Considering the ADC () input voltage range shown in 33:

$$at\ low\ gain: -26.3V < V_{SCOPE-SMA} < 26.3V$$

$$at\ high\ gain: -1.1V < V_{SCOPE-SMA} < 1.1V \tag{40}$$

To cover component value tolerances and to allow software calibration, only the ranges below are specified.

$$at\ low\ gain: -25V < V_{SCOPE-SMA} < 25V \tag{41}$$

$$at\ high\ gain: -1V < V_{SCOPE-SMA} < 1V \tag{42}$$

With the 14-bit ADC (), the absolute resolution of the scope is:

$$at\ low\ gain: \frac{52.6V}{2^{14}} = 3.21mV \tag{43}$$

$$at\ high\ gain: \frac{2.12V}{2^{14}} = 0.13mV \tag{44}$$

For V_{in} voltage value at the input of the Scope channel, the ZmodADC sends a signed 14 bit integer, N. This value is used to compute V_{in}:

$$V_{in} = \frac{N \cdot Range \cdot (1 + CG)}{2^{13}} + CA \tag{45}$$

were:

- N = the 14 bit, 2's complement integer number returned by the ADC ()
- V_{in}= the corrected value of the input voltage
- CA = calibration Additive constant (for the appropriate channel and gain; see Table 3)
- CG = calibration Gain constant (for the appropriate channel and gain; see Table 3)
- Range= the ideal Range of the Scope input stage (approximation of the values in equation 40):
  - 1.086 (for low range: ±1V) or
  - 26.25 (for high range: ±25V)

2.7 Scope Spectral Characteristics

Fig. 12 shows a typical spectral characteristic of the scope input stage. A PXIe-5433 80 MHz () Function/Arbitrary Waveform Generator was used to generate the input signal of 0.9V, for High Gain Scale, respectively 10V for the Low Gain scale. A Tektronix DPO5204B scope was used for measuring the reference signal (at the scope SMA connector) and the output signal (at the input of the ADC ()). A differential probe was used to read the output signal on the pads of the unloaded C115. The signal swept from 800kHz to 80MHz. The effective values of the input and output signals were recorded for each frequency. The measurements were furter processesd to display the input stage frequency characteristics, as shown in Fig. 10.

For both scales, the 3dB bandwidth is 70MHz+. The 0.5dB bandwidth is 30MHz and the 0.1dB bandwidth is 20MHz.

The standard -3dB bandwidth definition is derived from filter theory. At cutout frequency, the scope attenuates the spectral components by 0.707, assuming an error of ~30%, way too high for a measuring instrument. The bandwidth with a specified flatness is useful to better define the scope spectral performances. The Zmod ADC () exhibits 30MHz+ @ 0.5dB, meaning that a 30 MHz () sinusoidal signal is shown with a flatness error of a max 5.6%. 20MHz @ 0.1dB means that a 5 MHz () sinusoidal signal is shown with a flatness error of a max 1.1%.

3. MCU

The ATtinny44 MCU in Fig. 13 works as a I2C memory, storing the SYZYGY™ DNA information and the Calibration Coefficients. The J5 connector is used for programming the MCU and the SYZYGY™ DNA at manufacturing.

The DNA and the Factory Calibration Coefficients are stored in the Flash memory of the MCU, which appears to the I2C interface as “read-only”. The User Calibration Coefficients are stored in the EEPROM () memory of the MCU, which is write-protected via a magic number at a magic address. The memory structure can be consulted below.

- Program Memory Type: Flash
- Program Memory Size (KB): 4
  CPU Speed (MIPS/DMIPS): 20
  SRAM Bytes: 256
  Data EEPROM ()/HEF (bytes): 256
  Digital Communication Peripherals: 1-SPI, 1-I2C
  Capture/Compare/PWM Peripherals: 1 Input Capture, 1 CCP, 4PWM
  Timers: 1 x 8-bit, 1 x 16-bit
- Number of Comparators: 1
- Temperature Range (C): -40 to 85
- Operating Voltage Range (V): 1.8 to 5.5
- Pin Count: 14
- Low Power: Yes

Table 1. The Flash memory structure []

Address	Function	Size (Bytes)
0x8000 - 0x80FF	DNA	256
0x8100 - 0x817F	Factory Calibration	128
0x8180 - 0x83FF	Future use	896

3.1. SYZYGY™ DNA

The Zmod ADC () is compliant with SYZYGY™ Specification (https://syzygyfpga.io/specification/). It contains an MCU able to calculate the Geographical Address and provide the DNA information via I2C. The DNA is stored in the MCU FLASH at the address range: 0x8000 - 0x80FF with the following structure:

Table 2. The Zmod ADC DNA structure []

Contents	Type	Size(Bytes)	Value	Address
DNA full data length	uint16	2	91	0x8000
DNA header length	uint16	2	40	0x8002
SYZYGY DNA major version	uint8	1	1	0x8004
SYZYGY DNA minor version	uint8	1	0	0x8005
Required SYZYGY DNA major version	uint8	1	1	0x8006
Required SYZYGY DNA minor version	uint8	1	0	0x8007
Maximum operating 5V load (mA)	uint16	2	400	0x8008
Maximum operating 3.3V load (mA)	uint16	2	100	0x800A
Maximum VIO load (mA)	uint16	2	270	0x800C
Attribute flags	uint16	2	0	0x800E
Minimum operating VIO (10 mV steps)	uint16	2	180	0x8010
Maximum operating VIO (10 mV steps)	uint16	2	180	0x8012
Minimum operating VIO (10 mV steps)	uint16	2	170	0x8014
Maximum operating VIO (10 mV steps)	uint16	2	190	0x8016
Minimum operating VIO (10 mV steps)	uint16	2	0	0x8018
Maximum operating VIO (10 mV steps)	uint16	2	0	0x801A
Minimum operating VIO (10 mV steps)	uint16	2	0	0x801C
Maximum operating VIO (10 mV steps)	uint16	2	0	0x801E
Manufacturer name length	uint8	1	12	0x8020
Product name length	uint8	1	13	0x8021
Product model / Part number length	uint8	1	13	0x8022
Product version / revision length	uint8	1	1	0x8023
Serial number length	uint8	1	12	0x8024
RESERVED	uint8	1	0	0x8025
CRC-16 (most significant byte)	uint8	1	0x40	0x8026
CRC-16 (least significant byte)	uint8	1	0xF0	0x8027
END DATA HEADER				
Manufacturer name	string	12	Digilent Inc	0x8028
Product name	string	13	Zmod ADC () 1410	0x8034
Product model / Part number	string	13	Zmod ADC () 1410	0x8041
Product version / revision	string	1	B	0x804E
Serial number	string	12	210396000000	0x804F

3.2. Calibration Memory

The analog circuitry described in previous chapters includes passive and active electronic components. The datasheet specs show parameters (resistance, capacitance, offsets, bias currents, etc.) as typical values and tolerances. The equations in previous chapters consider typical values. Component tolerances affect DC and AC performances of the Zmod ADC (). To minimize these effects, the design uses:

- 0.1% resistors and 1% capacitors in all the critical analog signal paths
- Capacitive trimmers for balancing the Scope Input Divider and Gain Selection
- No other mechanical trimmers (as these are big, expensive, unreliable and affected by vibrations, aging, and temperature drifts)
- Software calibration, at manufacturing
- User software calibration, as an option

A software calibration is performed on each device as a part of the manufacturing test. Reference signals are connected to the Scope inputs. A set of measurements is used to identify all the DC errors (Gain, Offset) of each analog stage. Correction (Calibration) parameters are computed and stored in the Calibration Memory, on the Zmod ADC () device, both as Factory Calibration Data and User Calibration Data. The WaveForms software allows the user performing an in-house calibration and overwrite the User Calibration Data. Returning to Factory Calibration is always possible.

The Software reads the calibration parameters from the Zmod ADC () MCU via the I2C bus and uses them to correct the acquired signals. The structure of the calibration data is shown below:

Table 3. The Calibration Data Structure []

Heading 1	Name	Size (Bytes)	Type	Flash Address (Factory Calibration)	EEPROM () Address (User Calibration)
Magic ID		1	uchar 0xAD	0x8100	0x7000
Calibration Time		4	unix timestamp	0x8104	0x7004
Channel 1 LG Gain	CG	4	float32	0x8108	0x7008
Channel 1 LG Offset	CA	4	float32	0x810C	0x700C
Channel 1 HG Gain	CG	4	float32	0x8110	0x7010
Channel 1 HG Offset	CA	4	float32	0x8114	0x7014
Channel 2 LG Gain	CG	4	float32	0x8118	0x7018
Channel 2 LG Offset	CA	4	float32	0x811C	0x701C
Channel 2 HG Gain	CG	4	float32	0x8120	0x7020
Channel 2 HG Offset	CA	4	float32	0x8124	0x7024
Reserved Area		68	-	0x8168	0x7068
Log		22	string	0x817E	0x707E
CRC		1	uchar	0x817F	0x707F

Table 4. The EEPROM Memory Map []

Address	Function	Size (Bytes)
0x7000 - 0x707F	User Calibration	128
0x7080 - 0x70FF	Future Use	128

At the power up the EEPROM () memory is protected against write operations. To disable the write protection one has to write a magic number to a magic address over I2C. To re-enable the write protection one has to write a any other number to the magic address.

Table 5. The Write Protection Disable magic number and address []

Magic Number	Magic Adress
0xD2	0x6FFF

4. Power Supplies and Control

This block includes the internal power supplies.

The Zmod ADC () gets the digital rails from the carrier board, via the SYZYGY connector:

VCC5V0 - used for relays and analog supplies
VCC3V3 - used for the MCU and analog supplies
Vadj = 1.8V - used for the ADC () digital rail

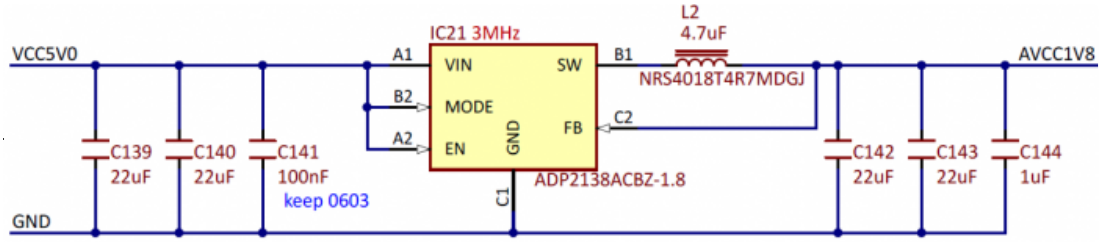
The internal analog rails sequence is:

AVCC1V8 - ADC () analog rail
AVCC3V0 - ADC () driver
AVCC-2V5, AVCC4V5 - Scope buffer, reference voltage

4.1. AVCC1V8

The analog supply AVCC1V8 is built from VCC5V0 using IC21, an ADP2138Fixed Output Voltage, 800mA, 3MHz, Step-Down DC-to-DC converter. To insure low output voltage ripple a second LC filter (FB9 in Fig. 9) is added and forced PWM mode is selected.

- Input voltage: 2.3 V to 5.5 V
  Peak efficiency: 95%
  3 MHz () fixed frequency operation
  Typical quiescent current: 24 µA
- Very small solution size
- 6-lead, 1 mm × 1.5 mm WLCSP package
- Fast load and line transient response
- 100% duty cycle low dropout mode
- Internal synchronous rectifier, compensation, and soft start
- Current overload and thermal shutdown protections
- Ultra-low shutdown current: 0.2 µA (typical)
- Forced PWM and automatic PWM/PSM modes



4.2. AVCC3V0

The analog supply AVCC3V0 is built from VCC3V3 using IC22, an ADP1225.5 V Input, 300 mA, Low Quiescent Current, CMOS Linear Regulator, Fixed Output Voltage. To reduce noise and reduce the crosstalk between supplied circuits, the rail uses individual LC filters: FB3 in Fig. 10, FB6 (Channel 2 ADC () Driver - not shown), FB7 in Fig. 7.

- Input voltage supply range: 2.3 V to 5.5 V
- 300 mA maximum output current
- Fixed and adjustable output voltage versions
- Very low dropout voltage: 85 mV at 300 mA load
- Low quiescent current: 45 µA at no load
- Low shutdown current: <1 µA
- Initial accuracy: ±1% accuracy
- Up to 31 fixed-output voltage options available from
- 1.75 V to 3.3 V
- Adjustable-output voltage range
- 0.8 V to 5.0 V (ADP123)
- Excellent PSRR performance: 60 dB at 100 kHz ()
- Excellent load/line transient response
- Optimized for small 1.0 µF ceramic capacitors
- Current limit and thermal overload protection
- Logic controlled enable
- Compact packages: 5-lead TSOT and 6-lead 2 mm × 2 mm LFCSP

4.3. AVCC4V5

The analog supply AVCC4V5 is built from VCC5V0 using IC19, an ADP123 5.5 V Input, 300 mA, Low Quiescent Current, CMOS Linear Regulator, Adjustable Output Voltage. To reduce noise and reduce the crosstalk between supplied circuits, the rail uses individual LC filters: FB2 in Fig. 6, FB5 (Channel 2 ADC () Buffer - not shown), FB8 in Fig. 9.

- Input voltage supply range: 2.3 V to 5.5 V
- 300 mA maximum output current
- Fixed and adjustable output voltage versions
- Very low dropout voltage: 85 mV at 300 mA load
- Low quiescent current: 45 µA at no load
- Low shutdown current: <1 µA
- Initial accuracy: ±1% accuracy
- Up to 31 fixed-output voltage options available from
- 1.75 V to 3.3 V

- Adjustable-output voltage range
- 0.8 V to 5.0 V (ADP123)
- Excellent PSRR performance: 60 dB at 100 kHz ()
- Excellent load/line transient response
- Optimized for small 1.0 µF ceramic capacitors
- Current limit and thermal overload protection
- Logic controlled enable
- Compact packages: 5-lead TSOT and 6-lead 2 mm × 2 mm LFCSP

4.4. AVCC-2V5

The AVCC-2V5 analog power supply is implemented with the ADP2301 Step-Down regulator in an inverting Buck-Boost configuration. See application Note AN-1083: Designing an Inverting Buck Boost Using the ADP2300 and ADP2301 . To reduce noise and reduce the crosstalk between supplied circuits, the rail uses individual LC filters: FB1 in Fig. 6, FB4 (Channel 2 ADC () Buffer - not shown). The ADP2301 features:

- 1.2 A maximum load current
  ±2% output accuracy over temperature range
  1.4 MHz () switching frequency
  High efficiency up to 91%
- Current-mode control architecture
- Output voltage from 0.8 V to 0.85 × VIN
- Automatic PFM/PWM mode switching
- Integrated high-side MOSFET and bootstrap diode,
- Internal compensation and soft start
- Undervoltage lockout (UVLO), Overcurrent protection (OCP) and thermal shutdown (TSD)
- Available in ultrasmall, 6-lead TSOT package

5. The SYZYGY™ Connector

The SYZYGY™ connector in provides the interface with the carrier board. The used signals are:

- Power rails
  - VCC5V0
  - VCC3V3
  - VADJ - needs to be set by the carier board to 1.8V
  - GND ()
  - Shield
- SYZYGY™ I2C bus:
  - MCU_SCLUSCK
    MCU_SDA_MOSI ()

  ADC () differential input clock
  - CLKIN_ADC ()_P
    CLKIN_ADC ()_N

  ADC () single ended output clock:
  - CLKOUT_ADC () (coupled with GND () in the differential P2C pair)
- R_GA for geographical address identification
  SYNC_ADC () for ADC () internal clock divider synchronization
  ADC () data bus: DOUT_ADC ()_0…13
  ADC () SPI bus:
    CS ()_SC1n
  - SCLK ()_SC
  - SDIO_SC
- relay control
  - SCx_yy_z

6. The SYZYGY™ compatibility table

Table 6. The SYZYGY™ compatibility table []

Parameter	**Value**
Maximum 5V supply current	400mA
Maximum 3.3V supply current	100mA

Parameter	Value
VIO supply voltage	1.8V
Maximum VIO supply current	270mA
Total number of I/O	28
Number of differential I/O pairs	0
Width	Single

Written by Mircea Dabacan, PhD, Technical University of Cluj-Napoca Romania

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1) The “SYZYGY™ ” mark is owned by Opal Kelly.

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