ETM59E-04

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Application Manual

Real Time Clock Module

RX8804 CE

SEIKO EPSON CORPORATION

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ETM59E Revision History

Rev No.	Date	Page	Description
ETM59E-01	16.Apr.2018		Release
ETM59E-02	18.Apr.2018	4	Updated Pull-up Resistor value.
		35	Updated mention of tCD.
		40	EVIN connects to VDD of 32kHz-TCXO.
ETM59E-03	27.Apr.2018	5	Note of Timing chart. I2C bus time out is 1second(Max,) from 2seconds,
		4	Peak Current consumption (2) 50µA(Typ.) from 55µA(Typ.)
		10	8.2.5. Extension register The default value was updated.
		11	8.2.6. Flag register The default value was updated.
		41	9.1.2. Marking layout Frequency stability Mark and Lot Mark was updated.
ETM59E-04	14.Jun.2018	16 40	5) RESET bit it explained detailed function of RESET. 8.15. Figure of 32 kHz-TCXO was updated. SCL and SDA connects to GND.

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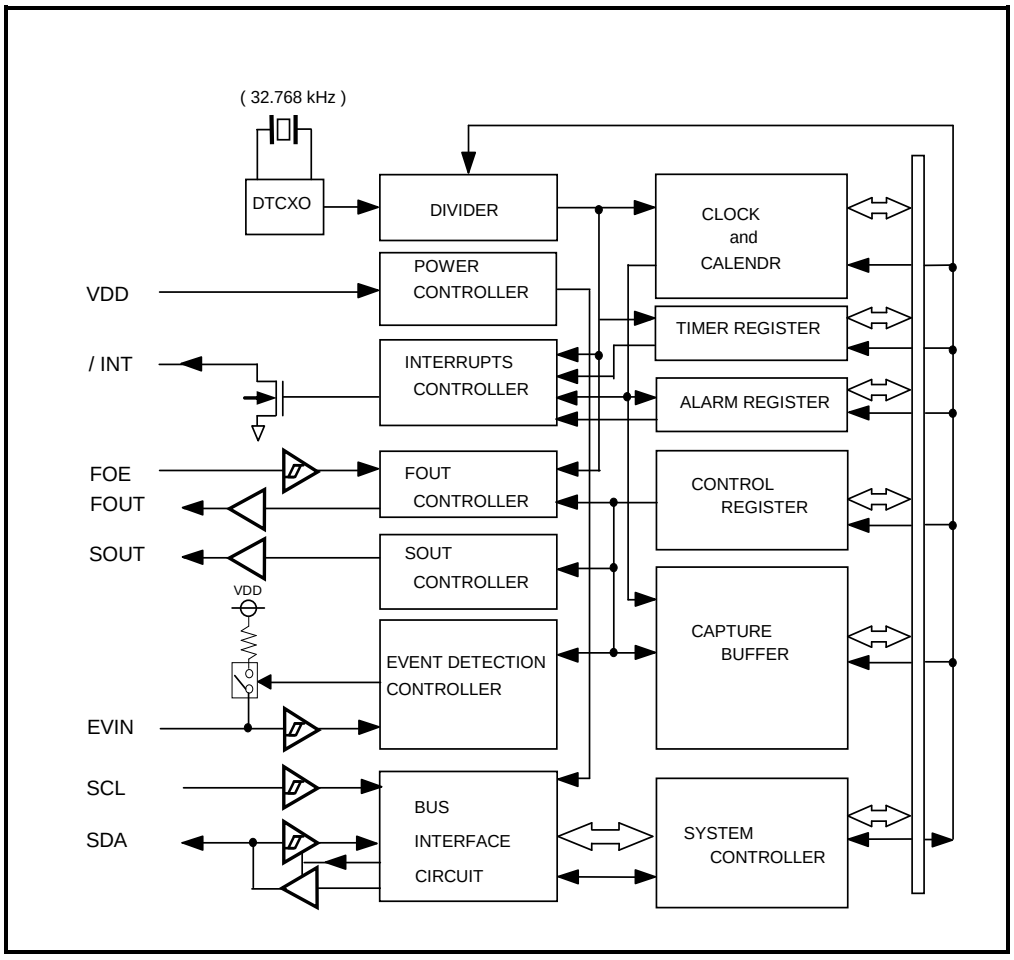
RX8804 CE

- Features built-in 32.768 kHz DTCXO.
- Supports I²C-Bus's high speed mode (Up to 400 kHz)
- Time -Stamp function with EVIN-Pin trigger.
- Outputs to SOUT-Pin of each of detection Flag or others.
- Alarm interrupt function for day, date, hour, and minute settings
- Fixed-cycle timer interrupt function — 244.14 µs to 32 years
- Time update interrupt function — (Seconds, minutes)
- Temperature compensated 32.768 kHz output with OE function — (FOE and FOUT pins)
- Auto correction of leap years — (from 2000 to 2099)
- Wide interface voltage range: 1.6 V to 5.5 V
- Wide time-keeping voltage range:1.5 V to 5.5 V
- Low current consumption: 0.35 µA / 3.0 V (Typ.)

1. Overview

This module is an I2C bus interface-compliant real-time clock which includes a 32.768 kHz DTCXO.
In addition to providing a calendar (year, month, date, day, hour, minute, second) function and a clock counter function, this module provides an abundance of other functions including an alarm function, fixed-cycle timer function, time update interrupt function, 32.768 kHz output function, Time-stamp function with EVIN-pin trigger, and. Programmable output function to SOUT-pin of detection Flag or others.
The devices in this module are fabricated via a C-MOS process for low current consumption, which enables long-term battery back-up.

2. Block Diagram



3. Terminal description

3.1. Terminal connections

RX8804CE

1.	FOE	10.	/ INT
2.	V_{DD}	9.	GND
3.	EVIN	8.	T2
4.	FOUT	7.	SDA
5.	SCL	6.	SOUT

3.2. Pin Functions

Signal name	I/O	Function
SDA	I/O	This pin's signal is used for input and output of address, data, and ACK bits, synchronized with the serial clock used for I^2C communications. Since the SDA pin is an N-ch open drain pin during output, be sure to connect a suitable pull-up resistance relative to the signal line capacity.
SCL	Input	This is the serial clock input pin for I^2C Bus communications.
FOUT	Output	This is the C-MOS output pin with output control provided via the FOE pin. When FOE = "H" (high level), this pin outputs a 32.768 kHz signal. (depend on FSEL bit) When output is stopped, the FOUT pin = Hi-Z (high impedance).
FOE	Input	This is an input pin used to control the output mode of the FOUT pin. When this pin's level is high, the FOUT pin is in output mode. When it is low, output via the FOUT pin is stopped.
/ INT	Output	This pin is used to output alarm signals, timer signals, time update signals, and other signals. This pin is an open drain pin.
EVIN	Input	Trigger input terminal for time-stamps. Built in disconnectable Pull-up resistor.
SOUT	Output	SOUT is push-pull for the inside state output. SOUT outputs state of a specified flag bit or selected logical 1 or 0.
V_{DD}	–	This pin is connected to a positive power supply.
GND	–	This pin is connected to a ground.
T2	–	Use only for testing in the factory. (Do not connect externally.)

Note: Be sure to connect a bypass capacitor rated at least 0.1 µF between V_{DD} and GND.

4. Absolute Maximum Ratings

GND = 0 V

Item	Symbol	Condition	Rating	Unit
Supply voltage	V_{DD}	Between V_{DD} and GND	–0.3 to +6.5	V
Input voltage (1)	V_{IN1}	FOE, SCL, SDA, EVIN pins	ND–0.3 to +6.5	V
Input voltage (2)	V_{IN2}	EVIN pin	GND–0.3 to V_{DD}+0.3	V
Output voltage (1)	V_{OUT1}	FOUT and SOUT pin	GND–0.3 to V_{DD}+0.3	V
Output voltage (2)	V_{OUT2}	SDA and /INT pins	GND–0.3 to +6.5	V
Storage temperature	T_{STG}	When stored separately, without packaging	–55 to +125	°C

5. Recommended Operating Conditions

GND = 0 V

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Operating supply voltage	V_{ACC}	Between V_{DD} and GND	1.6	3.0	5.5	V
Temp. compensation voltage	V_{TEM}	–	1.5	3.0	5.5	V
Clock supply voltage	V_{CLK}	–	1.5	3.0	5.5	V
Operating temperature	T_{OPR}	No condensation	–40	+25	+105	°C

* To apply Min. value of VACC and VCLK, the VDD needs to be supplied with more than 1.5 V at least for the oscillation to stabilize (oscillation start time tSTA).
* The Min. value of VCLK is the Min. voltage required to retain the time counting function; it is however necessary to maintain VTEM till the oscillation of the oscillator has stabilized (oscillation start time tSTA).
* The temperature compensation stops working below Min. value of VTEM.

6. Frequency Characteristics

GND = 0 V

Item	Symbol	Condition		Rating	Unit
Frequency stability	Δf/f	XA	Ta = 0 to +50 °C, V_{DD} = 3.0 V Ta = -40 to +85 °C, V_{DD} = 3.0 V Ta = -85 to +105 °C, V_{DD} = 3.0 V	±1.9[*1] ±3.4[*2] ±8.0[*3]	× 10^{-6}
		XB	Ta = 0 to +50 °C, V_{DD} = 3.0 V Ta = -40 to +85 °C, V_{DD} = 3.0 V Ta = -85 to +105 °C, V_{DD} = 3.0 V	±3.8[*4] ±5.0[*5] ±8.0[*3]	
Frequency/voltage characteristics	f/V	Ta= +25 °C, V_{DD}=1.5 V to 5.5 V		±1.0 Max.	× 10^{-6}/V
FOUT duty cycle	Duty	50% VDD +25 °C, V_{DD}=1.5 V to 5.5 V		50 ± 10	%
Oscillation start time	tSTA	Ta = +25 °C, V_{DD} = 1.5 V ~ 5.5 V Ta = -40 to +85 °C, V_{DD} = 1.6 V to 5.5 V		1.0 Max. 3.0 Max.	s
Aging	fa	Ta = +25 °C, V_{DD} = 3.0 V, first year		±3 Max.	× 10^{-6}/year
Reflow	fref	260 °C (Max.), 2 times		±3[*6] Max.	× 10^{-6}

*1 5 sec error per a month.
*2 9 sec error per a month.
*3 21 sec error per a month.
*4 10 sec error per a month.
*5 13.2 sec error per a month.
*6 The result that it was measured at 25 °C, 24 hours after processing of reflow soldering.

7. Electrical Characteristics

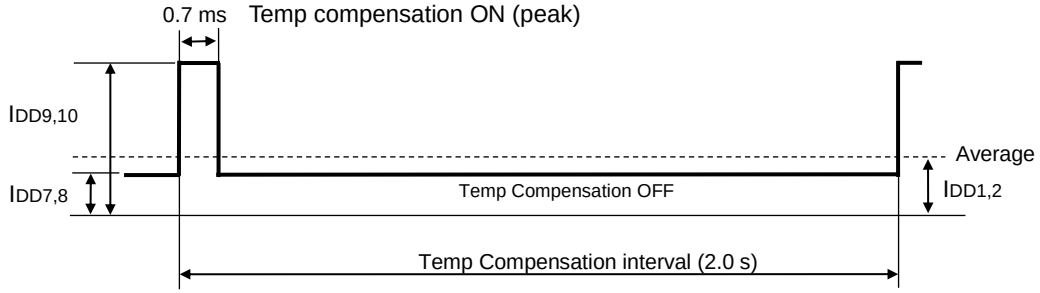
7.1. DC Characteristics

*Unless otherwise specified, GND = 0 V, VDD = 1.5 V to 5.5 V, Ta = −40 °C to +105 °C

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
Average Current consumption(1)	I_{DD1}	fSCL = 0 Hz. / INT = Hi-Z. FOUT is stopped. Temp compensation interval 2.0 s	VDD = 5 V		0.40	1.6	µA
Average Current consumption(2)	I_{DD2}		VDD = 3 V		0.35	1.5	
Average Current consumption(3)	I_{DD3}	fSCL = 0 Hz. / INT = Hi-Z. FOUT outputs 32 kHz. CL = 0 pF Temp compensation interval 2.0 s	VDD = 5 V		1.1	3.1	
Average Current consumption(4)	I_{DD4}		VDD = 3 V		1.0	3.0	
Average Current consumption(5)	I_{DD5}	fSCL = 0 Hz. / INT = Hi-Z. FOUT outputs 32 kHz. CL = 30 pF Temp compensation interval 2.0 s	VDD = 5 V		6.1	8.1	
Average Current consumption(6)	I_{DD6}		VDD = 3 V		4.0	6.0	
Average Current consumption(7)	I_{DD7}	fSCL = 0 Hz. / INT = Hi-Z. FOUT is stopped. Temp compensation is stopped.	VDD = 5 V		0.38	1.55	
Average Current consumption(8)	I_{DD8}		VDD = 3 V		0.33	1.45	
Peak Current consumption(1)	I_{DD9}	fSCL = 0 Hz. / INT = VDD. FOUT is stopped. Temp compensation ON (peak)	VDD = 5 V		55	100	
Peak Current consumption (2)	I_{DD10}		VDD = 3 V		50	95	
High-level input voltage	V_{IH1}	SCL, SDA, FOE		0.8 × VDD		5.5	V
	V_{IH2}	EVIN		0.8 × VDD		VDD	
Low-level input voltage	V_{IL}	SCL, SDA, FOE, EVIN		GND − 0.3		0.2 × VDD	
High-level output voltage	V_{OH1}	FOUT, SOUT	VDD = 5 V, IOH = −1 mA	4.5		5.0	
	V_{OH2}		VDD = 3 V, IOH = −1 mA	2.2		3.0	
	V_{OH3}		VDD = 3 V, IOH = −100 µA	2.9		3.0	
Low-level output voltage	V_{OL1}	FOUT, SOUT	VDD = 5 V, IOL = 1 mA	GND		GND+0.5	
	V_{OL2}		VDD = 3 V, IOL = 1 mA	GND		GND+0.8	
	V_{OL3}		VDD = 3 V, IOL = 100 µA	GND		GND+0.1	
	V_{OL4}	/ INT	VDD = 5 V, IOL = 1 mA	GND		GND+0.25	
	V_{OL5}		VDD = 3 V, IOL = 1 mA	GND		GND+0.4	
	V_{OL6}	SDA	VDD ≥ 2 V, IOL = 3 mA	GND		GND+0.4	
Input leakage current	I_{LK}	INPUT pins, VIN = VDD or GND		−0.5		0.5	µA
Output leakage current	I_{OZ}	Output pins, output voltage = VDD or GND		−0.5		0.5	
Pull-up Resistor	R_{EVIN}	EVIN		125	500	2000	kΩ
Detection voltage of VDET	V_{DET}	VDD		1.41	1.45	1.49	V
Detection voltage of VLF	V_{LOW}	VDD		0.9	1.0	1.2	

- Temperature compensation and consumption current

The current consumption of RX8804 increases at a timing of a temperature compensation.
As for this peak current consumption, it occurs in about 0.7ms.
IDD1, IDD2 is the average current consumption at temperature compensation in 2 seconds cycle.

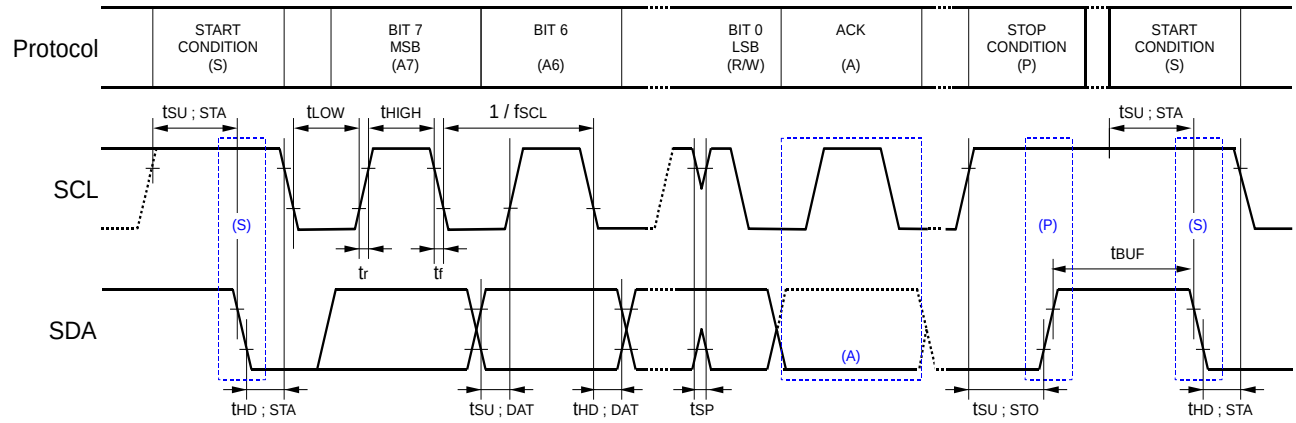


7.2. AC characteristics

* Unless otherwise specified, GND = 0 V , V_{DD} = 1.6 V to 5.5 V , Ta = –40 °C to +105 °C

Item	Symbol	Condition	SCL = 100 kHz (Standard-Mode		SCL = 400 kHz (Fast-Mode)		Unit
			Min.	Max.	Min.	Max.	
SCL clock frequency	f_{SCL}	–	–	100	–	400	kHz
Start condition setup time	$t_{SU;STA}$	–	4.7	–	0.6	–	µs
Start condition hold time	$t_{HD;STA}$	–	4.0	–	0.6	–	µs
Data setup time	$t_{SU;DAT}$	–	250	–	100	–	ns
Data hold time	$t_{HD;DAT}$	–	0	–	0	–	ns
Stop condition setup time	$t_{SU;STO}$	–	4.0	–	0.6	–	µs
Bus idle time between start condition and stop condition	t_{BUF}	–	4.7	–	1.3	–	µs
Time when SCL = "L"	t_{LOW}	–	4.7	–	1.3	–	µs
Time when SCL = "H"	t_{HIGH}	–	4.0	–	0.6	–	µs
Rise time for SCL and SDA	t_r	–	–	1.0	–	0.3	µs
Fall time for SCL and SDA	t_f	–	–	0.3	–	0.3	µs
Allowable spike time on bus	t_{SP}	–	–	50	–	50	ns

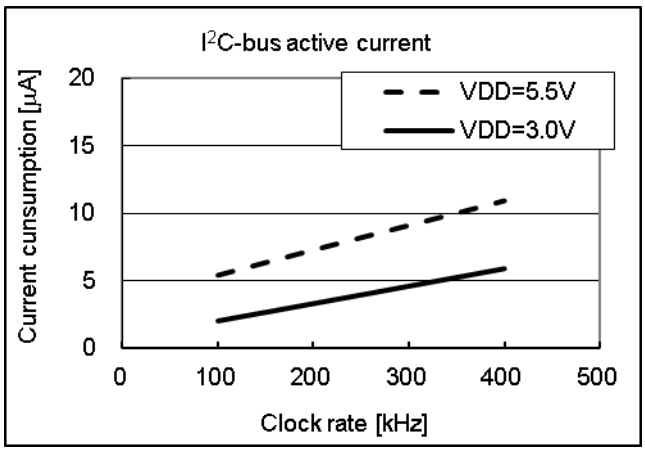
Timing chart



Note:

1. As for the communication of I^2C, completion of less than 1 second is recommended. If such communication requires 1 second (Max.) or longer, the I^2C bus interface is reset by the internal bus timeout function. When bus-time-out occur, SDA turns to Hi-Z input mode.
2. But readout data of a clock is stable anytime, and there isn't contradiction. And it does not occur that data of a clock delay even if access time is prolonged.

Reference characteristic data (Typical) I^2C-bus active current



8. Use Methods

8.1. Description of Registers

8.1.1. Write/Read and Bank Select

Address 00h to 0Fh: Basic time and calendar register. It compatible with RX-8803 and RX8900
Address 10h to 1Fh: Extension register
Access to more than address 20h is possible, but there is some control register for quality inspection. When more than
Address auto increment is looping in lower 4 bits address.
Upper 4bits address are fixed. (00, ..., 0E, 0F, 00, 01) (10, ..., 1E, 1F, 10, 11)

	Basic register	Time stamp register	Access is prohibited
Address (8bit)	0Fh from 00h	1Fh from 10h	FFh from 20h

8.1.2. Register table (Basic time and calendar register)

Address	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Init	Write
00	SEC	○	40	20	10	8	4	2	1		√
01	MIN	○	40	20	10	8	4	2	1		√
02	HOUR	○	○	20	10	8	4	2	1		√
03	WEEK	○	6	5	4	3	2	1	0		√
04	DAY	○	○	20	10	8	4	2	1		√
05	MONTH	○	○	○	10	8	4	2	1		√
06	YEAR	80	40	20	10	8	4	2	1		√
07	RAM	•	•	•	•	•	•	•	•		√
08	MIN Alarm	AE	40	20	10	8	4	2	1		√
09	HOUR Alarm	AE	•	20	10	8	4	2	1		√
0A	WEEK Alarm	AE	6	5	4	3	2	1	0		√
	DAY Alarm		•	20	10	8	4	2	1		
0B	Timer Counter 0	128	64	32	16	8	4	2	1		√
0C	Timer Counter 1	32768	16384	8132	4096	2048	1024	512	256		√
0D	Extension Register	TEST	WADA	USEL	TE	FSEL1	FSEL0	TSEL1	TSEL0	[0:2]	√
0E	Flag Register	○	○	UF	TF	AF	○	VLF	VDET	[0:0]	Clear only
0F	Control Register	CSEL1	CSEL0	UIE	TIE	AIE	○	○	RESET	[4:0]	√

○ Writing is avoid. Read value is 0, always. • It can read and write. √ is available. – avoid.
"Init" shows value of after power-on Reset. Unit is Hex.

Note After the initial power-up (from 0 V) or in case the VLF bit returns "1" , make sure to initialize all registers, before using the RTC.
Be sure to avoid entering incorrect date and time data, as clock operations are not guaranteed when the data or time data is incorrect.

- During the initial power-up, the following are the default settings for the register values
  Initial value_0: TSVLF, TSVDET,TEST, WADA, USEL, TE, FSEL1, FSEL0, TSEL0, UF, TF, AF, CSEL1, UIE, TIE, AIE, RESET, ECP, EHL, EPU, RCE, EIE, ET1, ET0, EF, EVMON, SOE0 ~ SOE7, DCE, DC, SRV, FS0～FS2, TRES, TSTP, All bits of address 1Ch, 1Dh, 1Eh, and 1Fh.
  Initial value_1: TSEL1, VLF,VDET,CSEL0
  ∗ At this point, all other register values are undefined, so be sure to perform a reset before using the module.
- Only a 0 can be written to the UF, TF, AF, VLF, VDET and EF bit.
  The EVMON bit is read only bit.
- Any bit marked with "○" should be used with a value of "0" after initialization.
- Any bit marked with "•" is a RAM bit that can be used to read or write any data.
- The TEST bit is used by the manufacturer for testing. Be sure to set "0" for this bit when writing.
- If an alarm function is not used, registers 08h-0Ah can be used as RAM. (AIE : "0")
- Reading register value of address 0Bh-0Ch and 1Fh is pre-set data.
  If a timer function is not used, register of 0Bh-0Ch and 1Fh can be used as RAM. (TE,TIE : "0")

8.1.3. Register table (Time stamp, EVIN, SOUT, Timer)

Address	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Init	Write
10	Time stamp Seconds	○	40	20	10	8	4	2	1	[0:0]	–
11	Time stamp Minutes	○	40	20	10	8	4	2	1	[0:0]	–
12	Time stamp Hours	○	○	20	10	8	4	2	1	[0:0]	–
13	Time stamp Weekday	○	6	5	4	3	2	1	0	[0:0]	–
14	Time stamp Days	○	○	20	10	8	4	2	1	[0:0]	–
15	Time stamp Months	TSVLF	TSVD	○	10	8	4	2	1	[0:0]	–
16	Time stamp Years	80	40	20	10	8	4	2	1	[0:0]	–
17	EVIN Control	ECP	EHL	EPU	RCE	EIE	○	ET1	ET0	[0:0]	√
18	EVIN Monitor	EF	○	○	○	EVMON	○	○	○	[0:0]	√
19	SOUT Control 1	SOE7	SOE6	SOE5	SOE4	SOE3	SOE2	SOE1	SOE0	[0:0]	√
1A	SOUT Control 2	DCE	DC	○	○	SRV	FS2	FS1	FS0	[0:0]	√
1B	Timer Control	TSTP	TRES	○	○	○	○	○	○	[0:0]	√
1C	Monitor of Timer0	128	64	32	16	8	4	2	1	[0:0]	–
1D	Monitor of Timer1	32768	16384	8192	4096	2048	1024	512	256	[0:0]	–
1E	Monitor of Timer2	8388608	4194304	2097152	1048576	524288	262144	131072	65536	[0:0]	–
1F	Timer Counter 2	8388608	4194304	2097152	1048576	524288	262144	131072	65536	[0:0]	√

○ Writing is avoid. Read value is 0, always. • It can read and write. √ is available. – avoid.
"Init" shows value of after power-on Reset. Unit is Hex.

8.1.4. Quick Reference

Update interrupt timing		Default
USEL = 0	Once per seconds	√
USEL = 1	Once per minutes	
Output Frequency selection		
FSEL1, FSEL0 = 00	32.768 kHz	√
FSEL1, FSEL0 = 01	1024 Hz	
FSEL1, FSEL0 = 10	1 Hz	
FSEL1, FSEL0 = 11	32.768 kHz	
Timer source clock selection		
TSEL1, TSEL0 = 00	4096 Hz	
TSEL1, TSEL0 = 01	64 Hz	
TSEL1, TSEL0 = 10	Every seconds update	√
TSEL1, TSEL0 = 11	Every minutes update	
Temperature compensation selection		
CSEL1, CSEL0 = 00	0.5 sec	
CSEL1, CSEL0 = 01	2.0 sec	√
CSEL1, CSEL0 = 10	10 sec	
CSEL1, CSEL0 = 11	30 sec	

8.2. Details of Registers

8.2.1. Clock counter (SEC - HOUR)

Address	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
00	SEC	○	40	20	10	8	4	2	1
01	MIN	○	40	20	10	8	4	2	1
02	HOUR	○	○	20	10	8	4	2	1

- “o” indicates write-protected bits. A zero is always read from these bits.
- The clock counter counts seconds, minutes, and hours.
- The data format is BCD format. For example, when the “seconds” register value is “0101 1001” it indicates 59 seconds.
- Note with caution that writing non-existent time data may interfere with normal operation of the clock counter.

1) Second counter

Address	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
00	**SEC**	○	40	20	10	8	4	2	1

- This second counter counts from “00” to “01”, “02”, and up to 59 seconds, after which it starts again from 00 seconds.
- When written data to a second register, less than a Second counter (512 Hz from 2 Hz) is cleared to zero. When more highly precise time synchronization is needed, RESET bit is most suitable. When 60 seconds were written to a second register, it returns to 00 second in next update. This special update is the same as plus-adjustment of leap second. This behavior is useful in the adjustments of Leap seconds.

2) Minute counter

Address	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
01	**MIN**	○	40	20	10	8	4	2	1

- This minute counter counts from “00” to “01”, “02”, and up to 59 minutes, after which it starts again from 00 minutes.

3) Hour counter

Address	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
02	**HOUR**	○	○	20	10	8	4	2	1

- This hour counter counts from “00” hours to “01”, “02””o indicates write-protected bits. A zero is always read from these bits.

8.2.2. Calendar counter (WEEK - YEAR)

Address	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
03	WEEK	○	6	5	4	3	2	1	0

- "o" indicates write-protected bits. A zero is always read from these bits.

1) Day of the WEEK counter

- The day (of the week) is indicated by 7 bits, bit 0 to bit 6.
- The day data values are counted as follows: Day 01h → Day 02h → Day 04h → Day 08h → Day 10h → Day 20h → Day 40h → Day 01h → Day 02h, etc.
- The correspondence between days and count values is shown below.

WEEK	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Day	Data [h]
Write/Read	0	0	0	0	0	0	0	**1**	Sunday	01 h
	0	0	0	0	0	0	**1**	0	Monday	02 h
	0	0	0	0	0	**1**	0	0	Tuesday	04 h
	0	0	0	0	**1**	0	0	0	Wednesday	08 h
	0	0	0	**1**	0	0	0	0	Thursday	10 h
	0	0	**1**	0	0	0	0	0	Friday	20 h
	0	**1**	0	0	0	0	0	0	Saturday	40 h
Write prohibit	∗ Do not set "1" to more than one day at the same time. Also, note with caution that any setting other than the seven shown above should not be made as it may interfere with normal operation.								–	–

Address	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
04	DAY	○	○	20	10	8	4	2	1
05	MONTH	○	○	○	10	8	4	2	1
06	YEAR	80	40	20	10	8	4	2	1

- "o" indicates write-protected bits. A zero is always read from these bits.
- The auto calendar function updates all dates, months, and years from January 1, 00 to December 31, 99.
- The data format is BCD format. For example, a date register value of "0011 0001" indicates the 31st.
- Note with caution that writing non-existent date data may interfere with normal operation of the calendar counter.

2) Date counter

Address	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
04	**DAY**	○	○	20	10	8	4	2	1

- The updating of dates by the date counter varies according to the month setting.
- A leap year is set whenever the year value is a multiple of four (such as 04, 08, 12, 88, 92, or 96). In February of a leap year, the counter counts dates from "01", "02", "0"3, to "28", "29", "01", etc.

DAY	Month	Date update pattern
Write/Read	1, 3, 5, 7, 8, 10, or 12	01, 02, 03 ~ 30, 31, 01 ~
	4, 6, 9, or 11	01, 02, 03 ~ 30, 01, 02 ~
	February in normal year	01, 02, 03 ~ 28, 01, 02 ~
	February in leap year	01, 02, 03 ~ 28, 29, 01 ~

3) Month counter

Address	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
05	**MONTH**	○	○	○	10	8	4	2	1

- The month counter counts from 01 (January), 02 (February), and up to 12 (December), then starts again at 01 (January).

4) Year counter

Address	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
06	**YEAR**	Y80	Y40	Y20	Y10	Y8	Y4	Y2	Y1

- The year counter counts from 00, 01, 02 and up to 99, then starts again at 00.
- Any year that is a multiple of four (04, 08, 12, 88, 92, 96, etc.) is handled as a leap year.

8.2.3. Alarm registers

Address	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
08	MIN Alarm	AE	40	20	10	8	4	2	1
09	HOUR Alarm	AE	•	20	10	8	4	2	1
0A	WEEK Alarm	AE	6	5	4	3	2	1	0
	DAY Alarm		•	20	10	8	4	2	1

- The alarm interrupt function is used, along with the AEI, AF, and WADA bits, to set alarms for specified date, day, hour, and minute values.
- When the settings in the above alarm registers and the WADA bit match the current time, the /INT pin goes to low level and “1” is set to the AF bit to report that an alarm interrupt event has occurred.

8.2.4. Fixed-cycle timer control registers

Address	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0B	Timer Counter 0	128	64	32	16	8	4	2	1
0C	Timer Counter 1	32768	16384	8192	4096	2048	1024	512	256
1B	Setup of Timer	TSTP	TRES	○	○	○	○	○	○
1C	Current value of Timer 0	128	64	32	16	8	4	2	1
1D	Current value of Timer 1	32768	16384	8192	4096	2048	1024	512	256
1E	Current value of Timer 2	8388608	4194304	2097152	1048576	524288	262144	131072	65536
1F	Timer Counter 2	8388608	4194304	2097152	1048576	524288	262144	131072	65536

- These registers are used to set the preset countdown value for the fixed-cycle timer interrupt function.
- The **TE, TF, TIE, and TSEL0/1 bits** are also used to set the fixed-cycle timer interrupt function.
- When the value in the above fixed-cycle timer control register just changes from 01h to 00h, the /INT pin goes to low level and “1” is set to the TF bit to report that a fixed-cycle timer interrupt event has occurred.

8.2.5. Extension register

Address	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0D	Extension Register (Default)	TEST (0)	WADA (0)	USEL (0)	TE (0)	FSEL1 (0)	FSEL0 (0)	TSEL1 (1)	TSEL0 (0)

- The default value is loaded after powering up from 0 V, automatically.
- TEST must be always cleared by a zero.
- This register is used to specify the target for the alarm function or time update interrupt function and to select or set operations such as fixed-cycle timer operations.

1) TEST bit

This is the manufacturer's test bit. Its value should always be “0”.
Be careful to avoid writing a “1” to this bit when writing to other bits.

TEST	Data	Description
Write/Read	0	Normal operation mode ＊Default
	1	Setting prohibited (manufacturer's test bit)

2) WADA (Week Alarm/Day Alarm) bit

This bit is used to specify either WEEK or DAY as the target of the alarm interrupt function.
Writing a “1” to this bit specifies a DAY alarm, meaning the alarm interrupt is initiated independent of the actual day when the set time is reached.
Writing a “0” to this bit specifies a WEEK alarm, so an alarm interrupt is only generated when the set time is reached on a dedicated day of a week.

3) USEL (Update Interrupt Select) bit

This bit is used to define if the RTC should output a “second update” or “minute update” interrupt, allowing to synchronize external clocks with the time registers of the RTC.

USEL	Data	update interrupts	Auto reset time tRTN
Write/Read	0	second update ∗ Default	500 ms
	1	minute update	Min. 7.813 ms

4) TE (Timer Enable) bit

This bit controls the start/stop setting for the fixed-cycle timer interrupt function.
Writing a “1” to this bit specifies starting of the fixed-cycle timer interrupt function (a countdown starts from a preset value).
Writing a “0” to this bit specifies stopping of the fixed-cycle timer interrupt function.

5) FSEL0, 1 (FOUT frequency Select 0, 1) bits

The combination of these two bits is used to set the FOUT frequency.
Note: All frequencies are temperature compensated!

FSEL0,1	FSEL1 (bit 3)	FSEL0 (bit 2)	FOUT frequency
Write/Read	0	0	32768 Hz Output ∗ Default
	0	1	1024 Hz Output
	1	0	1 Hz Output
	1	1	32768 Hz Output

6) TSEL0, 1 (Timer Select 0, 1) bits

The combination of these two bits is used to set the countdown period (source clock) for the fixed-cycle timer interrupt function (four settings can be made).

TSEL0,1	TSEL1 (bit 1)	TSEL0 (bit 0)	Source clock
Write/Read	0	0	4096 Hz / Once per 244.14 μs
	0	1	64 Hz / Once per 15.625 ms
	1	0	“Second update” / Once per second
	1	1	“Minute update” / Once per minute

8.2.6. Flag register

Address	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0E	Flag register (Default)	○ (0)	○ (0)	UF (0)	TF (0)	AF (0)	○ (0)	VLF (1)	VDET (1)

1. The default value is the value that is read (or is set internally) after powering up from 0 V.
2. “o” indicates write-protected bits. A zero is always read from these bits.

- This register is used to detect the occurrence of various interrupt events and low voltage which might compromise the reliability of provided time and data.

1) UF (Update Flag) bit

If set to “0” beforehand, this flag bit's value changes from “0” to “1” when a time update interrupt event has occurred. Once this flag bit's value is “1”, its value is retained until a “0” is written to it.
For details, see 8.4. Time Update Interrupt Function.

2) TF (Timer Flag) bit

If set to “0” beforehand, this flag bit's value changes from “0” to “1” when a fixed-cycle timer interrupt event has occurred. Once this flag bit's value is “1”, its value is retained until a “0” is written to it.
For details, see 8.3. Fixed-cycle Timer Interrupt Function.

3) AF (Alarm Flag) bit

If set to “0” beforehand, this flag bit's value changes from “0” to “1” when an alarm interrupt event has occurred. Once this flag bit's value is “1”, its value is retained until a “0” is written to it.
For details, see “8.5. Alarm Interrupt Function”.

4) VLF (Voltage Low Flag) bit

This flag bit indicates the retained status of clock operations or internal data. Its value change from “0” to “1” indicates a possible data loss or time data error due to a supply voltage drop. Once this flag bit's value is “1”, its value is retained until a “0” is written to it.

After powering up from 0 V, make sure to set this bit's value to “1”. Please confirm table in 8.11. Backup and Recovery.

VLF	Data	Description
Write	0	The VLF bit is cleared to zero to prepare for the next status detection.
	1	Invalid (writing a 1 will be ignored)!
Read	0	No supply voltage drops occurred.
	1	Low voltage has been detected, so data loss might have occurred and time information might be compromised. All registers must be initialized. (This setting is retained until a “” is written to this bit.)

5) VDET (Voltage Detection Flag) bit

This flag bit indicates the status of temperature compensation. Its value changes from “0” to “1” when the temperature compensation function has stopped operation due to a supply voltage drop. Once this flag bit's value is 1, its value is retained until a 0 is written to it.

After powering up from 0 V, make sure to set this bit's value to “1”. Please confirm table in 8.11. Backup and Recovery.

VDET	Data	Description
Write	0	The VDET bit is cleared to zero to prepare for the next low voltage detection.
	1	Invalid (writing a 1 will be ignored)!
Read	0	Temperature compensation is normal.
	1	Temperature compensation has been stopped.

8.2.7. Control register

Address	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0F	Control Register (Default)	CSEL1 (0)	CSEL0 (1)	UIE (0)	TIE (0)	AIE (0)	○ (0)	○ (0)	RESET (0)

1. The default value is the value that is read (or is set internally) after powering up from 0 V.
2. "o" indicates write-protected bits. A zero is always read from these bits.

- This register is used to control interrupt event output from the /INT pin and the stop/start status of clock and calendar operations.

1) CSEL0, 1 (Compensation interval Select 0, 1) bits

The combination of these two bits is used to set the temperature compensation interval.

CSEL0,1	CSEL1 (bit 7)	CSEL0 (bit 6)	Compensation interval
Write/Read	0	0	0.5 s
	0	1	2.0 s ＊Default
	1	0	10 s
	1	1	30 s

2) UIE (Update Interrupt Enable) bit

When a time update interrupt event is generated (when the UF bit value changes from 0 to 1), this bit's value specifies if an interrupt signal is generated (/INT status changes from Hi-Z to low) or is not generated (/INT status remains Hi-Z).

When a "1" is written to this bit, an interrupt signal is generated (/INT status changes from Hi-Z to low) when an interrupt event is generated.

When a "0" is written to this bit, no interrupt signal is generated when an interrupt event occurs.

UIE	Data	Function
Write/Read	0	When a time update interrupt event occurs, an interrupt signal is not generated or is canceled (/INT status changes from low to Hi-Z).
	1	When a time update interrupt event occurs, an interrupt signal is generated (/INT status changes from Hi-Z to low). * When a time update interrupt event occurs, low-level output from the /INT pin occurs only when the value of the control register's UIE bit is "1". This /INT status is automatically cleared (/INT status changes from low to Hi-Z) earliest 7.813 ms after the interrupt occurs.

3) TIE (Timer Interrupt Enable) bit

When a fixed-cycle timer interrupt event occurs (when the TF bit value changes from "0" to "1"), this bit's value specifies if an interrupt signal is generated (/INT status changes from Hi-Z to low) or is not generated (/INT status remains Hi-Z).

When a "1" is written to this bit, an interrupt signal is generated (/INT status changes from Hi-Z to low) when an interrupt event is generated.

When a "0" is written to this bit, no interrupt signal is generated when an interrupt event occurs.

TIE	Data	Function
Write/Read	0	When a fixed-cycle timer interrupt event occurs, an interrupt signal is not generated or is canceled (/INT status changes from low to Hi-Z).
	1	When a fixed-cycle timer interrupt event occurs, an interrupt signal is generated (/INT status changes from Hi-Z to low). * When a fixed-cycle timer interrupt event has been generated low-level output from the /INT pin occurs only when the value of the control register's TIE bit is 1. Earliest 7.813 ms after the interrupt occurs, the /INT status is automatically cleared (/INT status changes from low to Hi-Z).

4) AIE (Alarm Interrupt Enable) bit

When an alarm timer interrupt event occurs (when the AF bit value changes from “0” to “1”), this bit's value specifies if an interrupt signal is generated (/INT status changes from Hi-Z to low) or is not generated (/INT status remains Hi-Z).

When a “1” is written to this bit, an interrupt signal is generated (/INT status changes from Hi-Z to low) when an interrupt event is generated.

When a “0” is written to this bit, no interrupt signal is generated when an interrupt event occurs.

AIE	Data	Function
Write/Read	0	When an alarm interrupt event occurs, an interrupt signal is not generated or is canceled (/INT status changes from low to Hi-Z).
	1	When an alarm interrupt event occurs, an interrupt signal is generated (/INT status changes from Hi-Z to low). * When an alarm interrupt event has been generated low-level output from the /INT pin occurs only when the value of the control register's AIE bit is “1””. This setting is retained until the AF bit value is cleared to zero. (No automatic cancellation)

* For details, see “8.7. Alarm Interrupt Function”.

[Caution]
(1) The /INT pin is a shared interrupt output pin for three types of interrupts. It outputs the OR'ed result of these interrupt outputs. When an interrupt has occurred (when the /INT pin is at low level), the UF, TF, read AF flags to determine which flag has a value of 1”
(this indicates which type of interrupt event has occurred).
(2) The status of update interrupt, timer interrupt and alarm interrupt can be checked by software polling without using the /INT pin. In this case, write “0” into UIE, TIE, and AIE bits to avoid physical interrupt generation and thus reduce power consumption.

5) RESET bit

When highly precise synchronization of both time or timer is necessary, use RESET.

RESET	Data	Function
Write/Read	0	The read value of RESET is 0, always. writes 0, it is invalid.
	1	writes 1, it executes reset of count-down-chain from 32.768kHz.

The detailed function of RESET.

For example.
S is start condition. P is stop condition.

[Write access to RESET-bit.]

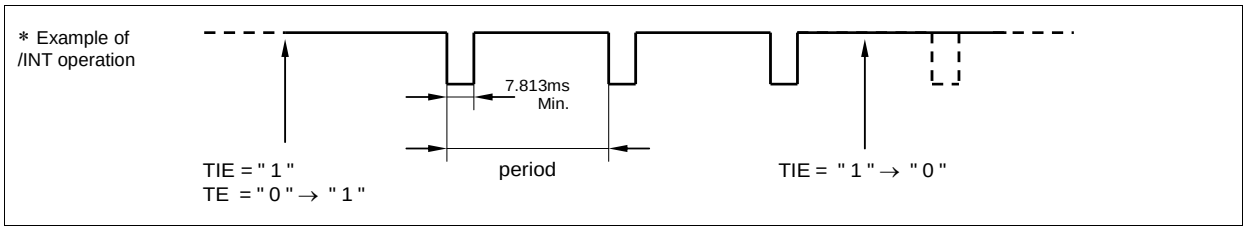
S---Slave address(w)---ACK1---0Fh---ACK2---01h---ACK3---P.

RESET executes and it keeps between P from ACK3.
After P, RESET-bit clears automatically.
reset area of circuit are the count-down-chain of 2 Hz from 16 kHz, are cleared.
As for next update timing of a Seconds counter from RESET.
That range is 1000 ms-30.5 μs from just 1000 ms.
RESET affects time update interruption, alarm, FOUT and timer.
but, it doesn't affect 32 kHz output.

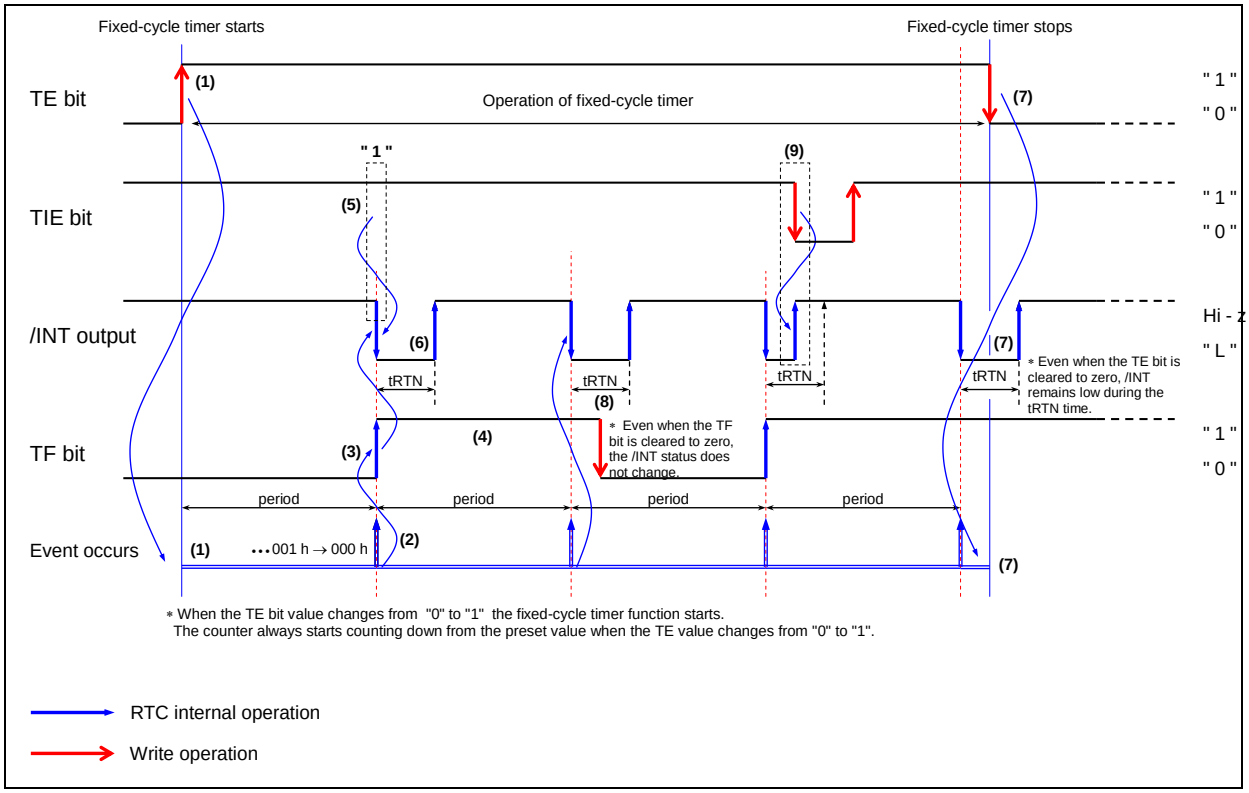
Note:
RESET is released by the reception of a START or RE-START condition before receiving an STOP condition.
The Single write access is recommended for precise RESET.
Unnecessary use of RESET, will be the cause of delay error of time.

8.3. Fixed-cycle Timer Interrupt Function

The fixed-cycle timer interrupt generation function generates an interrupt event periodically at any fixed cycle set between 244.14 µs and 32 years.
When an interrupt event is generated, the /INT pin goes to low level and “1” is set to the TF bit to report that an event has occurred. (However, when a fixed-cycle timer interrupt event has been generated low-level output from the /INT pin occurs only when the value of the control register's TIE bit is “1”. Earliest 7.813 ms after the interrupt occurs, the /INT status is automatically cleared (/INT status changes from low-level to Hi-Z).



8.3.1. Diagram of fixed-cycle timer interrupt function



(1) When a “1” is written to the TE bit, the fixed-cycle timer countdown starts from the preset value.

(2) A fixed-cycle timer interrupt event starts a countdown based on the countdown period (source clock). When the count value changes from 01h to 00h, an interrupt event occurs.
∗ After the interrupt event occurs, the counter automatically reloads the preset value and again starts to count down. (Repeated operation)

(3) When a fixed-cycle timer interrupt event occurs, “1” is written to the TF bit.

(4) When the TF bit = “1” its value is retained until it is cleared to zero.

(5) If the TIE bit = 1 when a fixed-cycle timer interrupt occurs, /INT pin output goes low.
∗ If the TIE bit = “0” when a fixed-cycle timer interrupt occurs, /INT pin output remains Hi-Z.

(6) Output from the /INT pin remains low during the tRTN period following each event, after which it is automatically cleared to Hi-Z status.
∗ /INT is again set low when the next interrupt event occurs.

(7) When a 0 is written to the TE bit, the fixed-cycle timer function is stopped and the /INT pin is set to Hi-Z status.
∗ When /INT = low, the fixed-cycle timer function is stopped. The tRTN period is the maximum amount of time before the /INT pin status changes from low to Hi-Z.

(8) As long as /INT = low, the /INT pin status does not change when the TF bit value changes from “1” to “0”.

(9) When /INT = low, tshe /INT pin status changes from low to Hi-Z as soon as the TIE bit value changes from “1” to ”0”.

8.3.2. Related registers for function of fixed-cycle timer interruption

The fixed-cycle timer interrupt generation function generates an interrupt event periodically at any fixed cycle set between 244.14 s and 16777215 minutes.

Address	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Read	Write
0B	Timer Counter 0	128	64	32	16	8	4	2	1	√	√
0C	Timer Counter 1	32768	16384	8192	4096	2048	1024	512	256	√	√
0D	Extension Register	TEST	WADA	USEL	TE	FSEL1	FSEL0	TSEL1	TSEL0	√	√
0E	Flag Register	O	O	UF	TF	AF	O	VLF	VDET	√	Clear only
0F	Control Register	CSEL1	CSEL0	UIE	TIE	AIE	O	O	RESET	√	√
1B	Setup of Timer	TSTP	TRES	O	O	O	O	O	O	√	√
1C	Monitor of Timer 0	128	64	32	16	8	4	2	1	√	-
1D	Monitor of Timer 1	32768	16384	8192	4096	2048	1024	512	256	√	-
1E	Monitor of Timer 2	8388608	4194304	2097152	1048576	524288	262144	131072	65536	√	-
1F	Timer Counter 2	8388608	4194304	2097152	1048576	524288	262144	131072	65536	√	√

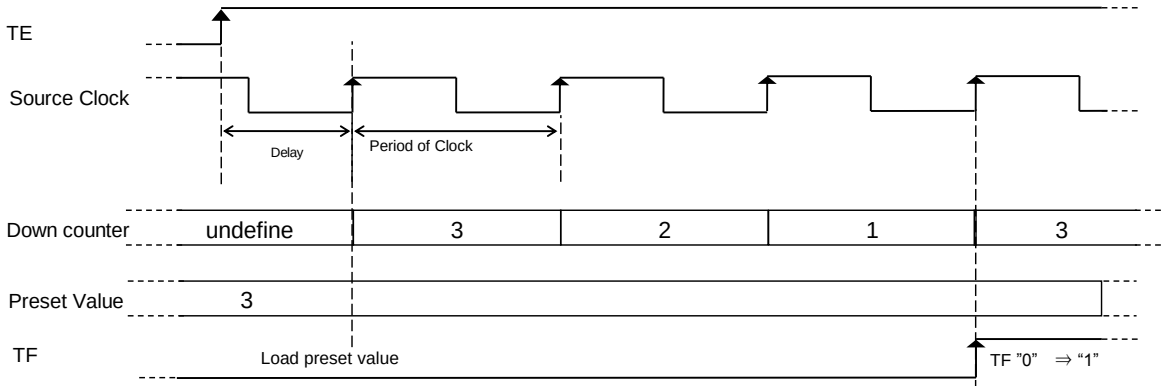
- Timer Counter 0, 1, 2 are preset value of Timer.
- Monitor of Timer 0, 1, 2 are current count value of a timer.
- Before entering settings for operations, we recommend writing a “0” to the TE and TIE bits to prevent hardware interrupts from occurring inadvertently while entering settings.
- When the RESET bit value is “1” the time update interrupt function does not operate.
- When the fixed-cycle timer interrupt function is not using, the fixed-cycle timer counter (0Bh, 0Ch,1Fh), these can use as a RAM register. In such cases, stop the fixed-cycle timer function by writing “0” to the TE and TIE bits.
- When writes 00h to all timer counter, Timer countdown are stop, and new Timer interruption are inhibited.

1) TSEL0, 1 (Timer Select 0, 1) bits

The combination of these two bits is used to set the countdown period (source clock) for the fixed-cycle timer interrupt function (four settings can be made).

TSEL0,1	TSEL1 (bit 1)	TSEL0 (bit 0)	Source clock	Auto reset time tRTN (Min.)	Effects of RESET bits
Write/Read	0	0	4096 Hz / Once per 244.14 µs	122 µs	–
	0	1	*Default 64 Hz / Once per 15.625ms	7.813 ms	* Does not operate when the RESET bit value is “1”.
	1	0	Second” update / Once per second	7.813 ms	
	1	1	“Minute” update / Once per minute	7.813 ms	

1. tRTN is different with a source clock in automatic release time. TF is not cleared automatically.
2. Source clock of 1Hz does not synchronize to update of a second. (It is a 1Hz clock for timers)
3. Source clock 1/60Hz synchronize in update of a minute.
4. A preset value, it is loaded with the first source clock of a timer counter after having set TE.
5. Therefore, two periods of source clocks are needed at the maximum till the first countdown starts after TE=”1”.



When timer count value is 0 from 1, preset value is loaded at the same time by a timer. Therefore, can't monitor 0 of timer counter.

Delay of the first countdown. Preset value is 3.

2) TSTP (Timer STOP) bit

This bit controls the temporarily stopped of Timer Counter.

TSTP	Data	Description
Write/Read	0	Timer Counter are stopped. (don't reset.)
	1	Count down of the Timer Counter are continued.

3) TRES (Timer Reset) bit

This bit can be employed like Watch Dog Timer function.

TRES	Data	Description
Write/Read	0	The Timer Counter is not affected.
	1	Preset value are loaded to all Timer Counters.

4) TE (Timer Enable) bit

This bit controls the start/stop setting for the fixed-cycle timer interrupt function.

TE	Data	Description
Write/Read	0	Preset value loaded to all Timer counter, and count-down stops.
	1	Starts fixed-cycle timer countdown. * The countdown that starts when the TE bit value changes from 0 to 1 always begins from the preset value.

5) TF (Timer Flag) bit

If set to 0 beforehand, this flag bit's value changes from "0" to "1" when a fixed-cycle timer interrupt event has occurred. Once this flag bit's value is "1", its value is retained until a "0" is written to it.

TF	Data	Description
Write	0	The TF bit is cleared to zero to prepare for the next status detection * Clearing this bit to zero does not enable the /INT low output status to be cleared (to Hi-Z).
	1	Invalid (writing a 1 will be ignored)!
Read	0	Fixed-cycle timer interrupt events are not detected.
	1	Fixed-cycle timer interrupt events are detected. (Result is retained until this bit is cleared to zero.)

6) TIE (Timer Interrupt Enable) bit

When a fixed-cycle timer interrupt event occurs (when the TF bit value changes from "0" to "1"), this bit's value specifies whether an interrupt signal is generated (/INT status changes from Hi-Z to low) or is not generated (/INT status remains Hi-Z).

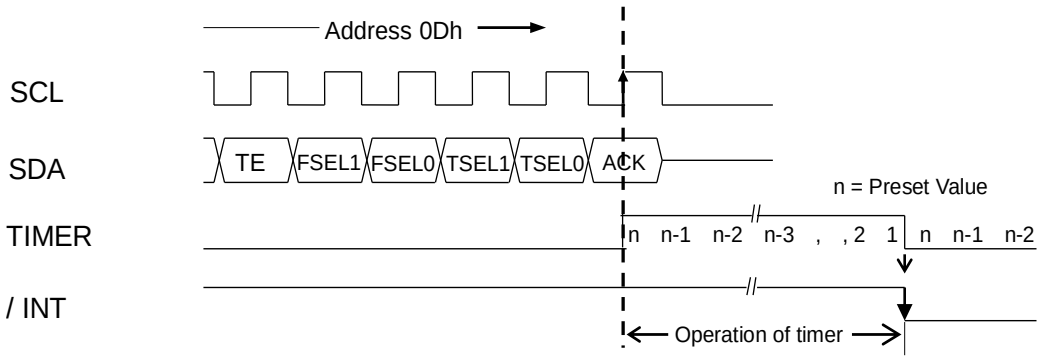
TIE	Data	Description
Write/Read	0	1) When a fixed-cycle timer interrupt event occurs, an interrupt signal is not generated or is canceled (/INT status remains Hi-Z). 2) When a fixed-cycle timer interrupt event occurs, the interrupt signal is canceled (/INT status changes from low to Hi-Z). * Even when the TIE bit value is "0" another interrupt event may change the /INT status to low (or may hold /INT = L).
	1	When a fixed-cycle timer interrupt event occurs, an interrupt signal is generated (/INT status changes from Hi-Z to low). * When a fixed-cycle timer interrupt event has been generated low-level output from the /INT pin occurs only when the value of the control register's TIE bit is 1. Earliest 7.813 ms the interrupt occurs, the /INT status is automatically cleared (/INT status changes from low to Hi-Z).

8.3.3. Fixed-cycle timer interrupt interval (example)

Preset Value	Source clock			
	4096 Hz TSEL1,0 = 0,0	64 Hz TSEL1,0 = 0,1	"Second" update TSEL1,0 = 1,0	"Minute" update TSEL1,0 = 1,1
0	–	–	–	–
1	244.14 μs	15.625 ms	1 s	1 min
2	488.28 μs	31.25 ms	2 s	2 min
⋮	⋮	⋮	⋮	⋮
41	10.010 ms	640.63 ms	41 s	41 min
82	20.020 ms	1.281 s	82 s	82 min
128	31.250 ms	2.000 s	128 s	128 min
192	46.875 ms	3.000 s	192 s	192 min
205	50.049 ms	3.203 s	205 s	205 min
320	78.125 ms	5.000 s	320 s	320 min
410	100.10 ms	6.406 s	410 s	410 min
640	156.25 ms	10.000 s	640 s	640 min
820	200.20 ms	12.813 s	820 s	820 min
1229	300.05 ms	19.203 s	1229 s	1229 min
1280	312.50 ms	20.000 s	1280 s	1280 min
1920	468.75 ms	30.000 s	1920 s	1920 min
2048	500.00 ms	32.000 s	2048 s	2048 min
2560	625.00 ms	40.000 s	2560 s	2560 min
3200	0.7813 s	50.000 s	3200 s	3200 min
3840	0.9375 s	60.000 s	3840 s	3840 min
4095	0.9998 s	63.984 s	4095 s	4095 min
⋮	⋮	⋮	⋮	⋮
16777215	4096 sec.	3 days,49 min.4 sec.	194 days	32 years

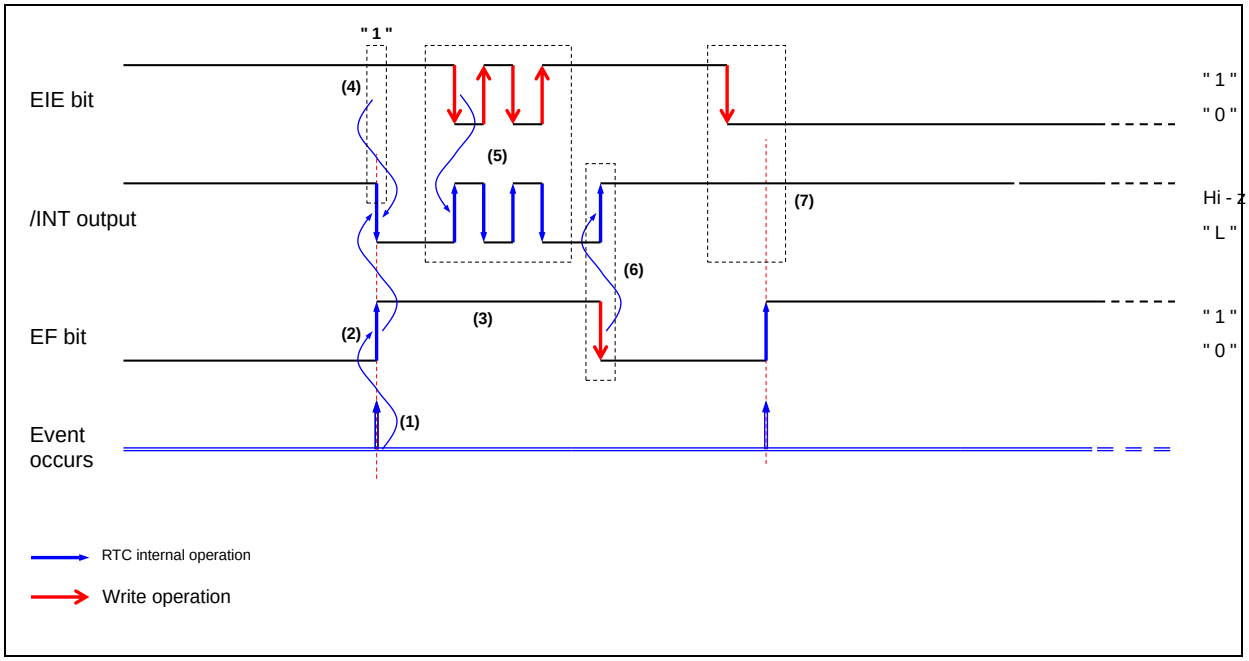
8.3.4. Fixed-cycle timer start timing

Counting down of the fixed-cycle timer value starts at the rising edge of the SCL signal that occurs when the TE value is changed from 0 to “1” (after bit “0” is transferred).



8.4. EVIN Interrupt and Time stamp Function

8.4.1. Diagram of EVIN interrupt function



(1) The EVIN interrupt event occurred.
(2) At the same time, EF bit values becomes “1”.

(3) When the EF bit = “1”, its value is retained until it is cleared to zero.

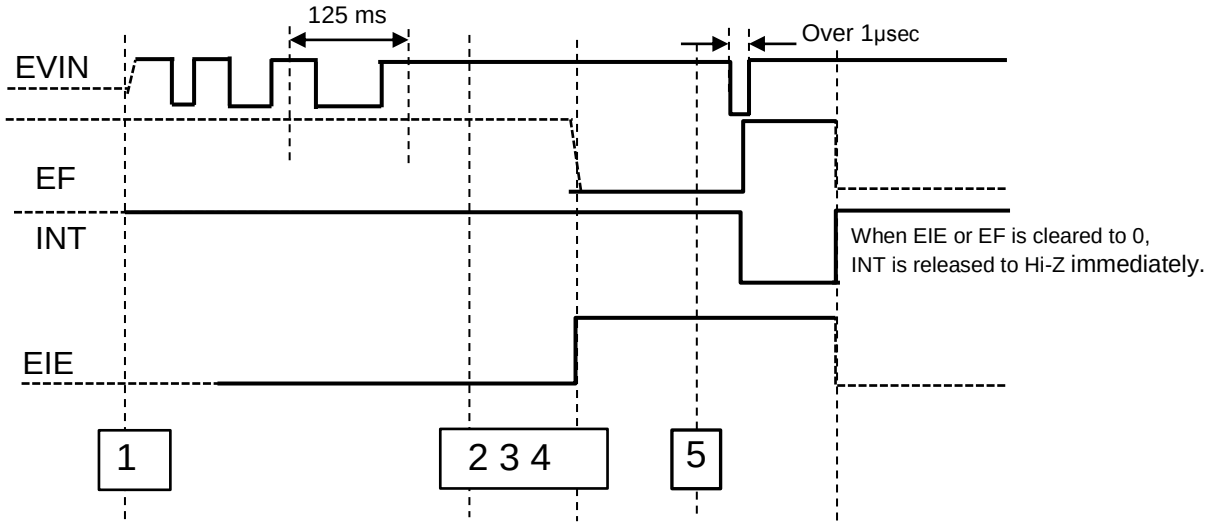
(4) If EIE = “1” when an EVIN interrupt occurs, the /INT pin output goes low.
∗ When an EVIN interrupt event occurs, /INT pin output goes low, and this status is then held until it is cleared via the EF bit or EIE bit.

(5) If the EIE value is changed from “1” to “0” while /INT is low, the /INT status immediately changes from low to Hi-Z. After the alarm interrupt occurs and before the EF bit value is cleared to zero, the /INT status can be controlled via the EIE bit.

(6) If the EF bit value is changed from “1” to “0” while /INT is low, the /INT status immediately changes from low to Hi-Z.

(7) If the EIE bit value is “0” when an EVIN interrupt occurs, the /INT pin status remains Hi-Z.

8.4.2. Operation example of Time-Stamp function.



STEP	Command example Write (Address, Data)	contents	Supplement
1	WriteRX8804(0x17, 0x23)	Disabled Time-stamp function. Low-active is specified. Enables Pull-Up resistor. Disabled repeat detection. Disable interruption of EVIN detection. Debounce period is 125ms	In first, disabled interruption of Event trigger input. Disabled detection of EVIN EVIN level is equal to VDD by EPU EVIN isn't detect. Less than 125ms are ignored.
2	WriteRX8804(0x0F, 0x00)	Disable interruption of Time update, Timer and Alarm.	Enabled only EVIN interruption.
3	WriteRX8804(0x0E, 0x38)	Held UF, TF and AF, and clears VLF and VDET	A value of update is stored at alarm, a timer, the time, and VLF/VDET is initialized.
4	WriteRX8804(0x18, 0x00)	Clears EVIN input detection Flag.	Clear EF
5	WriteRX8804(0x17, 0xA8)	Enables Time-stamp function Low-active is specified Disabled repeat detection Enables Pull-Up resistor Disabled repeat detection Disable interruption of EVIN detection Debounce is disabled	When LOW more than about 1 μ seconds is input into an EVIN terminal after this, date at that time is recorded. EVIN detection interruption signal is output by an INT terminal.

8.4.3. Related registers for EVIN Interrupt and Time stamp Function

Address	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Read	Write
10	Time stamp Seconds	○	40	20	10	8	4	2	1	√	–
11	Time stamp Minutes	○	40	20	10	8	4	2	1	√	–
12	Time stamp Hours	○	○	20	10	8	4	2	1	√	–
13	Time stamp Weekday	○	6	5	4	3	2	1	0	√	–
14	Time stamp Days	○	○	20	10	8	4	2	1	√	–
15	Time stamp Months	TSVLF	TSVDET	○	10	8	4	2	1	√	–
16	Time stamp Years	80	40	20	10	8	4	2	1	√	–
17	EVIN control	ECP	EHL	EPU	RCE	EIE	○	ET1	ET0	√	√
18	EVIN monitor	EF	○	○	○	EVMON	○	○	○	√	√

√ is available. – is not available.

When time stamp trigger was input into an EVIN terminal, time and calendar data copies to address16h from address 10h.
These resisters are read only.

1) Time stamp Seconds data from Year data.
When detect trigger input from EVIN terminal, Clock and calendar data are recorded.

2) TSVLF, TSVDET bit
TSVLF bit copies from VLF bit.
TSVDET bit copies from VDET bit.

3) ECP (Event capture Enable) bit
ECP enables Time Stamp function.

ECP	Data	Function
Write/Read	0	Time-stamp is disabled.
	1	Time-stamp is enabled. Time-stamp data are overwritten by latest time-stamp data.

4) EHL (EVIN pin, High / Low detection select) bit

EHL	Data	Function
Write/Read	0	EVIN pin detects active Low level.
	1	EVIN pin detects active High level.

5) EPU (Enable Pull-Up register) bit
EPU enables Pull-up-resistor of EVIN input terminal.

EPU	Data	Function
Write/Read	0	Pull-up resistor is disabled.
	1	Pull-up resistor is enabled.

6) RCE (Enables repeated Time stamp) bit

RCE	Data	Function
Write/Read	0	After time-stamp, ECP bit is cleared automatically and Time-stamp is not executed, till set ECP to 1, again.
	1	Repeated Time stamp is enabled. After a Time stamp execution, ECP is not cleared to 0. Time-stamp is executed in every event detection, and overwrites to time-stamp register.

7) EIE (EVIN Interrupt Enable) bit

When valid event input occurs (when the EIF bit value changes from “0” to “1”), this bit's value specifies whether an interrupt signal is generated (/INT status changes from Hi-Z to low) or is not generated. (/INT status remains Hi-Z).

EIE	Data	Description
Write/Read	0	1) When a EVIN interrupt event occurs, an interrupt signal is not generated or is canceled (/INT status remains Hi-Z). 2) When a EVIN interrupt event occurs, the interrupt signal is canceled (/INT status changes from low to Hi-Z). ∗ Even when the EIE bit value is “0” another interrupt event may change the /INT status to low (or may hold /INT = “L”).
	1	When a EVIN interrupt event occurs, an interrupt signal is generated (/INT status changes from Hi-Z to low). ∗ When a EVIN interrupt event has been generated low-level output from the /INT pin occurs only when the value of the control register's EIE bit is “1”.

(8) EVMON (EVENT Monitor) bit

EVMON can read the EVIN input level.

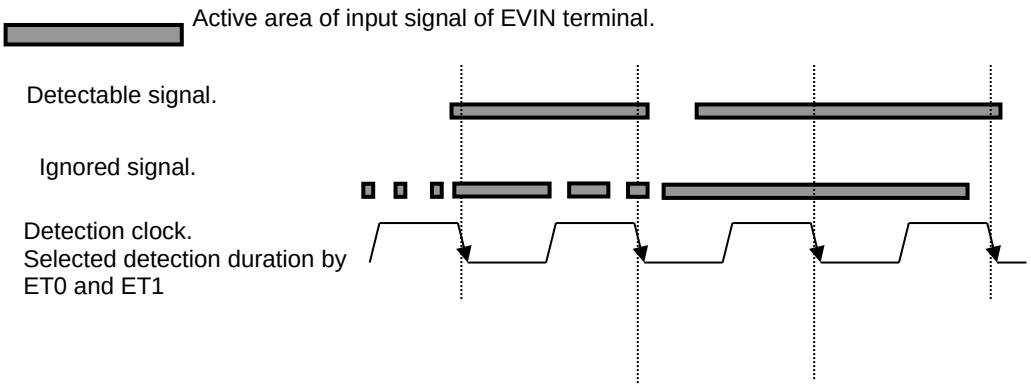
EVMON	Data	Function
Write/Read	0	The input level of EVIN is LOW.
	1	The input level of EVIN is HIGH.

9) ET1bit, ET0 bit Setup debounce duration.

debounce duration.

ET0, 1	**ET1**	**ET0**	duration
Write/Read	0	0	No filtered (*1)
	0	1	3.9 ms
	1	0	15.6 ms
	1	1	125 ms

(*1) Input sensibility.
Input signal width is needed more than about 1µs.



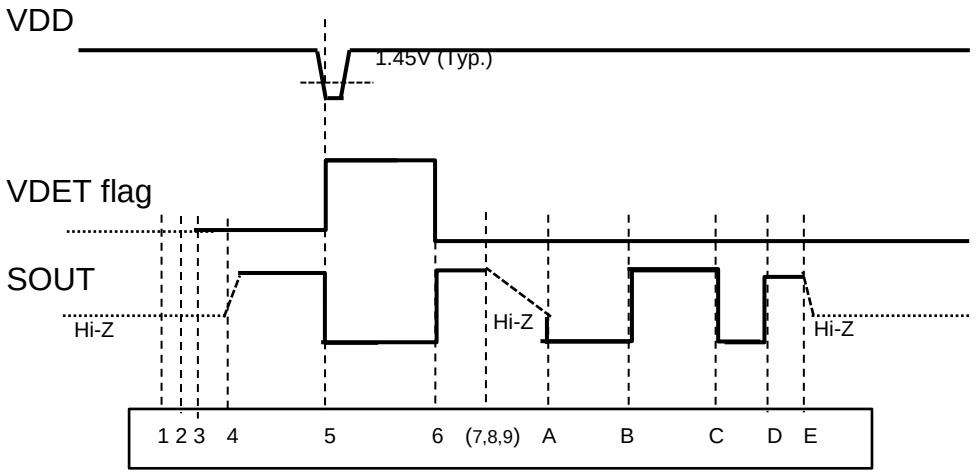
(10) EF (Event trigger Flag) bit

EF	Data	Function
Write/Read	0	Trigger input was not detected from EVIN terminal. When clears to 0, INT output of EVIN are disabled, immediately.
	1	Trigger input was detected from EVIN terminal. EF bit is only cleared by 0. 1 writing is ignored

8.5. SOUT Interrupt Function

Controller can select and use interrupt of a voltage drop or other detection of RTC, as a hardware interruption, and controller can use SOUT like as GPO port.

8.5.1. Operation example of SOUT function.



(Ex.1) When a VDD voltage fell, SOUT outputs active LOW signal.

STEP	Command : example Write (Address, Data)	contents	Supplement
1	WriteRX8804(0x19, 0x00)	SOUT is disabled (Not 0x69)	SOUT is Hi-Z.
2	WriteRX8804(0x0E, 0x3A)	Clear VDET	
3	WriteRX8804(0x1A, 0xC0)	Specified VDET and LOW active by SRV.	
4	WriteRX8804(0x19, 0x69)	SOUT is enabled.	SOUT is HIGH.
5		VDD fell and set VDET.	SOUT outputs active LOW.
6	WriteRX8804(0x0E, 0x3A)	Clear VDET.	
7	WriteRX8804(0x19, 0x00)	SOUT is disabled.	

(Ex.2) SOUT use like a GPO port.

STEP	Command : example Write (Address, Data)	contents	Supplement
8	WriteRX8804(0x19, 0x00)	SOUT is disabled. (Not 0x69)	SOUT is Hi-Z.
9	WriteRX8804(0x1A, 0x80)	SOUT is outputs LOW by direct control.	
A	WriteRX8804(0x19, 0x69)	SOUT is enabled.	SOUT is LOW.
B	WriteRX8804(0x1A, 0XC0)	SOUT is outputs HIGH by direct control.	SOUT is HIGH.
C	WriteRX8804(0x1A, 0x80)	SOUT is outputs LOW by direct control.	SOUT is LOW.
D	WriteRX8804(0x1A, 0XC0)	SOUT is outputs HIGH by direct control.	SOUT is HIGH.
E	WriteRX8804(0x19, 0x00)	SOUT is disabled.	SOUT is Hi-Z.

When system need avoid the Hi-Z output, install Pull-up or pull-down resistor to SOUT if necessary.

8.5.2. Related registers for SOUT interrupt functions.

Address	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
19	SOUT Enable	SOE7	SOE6	SOE5	SOE4	SOE3	SOE2	SOE1	SOE0
1A	SOUT Select	DCE	DC	-	-	SRV	FS2	FS1	FS0

1) SOE0 to SOE7 (SOUT Enable) bits
When value of address 0x19 is 0x69, SOUT pin output function is enabled.
When value of address 0x19 is other value, SOUT pin are disabled.

2) DCE, DC (Direct control enable, Direct control) bits

DCE, DC	**DCE**	**DC**	SOUT status.
Write/Read	0	0	SOUT is output according to SRV, FS0 from FS2.
	0	1	
	1	0	SOUT outputs LOW. SRV doesn't have effect.
	1	1	SOUT outputs HIGH. SRV doesn't have effect.

3) SRV (Reverse SOUT.) bit

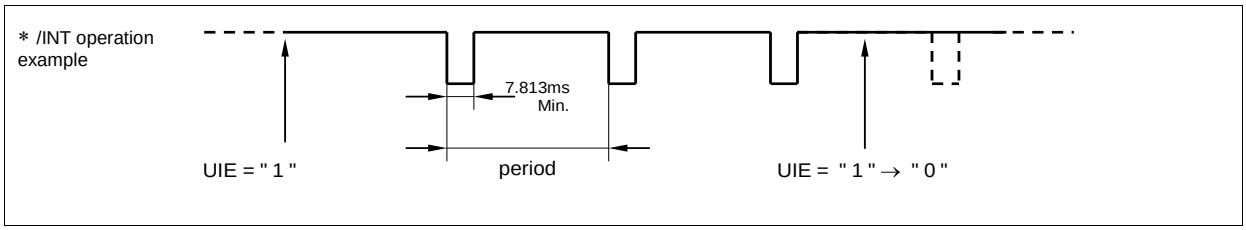
SRV	Data	Description
Write/Read	0	The outputs signal of SOUT is active high
	1	The outputs signal phase of SOUT is inverted. (active Low.)

4) FS (Flag select) bits

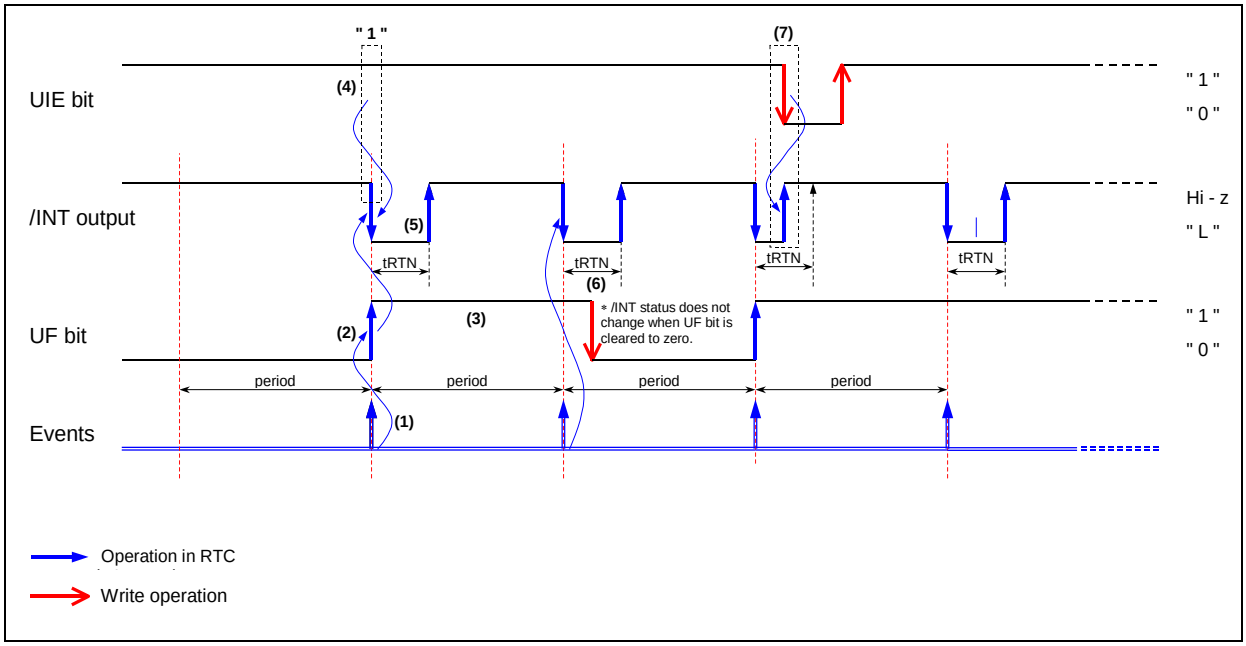
FS0, 1, 2	**FS2**	**FS1**	**FS0**	Select status flag for outputs to SOUT	Availability of SRV
Write/Read	0	0	0	TF (Timer-flag)	SRV is available for inverted outputs polarity
	0	0	1	AF (Alarm flag)	
	0	1	0	UF (Update Flag)	
	0	1	1	EF (Event detection flag)	
	1	0	0	VDET flag	
	1	0	1	VLF flag	
	Other combination			Always low	Not available
				Direct control by DCE and DC.	

8.6. Time Update Interrupt Function

The time update interrupt function generates interrupt events at one-second or one-minute intervals, according to the timing of the internal clock.
When an interrupt event occurs, the UF bit value becomes “1” and the /INT pin goes to low level to indicate that an event has occurred. (However, when a fixed-cycle timer interrupt event has been generated, low-level output from the /INT pin occurs only when the value of the control register's UIE bit is “1”. This /INT status is automatically cleared (/INT status changes from low level to Hi-Z) earliest 7.813 ms (fixed value) after the interrupt occurs.



8.6.1. Time update interrupt function diagram



(1) A time update interrupt event occurs when the internal clock's value matches either the second update time or the minute update time. The USEL bit's specification determines whether it is the second update time or the minute update time that must be matched.

(2) When a time update interrupt event occurs, the UF bit value becomes “1”.

(3) When the UF bit value is “1” its value is retained until it is cleared to zero.

(4) When a time update interrupt occurs, /INT pin output is low if UIE = ”1”.
∗ If UIE = ”0” when a timer update interrupt occurs, the /INT pin status remains Hi-Z.

(5) Each time an event occurs, /INT pin output is low only up to the tRTN time (which is fixed as 7.813 ms for time update interrupts) after which it is automatically cleared to Hi-Z.
∗ /INT pin output goes low again when the next interrupt event occurs.

(6) As long as /INT = low, the /INT pin status does not change, even if the UF bit value changes from “1” to “0”.

(7) When /INT = low, the /INT pin status changes from low to Hi-Z as soon as the UIE bit value changes from “1” to ”0”.

8.6.2. Related registers for time update interrupt functions.

Address	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0D	Extension Register	TEST	WADA	**USEL**	TE	FSEL1	FSEL0	TSEL1	TSEL0
0E	Flag Register	○	○	**UF**	TF	AF	○	VLF	VDET
0F	Control Register	CSEL1	CSEL0	**UIE**	TIE	AIE	○	○	RESET

∗) o indicates write-protected bits. A zero is always read from these bits.

∗ Before entering settings for operations, we recommend writing a “0” to the UIE bit to prevent hardware interrupts from occurring inadvertently while entering settings.

∗ When the RESET bit value is 1 time update interrupt events do not occur.

∗ Although the time update interrupt function cannot be fully stopped, if “0” is written to the UIE bit, the time update interrupt function can be prevented from changing the /INT pin status to low.

1) USEL (Update Interrupt Select) bit

This bit is used to select "second" update or "minute" update as the timing for generation of time update interrupt events.

USEL	Data	Description
Write/Read	0	Selects "second update" (once per second) as the timing for generation of interrupt events
	1	Selects "minute update" (once per minute) as the timing for generation of interrupt events

2) UF (Update Flag) bit

Once it has been set to "0", this flag bit value changes from "0" to "1" when a time update interrupt event occurs. When this flag bit = "1" its value is retained until a "0" is written to it.

UF	Data	Description
Write	0	The UF bit is cleared to zero to prepare for the next status detection ∗ Clearing this bit to zero does not enable the /INT low output status to be cleared (to Hi-Z).
	1	Invalid (writing a 1 will be ignored)!
Read	0	Time update interrupt events are not detected.
	1	Time update interrupt events are detected. (The result is retained until this bit is cleared to zero.)

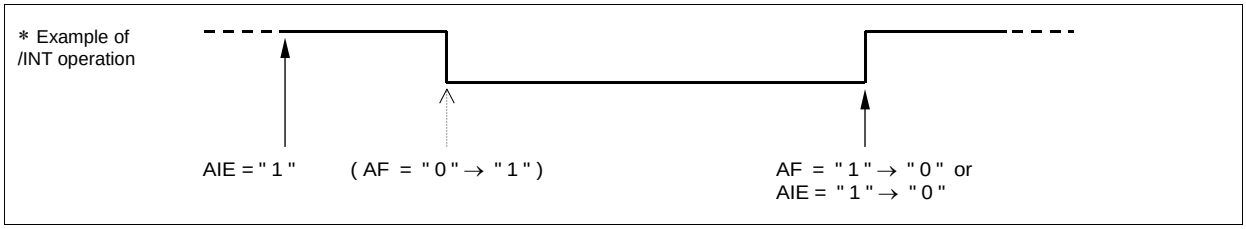
3) UIE (Update Interrupt Enable) bit

When a time update interrupt event occurs (UF bit value changes from “0” to ”1”), this bit selects whether to generate an interrupt signal (/INT status changes from Hi-Z to low) or to not generate it (/INT status remains Hi-Z).

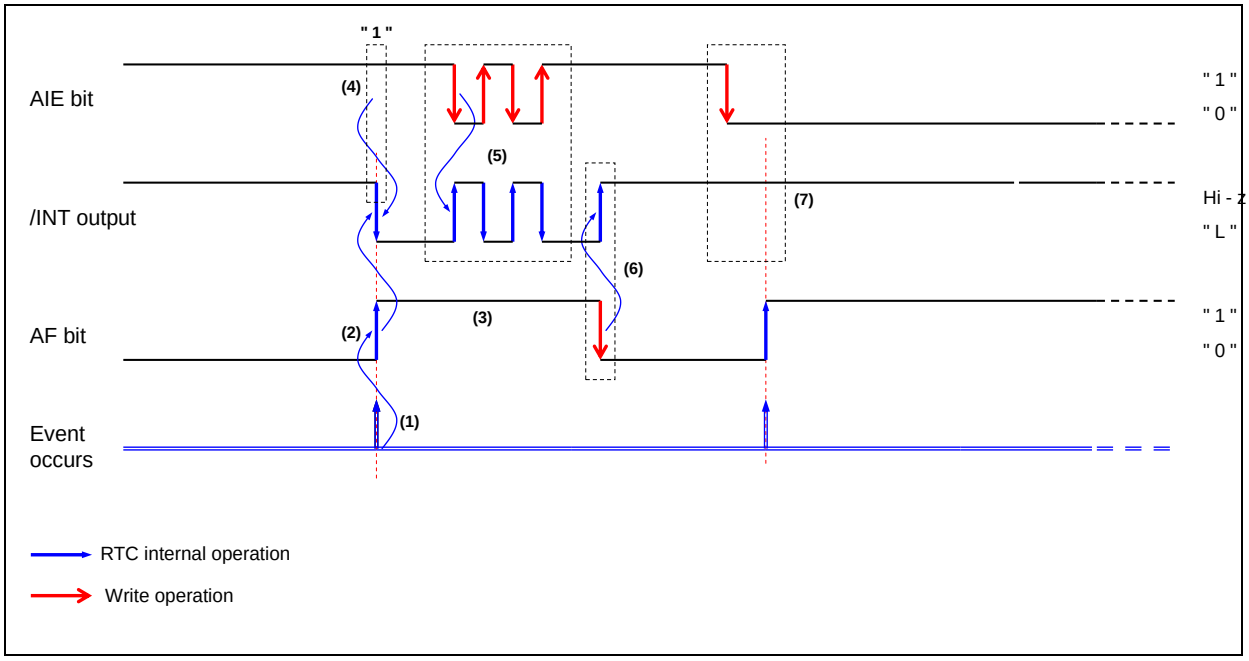
UIE	Data	Description
Write/Read	0	1) Does not generate an interrupt signal when a time update interrupt event occurs (/INT remains Hi-Z) 2) Cancels interrupt signal triggered by time update interrupt event (/INT changes from low to Hi-Z). ∗ Even when the UIE bit value is “0” another interrupt event may change the /INT status to low (or may hold /INT = L).
	1	When a time update interrupt event occurs, an interrupt signal is generated (/INT status changes from Hi-Z to low). ∗ When a time update interrupt event occurs, low-level output from the /INT pin occurs only when the UIE bit value is “1”. Earliest 7.813 ms after the interrupt occurs, the /INT status is automatically cleared (/INT status changes from low to Hi-Z).

8.7. Alarm Interrupt Function

The alarm interrupt generation function generates interrupt events for alarm settings such as date, day, hour, and minute settings.
When an interrupt event occurs, the AF bit value is set to “1” and the /INT pin goes to low level to indicate that an event has occurred.



8.7.1. Diagram of alarm interrupt function



(1) The minute, hour, day and date, when an alarm interrupt event is supposed to occur has to be set in advance, along with the WADA bit (Note) Even if the current date/time is used as the setting, the alarm will not occur until the counter counts up to the current date/time (i.e., an alarm will occur next time, not immediately).

(2) When a time update interrupt event occurs, the AF bit values becomes “1”.

(3) When the AF bit = 1, its value is retained until it is cleared to zero.

(4) If AIE = 1 when an alarm interrupt occurs, the /INT pin output goes low.
* When an alarm interrupt event occurs, /INT pin output goes low, and this status is then held until it is cleared via the AF bit or AIE bit.

(5) If the AIE value is changed from “1” to “0” while /INT is low, the /INT status immediately changes from low to Hi-Z. After the alarm interrupt occurs and before the AF bit value is cleared to zero, the /INT status can be controlled via the AIE bit.

(6) If the AF bit value is changed from “1” to “0” while /INT is low, the /INT status immediately changes from low to Hi-Z.

(7) When the AIE bit value is “0”, and an alarm interrupt occurs, the /INT pin stay Hi-Z.

8.7.2. Related registers for Alarm interrupt function

Address	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
01	MIN	O	40	20	10	8	4	2	1
02	HOUR	O	O	20	10	8	4	2	1
03	WEEK	O	6	5	4	3	2	1	0
04	DAY	O	O	20	10	8	4	2	1
08	MIN Alarm	**AE**	40	20	10	8	4	2	1
09	HOUR Alarm	**AE**	•	20	10	8	4	2	1
0A	WEEK Alarm	**AE**	6	5	4	3	2	1	0
	DAY Alarm		•	20	10	8	4	2	1
0D	Extension Register	TEST	**WADA**	USEL	TE	FSEL1	FSEL0	TSEL1	TSEL0
0E	Flag Register	O	O	UF	TF	**AF**	O	VLF	VDET
0F	Control Register	CSEL1	CSEL0	UIE	TIE	**AIE**	O	O	RESET

∗1) O indicates write-protected bits. A zero is always read from these bits.

∗2) Bits marked with • are RAM bits that can contain any value and are read/write-accessible.

∗ Before entering settings for operations, we recommend writing a “0” to the AIE bit to prevent hardware interrupts from occurring inadvertently while entering settings.

∗ When the RESET bit value is “1” alarm interrupt events do not occur.

∗ When the alarm interrupt function is not being used, the Alarm registers (Reg – 08h to 0Ah) can be used as a RAM register. In such cases, be sure to write “0” to the AIE bit.

∗ When the AIE bit value is “1” and the Alarm registers (Reg – 08h to 0Ah) is being used as a RAM register, /INT may be changed to low level unintentionally.

1) WADA (Week Alarm /Day Alarm) bit

The alarm interrupt function uses either” Day” or “Week” as its target. The WADA bit is used to specify either WEEK or DAY as the target for alarm interrupt events.

WADA	Data	Description
Write/Read	0	Sets WEEK as target of alarm function (DAY setting is ignored)
	1	Sets DAY as target of alarm function (WEEK setting is ignored)

2) Alarm registers

Address	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
08	MIN Alarm	AE	40	20	10	8	4	2	1
09	HOUR Alarm	AE	•	20	10	8	4	2	1
0A	WEEK Alarm	AE	6	5	4	3	2	1	0
	DAY Alarm		•	20	10	8	4	2	1

The minute, hour, day and date when an alarm interrupt event will occur is set using this register and the WADA bit.

In the WEEK alarm /Day alarm register (Reg - 0Ah), the setting selected via the WADA bit determines whether WEEK alarm data or DAY alarm data will be set. If WEEK has been selected via the WADA bit, multiple days can be set (such as Monday, Wednesday, Friday, Saturday).

When the settings made in the alarm registers and the WADA bit match the current time, the AF bit value is changed to 1. At that time, if the AIE bit value has already been set to “1”, the /INT pin goes low.
Note: AE-bit is low active, so in order to enable 1 interrupt every hour once the actual minutes match the alarm setting, it is necessary to set the AE of register 08h to “0” and the AE of 09h and 0Ah to “1”.
In order to generate an alarm interrupt only once a week, all 3 AE-bits have to be clear “0”

∗1) The alarm function is not a HW feature but software function inside the RTC!

*2) In case AE bit of register 0Ah is set to “1”, the day will be ignored and an interrupt occurs ones the actual time matches the minutes and/or hour setting of the alarm register.
(Example) Write 80h (AE = “1”) to the WEEK Alarm /DAY Alarm register (Reg - 0Ah):
Only the hour and minute settings are used as alarm comparison targets. The week and date settings are not used as alarm comparison targets.
As a result, alarm occurs if only the hour and minute values match the alarm data.

∗3) If all three AE bit values are “1” the week/date and time settings are ignored and an alarm interrupt event will occur once per minute.

3) AF (Alarm Flag) bit

When this flag bit value is already set to “0”, occurrence of an alarm interrupt event changes it to “1”. When this flag bit value is “1”, its value is retained until a “0” is written to it.

AF	Data	Description
Write	0	The AF bit is cleared to zero to prepare for the next status detection ∗ Clearing this bit to zero enables /INT low output to be canceled (/INT remains Hi-Z) when an alarm interrupt event has occurred.
	1	Invalid (writing a 1 will be ignored)!
Read	0	Alarm interrupt events are not detected.
	1	Alarm interrupt events are detected. (Result is retained until this bit is cleared to zero.)

4) AIE (Alarm Interrupt Enable) bit

When an alarm interrupt event occurs (when the AF bit value changes from “0” to “1”), this bit's value specifies whether an interrupt signal is generated (/INT status changes from Hi-Z to low) or is not generated (/INT status remains Hi-Z).

AIE	Data	Description
Write/Read	0	1) When an alarm interrupt event occurs, an interrupt signal is not generated or is canceled (/INT status remains Hi-Z). 2) When an alarm interrupt event occurs, the interrupt signal is canceled (/INT status changes from low to Hi-Z). ∗ Even when the AIE bit value is “0” another interrupt event may change the /INT status to low (or may hold /INT = ”L”).
	1	When an alarm interrupt event occurs, an interrupt signal is generated (/INT status changes from Hi-Z to low). ∗ When an alarm interrupt event occurs, low-level output from the /INT pin occurs only when the AIE bit value is “1”. This value is retained (not automatically cleared) until the AF bit is cleared to zero.

8.7.3. Examples of alarm settings

1) Example of alarm settings when “Day” has been specified (and WADA bit = ”0”)

Day is specified WADA bit = “0”	Reg – A								Reg - 9	Reg - 8
	bit 7 AE	bit 6 S	bit 5 F	bit 4 T	bit 3 W	bit 2 T	bit 1 M	bit 0 S	HOUR Alarm	MIN Alarm
Monday through Friday, at 7:00 AM ∗ Minute value is ignored	0	0	1	1	1	1	1	0	07h	80h ~ FFh
Every Saturday and Sunday, for 30 minutes each hour ∗ Hour value is ignored	0	1	0	0	0	0	0	1	80h ~ FFh	30h
Every day, at 6:59 AM	0 1	1 X	1 X	1 X	1 X	1 X	1 X	1 X	18h	59h

X: Don't care

2) Example of alarm settings when Day has been specified (and WADA bit = ”1”)

Day is specified WADA bit = “1”	Reg - A								Reg - 9	Reg - 8
	bit 7 AE	bit 6 •	bit 5 20	bit 4 10	bit 3 08	bit 2 04	bit 1 02	bit 0 01	HOUR Alarm	MIN Alarm
First of each month, at 7:00 AM ∗ Minute value is ignored	0	0	0	0	0	0	0	1	0 h	80h ~ FFh
15th of each month, for 30 minutes each hour ∗ Hour value is ignored	0	0	0	1	0	1	0	1	80h ~ FFh	30h
Every day, at 6:59 PM	1	X	X	X	X	X	X	X	18h	59h

X: Don't care

8.8. About the interrupt function for operation /INT = “L” interrupt output.

1) How to identify events when the interrupt output occurred?
   /INT output pin is common output terminal of interrupt events of three types (Fixed-cycle timer Time interrupt, alarm interrupt, time update interrupt).
   When an interrupt occurs, please read the TF, AF, UF flag to confirm which types of events occurred.
2) Processing method when not using an interrupt output.
   1. Please keep interrupt pin not connected.
   2. Please set “0” to TIE, AIE, and UIE bits.

8.9. Temperature compensation function.

8.9.1. Temperature compensation function

During the production process of the RTC, we are programming the individual characteristics of the built-in crystal into the non-volatile memory of the RTC. The build-in temperature sensor measures the actual temperature of the module and compensates the oscillation frequency of the crystal oscillator using the stored compensation data. This way not only the time information is temperature compensated, but as well the FOUT signal, even when outputting 32.768 kHz. This function works in the supply voltage range VTEM.

8.9.2. Related registers for temperature compensation function

Address	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0F	Control Register	**CSEL1**	**CSEL0**	UIE	TIE	AIE	○	○	RESET

1) CSEL1, CSEL0 (Compensation Interval Select 1, 0) bit
   This bit sets an interval of a temperature compensation operation.
   Current consumption decreases when increasing the Compensation Interval by means CSEL1, 0. CSEL1, 0 is set at the time of initial power-up to (“0”, “1”).

CSEL1	**CSEL0**	Compensation Interval
0	0	0.5 s
0	1	2.0 s
1	0	10 s
1	1	30 s

Even if the power supply voltage falls below VTEM and a VDET bit is set to “1”, the temperature compensation operation is performed again if the supply voltage raises above VTEM.

8.10. Reading/Writing Data via the I²C Bus Interface

8.10.1. Overview of I2C-BUS

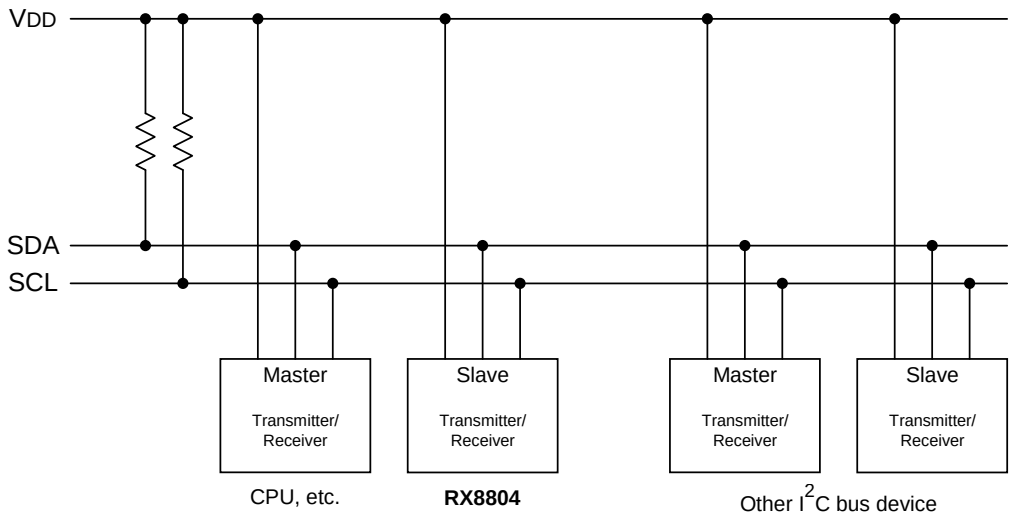
The I²C bus supports bi-directional communications via two signal lines: the SDA (data) line and SCL (clock) line. A combination of these two signals is used to transmit and receive communication start/stop signals, data transfer signals, acknowledge signals, and so on.

Both the SCL and SDA signals are held at high level whenever communications are not being performed.
The starting and stopping of communications is controlled at the rising edge or falling edge of SDA while SCL is at high level.

During data transfers, data changes that occur on the SDA line are performed while the SCL line is at low level, and on the receiving side the data is output while the SCL line is at high level.
The I²C bus device does not include a chip select pin such as is found in ordinary logic devices. Instead of using a chip select pin, slave addresses are allocated to each device and the receiving device responds to communications only when its slave address matches the slave address in the received data. In either case, the data is transferred via the SCL line at a rate of one bit per clock pulse.

8.10.2. System configuration

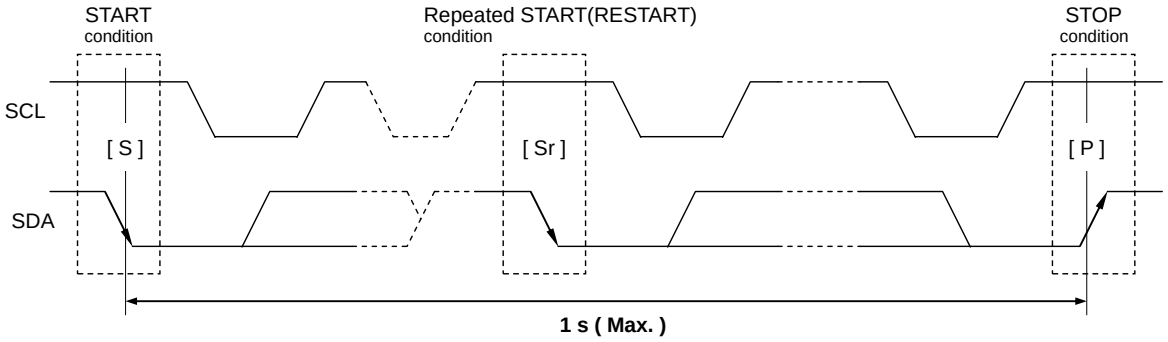
All ports connected to the I2C bus must be either open drain or open collector ports in order to enable "AND-connections" to multiple devices.
SCL and SDA are both connected to the VDD line via a pull-up resistance. Consequently, SCL and SDA are both held at high level when the bus is released (when communication is not being performed).



Any device that controls the data transmission and data reception is defined as a "Master".
And any device that is controlled by a master device is defined as a "Slave".
The device transmitting data is defined as a "Transmitter" and the device receiving data is defined as a "receiver"

In the case of this RTC module, controllers such as a CPU are defined as master devices and the RTC module is defined as a slave device. When a device is used for both transmitting and receiving data, it is defined as either a transmitter or receiver depending on these conditions.

8.10.3. Starting and stopping I^2C bus communications



1) START condition, repeated START condition, and STOP condition

(1) START condition

- The SDA level changes from high to low while SCL is at high level.

(2) STOP condition

- This condition regulates how communications on the I^2C-BUS are terminated. The SDA level changes from low to high while SCL is at high level.

(3) Repeated START condition (RESTART condition)

- In some cases, the START condition occurs between a previous START condition and the next STOP condition, in which case the second START condition is distinguished as a RESTART condition. Since the required status is the same as for the START condition, the SDA level changes from high to low while SCL is at high level.

2) Caution points

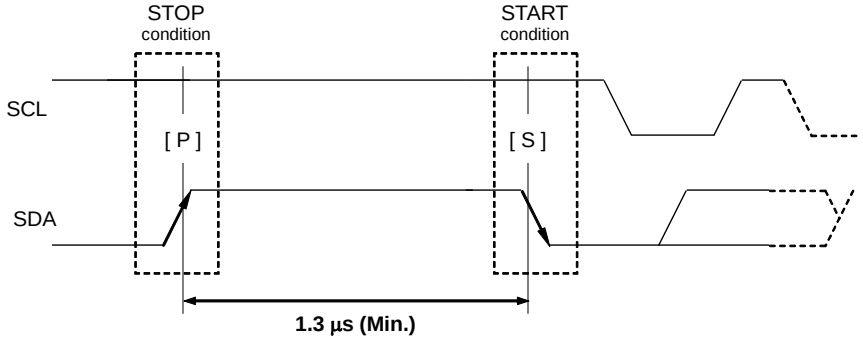
∗1) The master device always controls the START, RESTART, and STOP conditions for communications.

∗2) The master device does not impose any restrictions on the timing by which STOP conditions affect transmissions, so communications can be forcibly stopped at any time while in progress. (However, this is only when this RTC module is in receiver mode (data reception mode = SDA released).

∗3) When communicating with this RTC module, the series of operations from transmitting the START condition to transmitting the STOP condition should occur **within 1 seconds**. (A RESTART condition may be sent between a START condition and STOP condition, but even in such cases the series of operations from transmitting the START condition to transmitting the STOP condition should still occur **within 1 second**.)

If this series of operations requires **1 seconds or longer,** the I^2C bus interface will be automatically cleared and set to standby mode by this RTC module's bus timeout function. Note with caution that both write and read operations are invalid for communications that occur during or after this auto clearing operation. (When the read operation is invalid, all data that is read has a value of “1”).
Restarting of communications begins with transfer of the START condition again

∗4) When communicating with this RTC module, wait **at least 1.3 µs (see the tBUF rule)** between transferring a STOP condition (to stop communications) and transferring the next START condition (to start the next round of communications).

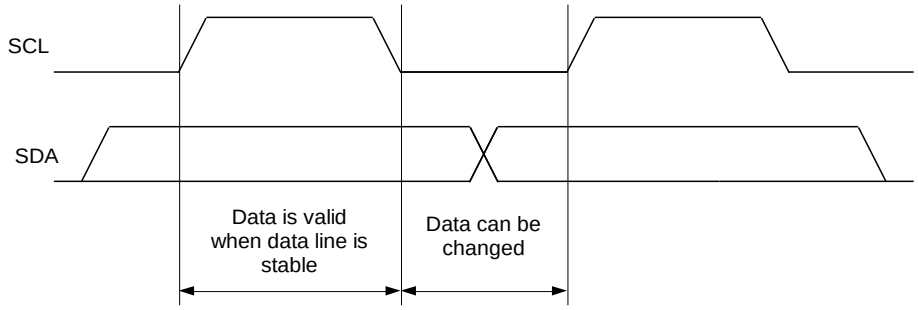


8.10.4. Data transfers and acknowledge responses during I^2C-BUS communications

1) Data transfers

Data transfers are performed in 8-bit (1 byte) units once the START condition has occurred. There is no limit on the amount (bytes) of data that are transferred between the START condition and STOP condition.
(**However, the transfer time must be no longer than 1 second**.)

Updating of data on the transmitter (transmitting side)'s SDA line is performed while the SCL line is at low level. The receiver (receiving side) receives data while the SCL line is at high level.

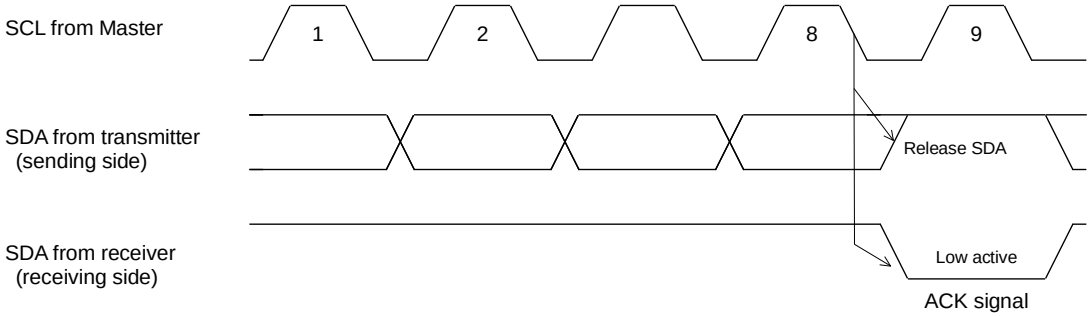


∗ Note with caution that if the SDA data is changed while the SCL line is at high level, it will be treated as a START, RESTART, or STOP condition.

2) Data acknowledge response (ACK signal)

When transferring data, the receiver generates a confirmation response (ACK signal, low active) each time an 8-bit data segment is received. If there is no ACK signal from the receiver, it indicates that normal communication has not been established. (This does not include instances where the master device intentionally does not generate an ACK signal.)

Immediately after the falling edge of the clock pulse corresponding to the 8th bit of data on the SCL line, the transmitter releases the SDA line and the receiver sets the SDA line to low (= acknowledge) level.



After transmitting the ACK signal, if the Master remains the receiver for transfer of the next byte, the SDA is released at the falling edge of the clock corresponding to the 9th bit of data on the SCL line. Data transfer resumes when the Master becomes the transmitter.
When the Master is the receiver, if the Master does not send an ACK signal in response to the last byte sent from the slave, that indicates to the transmitter that data transfer has ended. At that point, the transmitter continues to release the SDA and awaits a STOP condition from the Master.

8.10.5. Slave address

The I^2C bus device does not include a chip select pin such as is found in ordinary logic devices. Instead of using a chip select pin, slave addresses are allocated to each device.
All communications begin with transmitting the [START condition] + [slave address (+ R/W specification)]. The receiving device responds to this communication only when the specified slave address it has received matches its own slave address.

Slave addresses have a fixed length of 7 bits. This RTC's slave address is **[0110 010*]**.
An R/W bit ("*" above) is added to each 7-bit slave address during 8-bit transfers.

	Transfer data	Slave address							R/W bit
		bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Read	**65 h**	**0**	**1**	**1**	**0**	**0**	**1**	**0**	1 (= Read)
Write	**64 h**								0 (= Write)

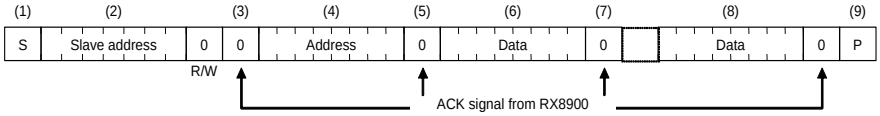
8.10.6. I²C bus protocol

In the following sequence descriptions, it is assumed that the CPU is the master and the RX8804 is the slave.

a. Address specification write sequence

Since the RX8804 includes an address auto increment function, once the initial address has been specified, the RX8804 increments (by one byte) the receive address each time data is transferred.

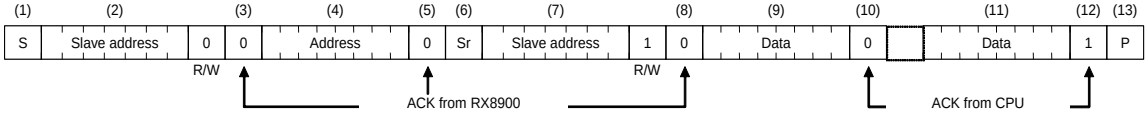
(1) CPU transfers start condition [S].
(2) CPU transmits the RX8804's slave address with the R/W bit set to write mode.
(3) Check for ACK signal from RX8804.
(4) CPU transmits write address to RX8804.
(5) Check for ACK signal from RX8804.
(6) CPU transfers write data to the address specified at (4) above.
(7) Check for ACK signal from RX8804.
(8) Repeat (6) and (7) if necessary. Addresses are automatically incremented.
(9) CPU transfers stop condition [P].



b. Address specification read sequence

After using write mode to write the address to be read, set read mode to read the actual data.

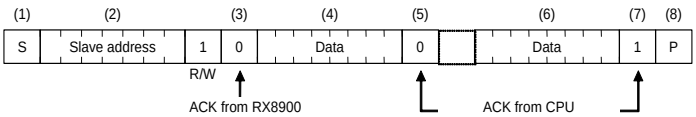
(1) CPU transfers start condition [S].
(2) CPU transmits the RX8804's slave address with the R/W bit set to write mode.
(3) Check for ACK signal from RX8804.
(4) CPU transfers address for reading from RX8804.
(5) Check for ACK signal from RX8804.
(6) CPU transfers RESTART condition [Sr] (in which case, CPU does not transfer a STOP condition [P]).
(7) CPU transfers RX8804's slave address with the R/W bit set to read mode.
(8) Check for ACK signal from RX8804 (from this point on, the CPU is the receiver and the RX8804 is the transmitter).
(9) Data from address specified at (4) above is output by the RX8804.
(10) CPU transfers ACK signal to RX8804.
(11) Repeat (9) and (10) if necessary. Read addresses are automatically incremented.
(12) CPU transfers ACK signal for “1”.
(13) CPU transfers stop condition [P].



c. Read sequence when address is not specified

Once read mode has been initially set, data can be read immediately. In such cases, the address for each read operation is the previously accessed address + 1.

(1) CPU transfers start condition [S].
(2) CPU transmits the RX8804's slave address with the R/W bit set to read mode.
(3) Check for ACK signal from RX8804 (from this point on, the CPU is the receiver and the RX8804 is the transmitter).
(4) Data is output from the RX8804 to the address following the end of the previously accessed address.
(5) CPU transfers ACK signal to RX8804.
(6) Repeat (4) and (5) if necessary. Read addresses are automatically incremented in the RX8804.
(7) CPU transfers ACK signal for “1”.
(8) CPU transfers stop condition [P].



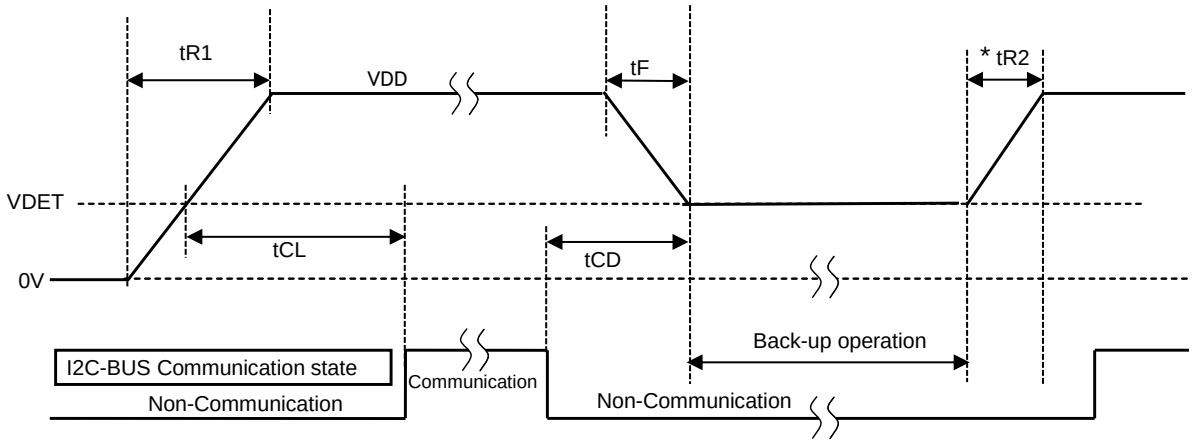
d. The address auto increment in Read/Write.

(1) In Basic time and calendar resister.
Address - - - - - - - 08 - 09 - 0A - 0B - 0C - 0D - 0E - 0F - 00 - 01 - 02 - -

(2) In Extension resister
Address - - - - - - - 18 - 19 - 1A - 1B - 1C - 1D - 1E - 1F - 10 - 11 - 12 - -

- This circuit is sensitive to power supply noise and supply voltage should be stabilized to avoid negative impact on the accuracy.
- tR1 is needed for a proper power-on reset. If this power-on condition cannot be kept, it is necessary to send an initialization routine to the RTC by software.
- In case of repeated ON/OFF of the power supply within short term, it is possible that the power-on reset becomes unstable.
- After power-OFF, keep VDD = GND for more than 10 seconds for a proper power-on reset.
  When it is impossible, please initialize the RTC by the software.
- As for the communication of I2C, completion of less than 1 second is recommended.
- If such communication requires 2 seconds (Max.) or longer, the I2C bus interface is reset by the internal bus timeout function.
- When bus-time-out occur, SDA turns to Hi-Z input mode.
- But readout data of a clock is stable anytime, and there isn't contradiction.

And it does not occur that data of a clock delay even if access time is prolonged.



Item	Symbol	Condition	Min.	Typ.	Max.	Unit.
Power supply rise time1	tR1	VDD = VSS to 5.5 V	1	-	10	ms/V
Access wait time (After initial power on)	tCL	After VDD = VDET	30	-	-	ms
Power supply fall time	tF	VDD = 5.5 V to VDET	100	-	-	µs/V
Power supply rise time2	tR2	VDD = VDET to 5.5 V	15	-	-	µs/V
Setup time from Finish of I2C.	tCD	Before VDD = VDET	0	-	-	µs

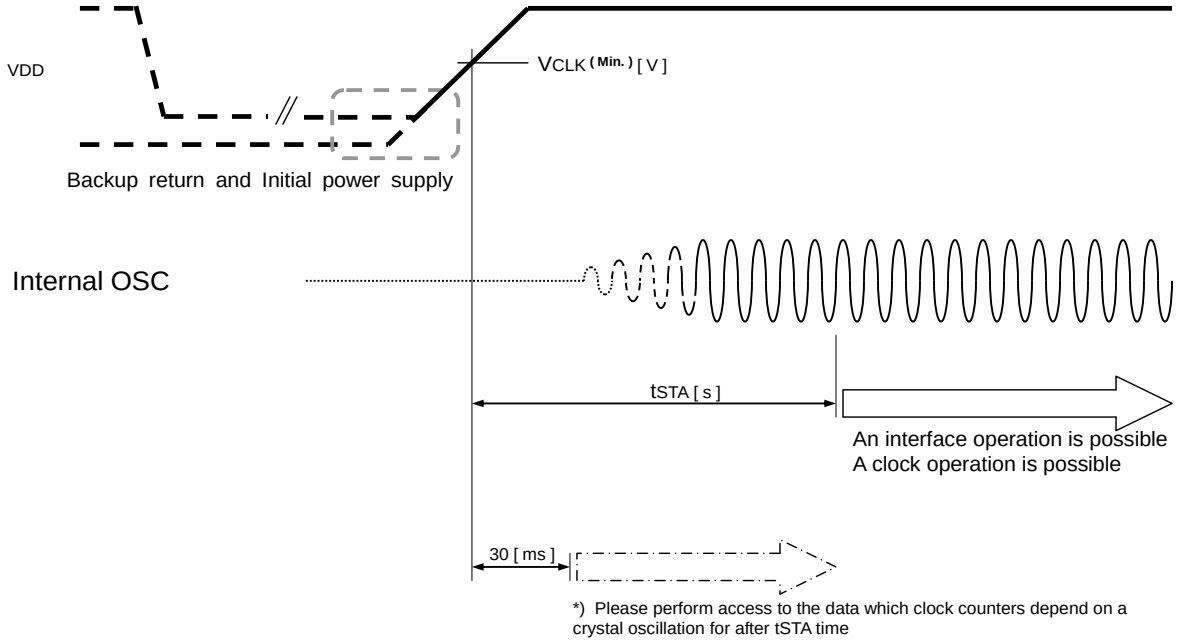
*: tR2 is specifications for an oscillation not to stop. Some clocks are not output by an FOUT terminal.

8.12. About access at the time of backup return and initial power supply

Because most of RTC registers are synchronized with the oscillation clock of the built-in crystal oscillator, the RTC does not work normally without the integrated oscillator having stabilized. Please initialize the RTC at the time the power supply voltage returns (VLF = 1) after the oscillation has stabilized (after oscillation start time tSTA).

If intending to access the RTC after the main supply voltage returns, please note following points:

1. Please begin to read VLF-bit first.
2. If VLF-bit returns “1”, please initialize all registers. Please perform initial setting only tSTA (oscillation start time), when the built-in oscillation is stable.
3. Access is prohibited within 30 ms the supply voltage exceeds min. VCLK (clock supply voltage (VDD > 1.5 V).
4. If VLF-bit returns “0”, access is possible without waiting time.
5. Before the internal crystal oscillator has stabilized (tSTA), no clock operation is possible and time is not counted.

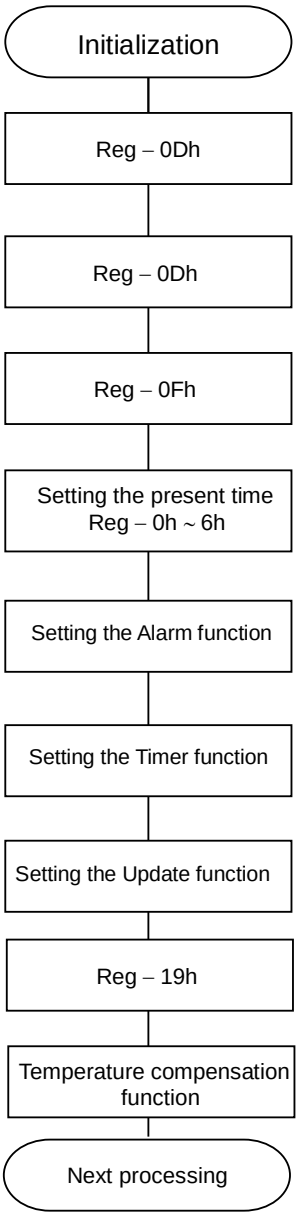


8.13. Flow chart

The following flow-chart is one example, but it is not necessarily applicable for every use-case and not necessarily the most effective process for individual applications.

1) An example of the initialization

Ex.1 Initialize



- Set TE bit to “0”.
- Set FSEL1, 0 bit optionally.

- SET TEST bit to “0”.
- Clear VDET, VLF bit to “0”.

- Set AIE, TIE, UIE bit to “0 " to prevent unprepared interruption output.

- Set the present time.
  ∗ Setting the present time concerned, please refer to item of [Clock and calendar writing] .

- Set the Alarm interrupt function.
  When the alarm interrupt function is not being used, the Alarm registers can be used as a RAM register. In such cases, be sure to write "0" to the AIE bit.

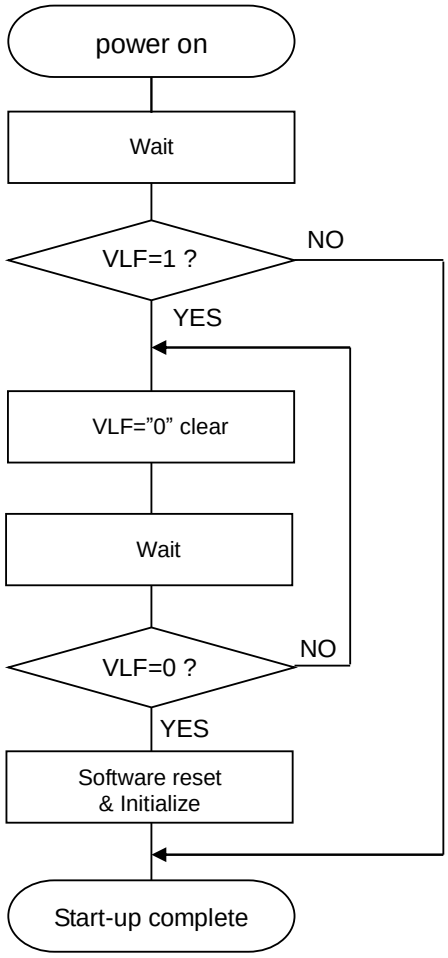
- Set the fixed-cycle Timer function.
  When the fixed-cycle timer function is not being used, the Timer Counter register can be used as a RAM register. In such cases, stop the fixed-cycle timer function by writing "0" to the TE and TIE bits.

- Set the Update interrupt function.

- Writes 00h. Disable output of SOUT.

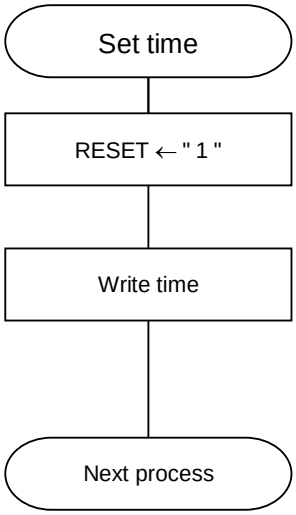
- Set the interval of a temperature compensation operation

2) Method of initialization after starting of internal oscillation (VLF stays “0”)



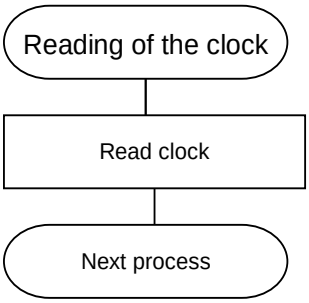
- Wait time of 30 ms is necessary at least
- Whether it is a return from the state of the backup is confirmed.
- When an internal oscillation starts, 0 writing of VLF is approved.
- Please set waiting time depending on load of a system optionally

3) The setting of the clock and calendar



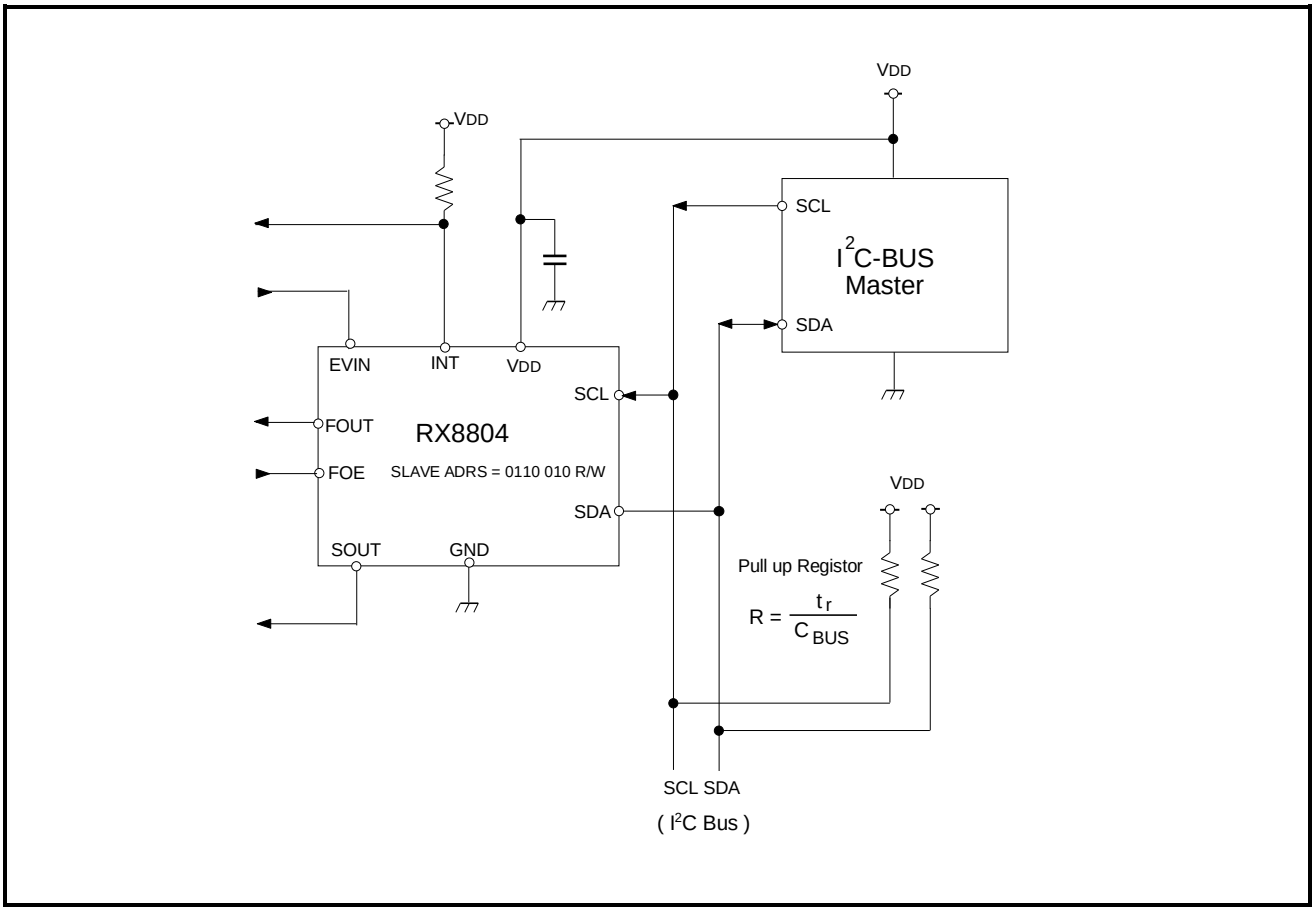
- Set RESET bit to “1” to prevent timer update in time setting.
- Write information of [year / month /date [day of the week] hour: minute: second] which is necessary to set (or reset). In case of initialization, please initialize all data.
- Please complete access within 0.95 seconds

4) The reading of the clock and calendar

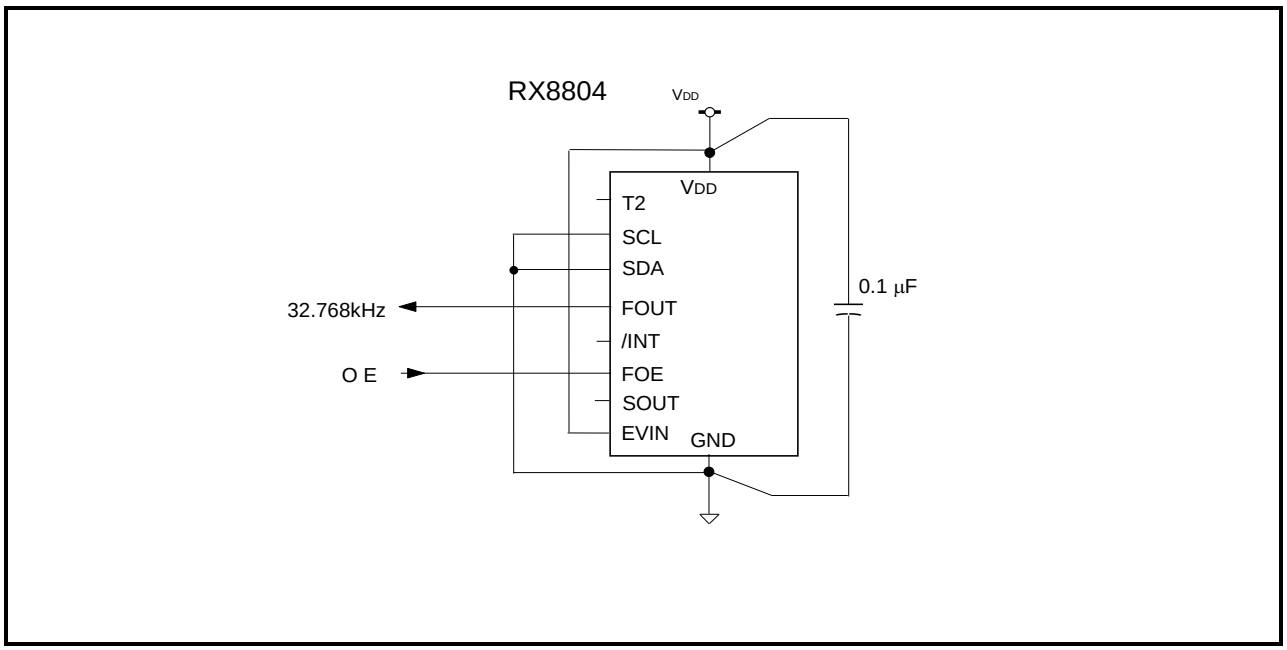


- Please complete access within 0.95 seconds
- At the time of a communication start, the Clock & Calendar data are fixed (hold the carry operation), and it is automatically revised at the time of the communication end.
- The access to a clock calendar recommends to have access to continuation by a auto increment function.

8.14. Connection with Typical Microcontroller



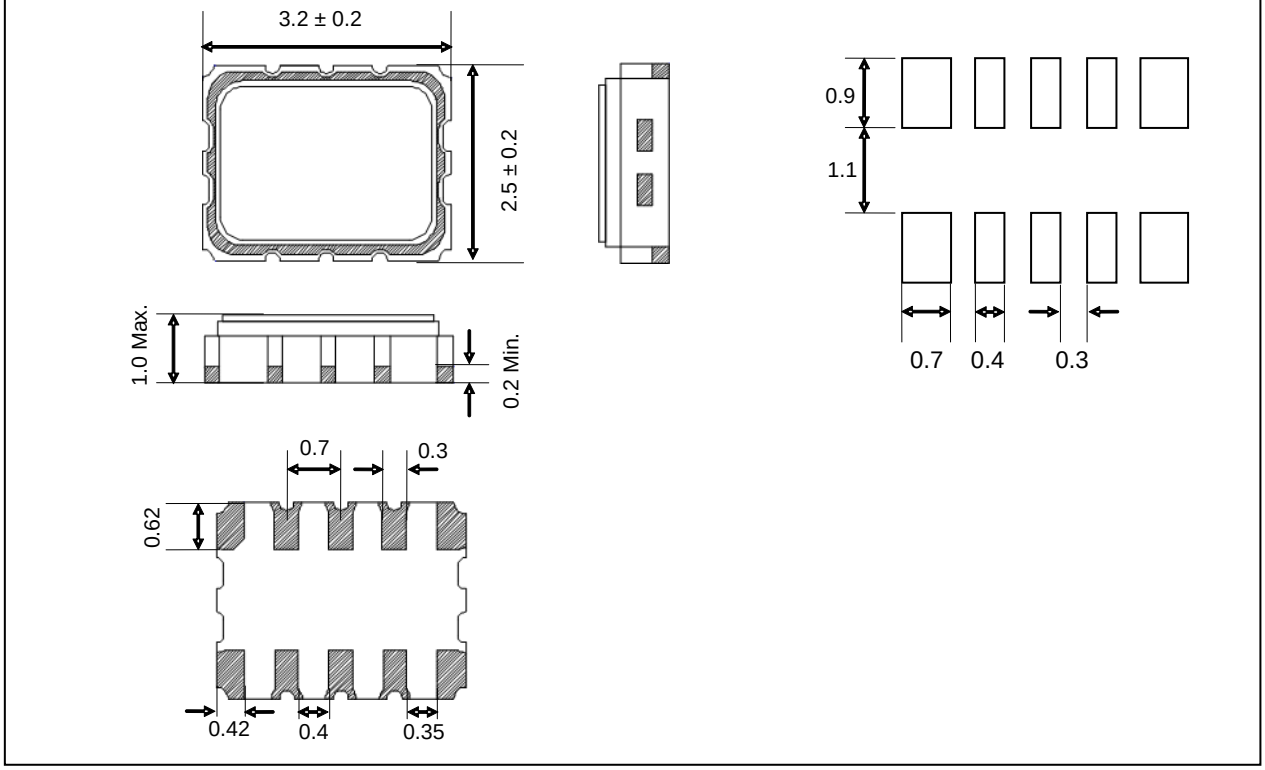
8.15. When used as a clock source (32 kHz-TCXO)



9. External Dimensions / Marking Layout

9.1. RX8804CE

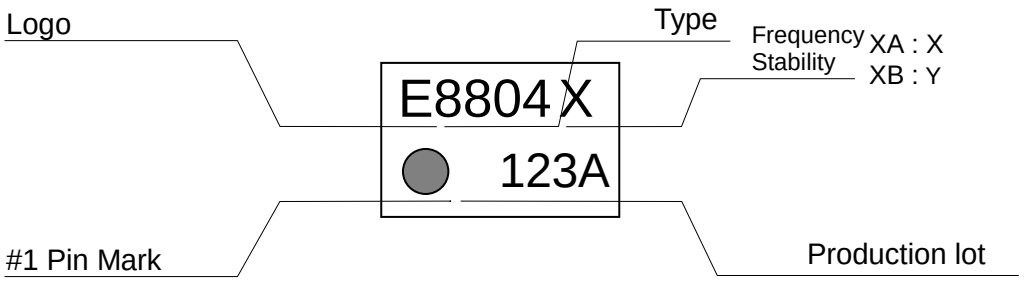
9.1.1. External dimensions



The small metal pads on the short side of the ceramic package are used to test the crystal.
When assembling the part, please be careful not to connect or short circuit this pads.
In addition, please avoid short circuit between these metal parts by dew condensation or particle adhesion.

9.1.2. Marking layout

RX8804CE



∗ Contents displayed indicate the general markings and display, but are not the standards for the fonts, sizes and positioning.

10. Application notes

1) Notes on handling

This module uses a C-MOS IC to realize low power consumption. Carefully note the following cautions when handling.

(1) Static electricity

While this module has built-in circuitry designed to protect it against electrostatic discharge, the chip could still be damaged by a large discharge of static electricity. Containers used for packing and transport should be constructed of conductive materials. In addition, only soldering irons, measurement circuits, and other such devices which do not leak high voltage should be used with this module, which should also be grounded when such devices are being used.

(2) Noise

If a signal with excessive external noise is applied to the power supply or input pins, the device may malfunction or "latch up." In order to ensure stable operation, connect a filter capacitor (preferably ceramic) of greater that 0.1 μF as close as possible to the power supply pins (between VDD and GNDs). Also, avoid placing any device that generates high level of electronic noise near this module.

* Do not connect signal lines to the shaded area in the figure shown in Fig. 1 and, if possible, embed this area in a GND land.

(3) Voltage levels of input pins

When the input pins are at the mid-level, this will cause increased current consumption and a reduced noise margin, and can impair the functioning of the device. Therefore, please apply the voltage level close to VDD or GND.

(4) Handling of unused pins

Since the input impedance of the input pins is extremely high, operating the device with these pins in the open circuit state can lead to unstable voltage level and malfunctions due to noise. Therefore, please apply the voltage level close to VDD or GND. But these pins must be the disposals that followed specification of pin exposition when it was specified N.C or open by pin exposition.

2) Notes on packaging

(1) Soldering heat resistance.

If the temperature within the package exceeds +260 °C, the characteristics of the crystal oscillator will be degraded and it may be damaged. The reflow conditions within our reflow profile is recommended. Therefore, always check the mounting temperature and time before mounting this device. Also, check again if the mounting conditions are later changed.

* See Fig. 2 profile for our evaluation of Soldering heat resistance for reference.

(2) Mounting equipment

While this module can be used with general-purpose mounting equipment, the internal crystal oscillator may be damaged in some circumstances, depending on the equipment and conditions. Therefore, be sure to check this. In addition, if the mounting conditions are later changed, the same check should be performed again.

(3) Ultrasonic cleaning

Depending on the usage conditions, there is a possibility that the crystal oscillator will be damaged by resonance during ultrasonic cleaning. Since the conditions under which ultrasonic cleaning is carried out (the type of cleaner, power level, time, state of the inside of the cleaning vessel, etc.) vary widely, this device is not warranted against damage during ultrasonic cleaning.

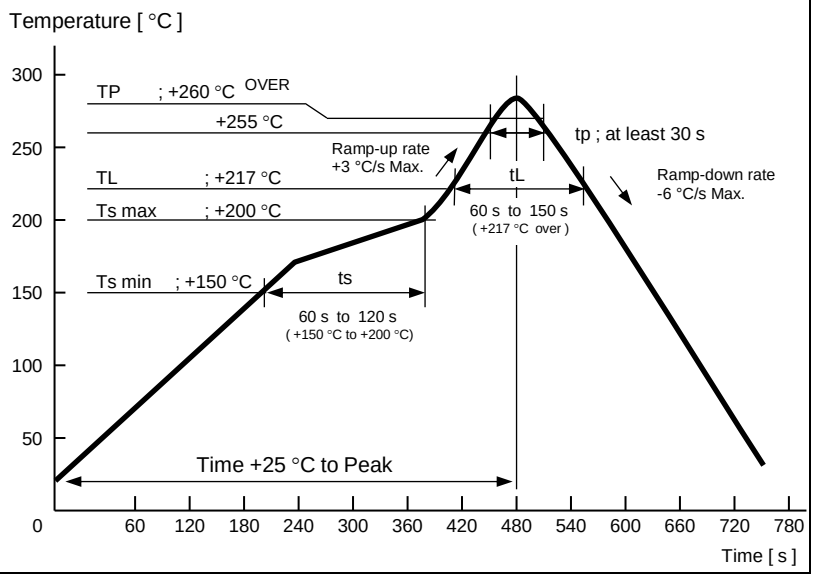
(4) Mounting orientation

This device can be damaged if it is mounted in the wrong orientation. Always confirm the orientation of the device before mounting.

(5) Leakage between pins

Leakage between pins may occur if the power is turned on while the device has condensation or dirt on it. Make sure the device is dry and clean before supplying power to it.

Fig. 1: Reference profile for our evaluation of Soldering heat resistance.



Application Manual

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