EVB-LAN9668 Evaluation Board User's Guide

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Preface

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For the most up-to-date information on development tools, see the MPLAB® IDE online help. Select the Help menu, and then Topics to open a list of available online help files.

INTRODUCTION

This chapter contains general information that will be useful to know before using the Microchip EVB-LAN9668 Evaluation Board. Items discussed in this chapter include:

- Document Layout
- Conventions Used in this Guide
- The Microchip Website
- Development Systems Customer Change Notification Service
- Customer Support
- Document Revision History

DOCUMENT LAYOUT

This document features the EVB-LAN9668 Evaluation Board. The manual layout is as follows:

- **Chapter 1. "Overview"** – This section provides an overview of the additional documentation needed and a brief description of the Evaluation Board feature list.
- **Chapter 2. "Management Software"** – This section gives a brief introduction of the turnkey managed software, which offers a Cisco-style Command Line Interface, as well as Web-based Graphical User Interface, to set up and control the switch.
- **Chapter 3. "Board Details"** – This section briefly walks through the different connector types and LEDs found on the Evaluation Board.
- **Chapter 4. "Hardware Details"** – This section describes the hardware implementation in details.
- **Chapter 5. "PCB Layout"** – This section shows the different PCB layers, especially the routing to the DDR RAM.
- **Chapter 6. "Initial Board Bring-Up Procedure"** – This section lists the order of milestones to make a complete bring-up of the Evaluation Board.

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CONVENTIONS USED IN THIS GUIDE

This manual uses the following documentation conventions:

DOCUMENTATION CONVENTIONS

Description	Represents	Examples
Arial font:		
Italic characters	Referenced books	*MPLAB® IDE User's Guide*
	Emphasized text	...is the *only* compiler...
Initial caps	A window	the Output window
	A dialog	the Settings dialog
	A menu selection	select Enable Programmer
Quotes	A field name in a window or dialog	"Save project before build"
Underlined, italic text with right angle bracket	A menu path	*File>Save*
Bold characters	A dialog button	Click **OK**
	A tab	Click the **Power** tab
N'Rnnnn	A number in verilog format, where N is the total number of digits, R is the radix and n is a digit.	4'b0010, 2'hF1
Text in angle brackets < >	A key on the keyboard	Press <Enter>, <F1>
Courier New font:		
Plain Courier New	Sample source code	`#define START`
	Filenames	`autoexec.bat`
	File paths	`c:\mcc18\h`
	Keywords	`_asm, _endasm, static`
	Command-line options	`-Opa+, -Opa-`
	Bit values	`0, 1`
	Constants	`0xFF, 'A'`
Italic Courier New	A variable argument	*`file.o`*`, where `*`file`*` can be any valid filename`
Square brackets [ ]	Optional arguments	`mcc18 [options] file [options]`
Curly brackets and pipe character: { | }	Choice of mutually exclusive arguments; an OR selection	`errorlevel {0|1}`
Ellipses...	Replaces repeated text	`var_name [, var_name...]`
	Represents code supplied by user	`void main (void) { ... }`

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- **Emulators** – The latest information on Microchip in-circuit emulators.This includes the MPLAB® REAL ICE™ and MPLAB ICE 2000 in-circuit emulators.
- **In-Circuit Debuggers** – The latest information on the Microchip in-circuit debuggers. This includes MPLAB ICD 3 in-circuit debuggers and PICkit™ 3 debug express.
- **MPLAB IDE** – The latest information on Microchip MPLAB IDE, the Windows® Integrated Development Environment for development systems tools. This list is focused on the MPLAB IDE, MPLAB IDE Project Manager, MPLAB Editor and MPLAB SIM simulator, as well as general editing and debugging features.
- **Programmers** – The latest information on Microchip programmers. These include production programmers such as MPLAB REAL ICE in-circuit emulator, MPLAB ICD 3 in-circuit debugger and MPLAB PM3 device programmers. Also included are non-production development programmers such as PICSTART® Plus and PICkit™ 2 and 3.

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DOCUMENT REVISION HISTORY

Revisions	Section/Figure/Entry	Correction
DS50003349A (06-23-22)	Initial release	

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Chapter 1. Overview

1.1 INTRODUCTION

This hardware manual describes the design of the LAN9668 reference board, demonstrating the Maserati TSN Ethernet Switch architecture. The LAN9668 reference board is based on the EVB-LAN9668 (Part Number: EV18W53) Reference Design Schematic.

1.1.1 Audience

This document is primarily intended for hardware and software engineers who want to get an overview of designing products based on the LAN9668.

1.1.2 References

1.1.2.1 MICROCHIP DOCUMENTS

- *EVB-LAN9668B Reference Design Schematic*, 2021/12/09
- *LAN9668 Product Data Sheet* (www.microchip.com/DS00004031)
- *LAN8814 Product Data Sheet* (www.microchip.com/DS00003592)
- *LAN8814 Errata* (www.microchip.com/DS800001002)
- *ZL30771_772_773 Data Sheet*
- *ENT-AN1187 - Using the Serial GPIO/LED Controller*

1.1.2.2 IEEE STANDARDS

- IEEE802.1D, Media Access Control Bridges
- IEEE802.1Q, Virtual Bridged Local Area Networks
- IEEE802.3, CSMA/CD Access Method and Physical Layer Specification
- IEEE1588-2008, Precision Clock Synchronization Protocol

1.1.3 Terms and Abbreviations

- AMS: Automatic Media-Sense
- CLI: Command Line Interface
- EMI: Electromagnetic Interference, emissions
- JTAG: Joint Test Access Group, IEEE1149
- LVDS: Low Voltage Differential Signaling
- LVTTL: Low Voltage TTL
- PCS: Physical Coding Sublayer
- PHY: Physical layer device
- PTP: Precision Time Protocol, IEEE1588
- SI: Serial Interface, SPI
- SME: Small/Medium Enterprise
- SSM: Synchronization Status Message
- SyncE: Synchronous Ethernet, ITU-T G.8262/Y.1362

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1.2 FEATURES

1.2.1 Feature List

The EVB-LAN9668 evaluation board use case is a Managed TSN Switch, exposing the main interfaces and features of LAN9668.

- LAN9668 TSN Switch with internal 600 MHz ARM® Cortex® A7 CPU and external 1GB SDRAM
- 8x tri-speed (10/100/1000M) RJ45 front ports using LAN8814 QuadPHY via QSGMII
- On-board SyncE DPLL ZL30772 to generate all the required clocks
- micro USB 2.0 port for management and debugging through a firmware driven Command Line Interface (CLI)
- PCIe® 2.0 End Point interface through USB3 connector or SPI for external CPU control
- Four SMA connectors for SyncE and PTP applications
- Reset button, which can also be used for SW detection of long press — for resetting to defaults
- System status LED and per network port status LEDs for link and activity indication
- 2x20 pin Expansion header exposing various interfaces: UART, QSPI, I^2C, PTP, CAN, and IRQ
- Standard 12V DC power input Jack (5.5 mm/2.5 mm center pin) or 12-48V DC input terminal screw connector type

1.2.2 CPU System

1.2.2.1 EMBEDDED ARM® CORTEX® A7 CPU SYSTEM

By default, the LAN9668 switch core is managed by its embedded CPU system with on-board SDRAM and SPI boot from either NOR or e-MMC™ NAND Flash (or both).

- Embedded ARM Cortex A7 single core 32-bit processor operating at 600 MHz
- External memories include 1 GB DDR3L SDRAM, 2 MB NOR, and/or 4 GB e-MMC SPI boot Flash memory

The Flash devices are used as device stage boot loader in a Secure boot environment.

1.2.2.2 EXTERNAL CPU CONNECTOR

Optionally, an external host CPU system can be connected to and control the LAN9668 configured as a client device through an external CPU connector, using either:

- PCIe 2.0 End Point — cabled to an external host system using a non-standard USB3 connector
- SPI — serial register access through the switch SI client interface exposed in the Expansion header

1.2.3 Management and User I/O

The embedded CPU system includes that the switch can be locally managed either through a WebGUI or CLI:

- WebGUI/https through any Ethernet port connected to the switch core
- micro USB 2.0 (or Telnet session) for CLI using a standard terminal application, like PuTTY

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1.2.4 CuPHYs

The reference board uses two tri-speed QuadPHYs LAN8814, which have low EMI line drivers with integrated line-side termination resistors, support for HP Auto MDI-/MDI-X™, and operate over standard Category 5 cabling at 10/100/1000 Mbit/s and Category 3 cabling at 10 Mbit/s.

1.2.5 Timing and Synchronization

1.2.5.1 SYNCE

The reference board supports SyncE through an on-board Microchip ZL30772 (Redwood) SyncE controller. SyncE is managed as part of the general switch management software.

The DPLL generates two reference clocks to LAN9668. The clock source can be either a free-running oscillator or a clock recovered from one of the CuPHY ports. The two LAN8814 CuPHYs simply daisy-chain the selected recovered clocks (2x) to the ZL30772 input.

For SyncE, the DPLL prioritizes and selects the clock source under software control and attenuates jitter before presenting the resulting clocks to LAN9668 and the two LAN8814. There is also one input and one output SMA available for SyncE, supporting 10 MHz, 2.048 MHz, and 1.544 MHz input and output station clocks.

1.2.5.2 PTP/IEEE1588V2

Precision Time Protocol (PTP) interfacing is available through all network ports (with high accuracy timestamping in the LAN8814 CuPHYs) and through input and output of 1 PPS SMA connectors.

The LAN9668 can be configured as boundary clock, transparent clock, PTP master, or PTP slave. LAN9668 can support both one-step and two-step operations.

A free-running 114.285 MHz XO provides the base clock to the board DPLL. Optionally, a 25 MHz TCXO can be used to provide improved frequency stability.

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Chapter 2. Management Software

2.1 INTRODUCTION

The reference board can be managed remotely by using a browser-based graphical user interface (WebGUI) or locally through an USB serial port using a command line interface (CLI). The reference board is intended to run with one of the WebStaX turnkey programs VSC6816-VSC6819. (It is, however, also possible to use the small demo application found in the API (MESA).)

2.2 CLI FOR MANAGEMENT AND DEBUGGING

The board can be connected directly to a PC USB port using a basic USB 2.0 A-Male to micro-B cable to access the CLI.

When connected, the PC will detect the LAN9668 built-in USB controller. There is no need to set up baud rate, data bits, parity or flow control in the terminal program running on the PC, as it is standard USB to USB 2.0 connection. However, in case the terminal program needs this, the COM port can be set up to run 8 data bits, 1 stop bit, no parity, 115200 baud, and without flow control.

Login into the switch can be made by using the default username, *admin* (without quotes). The default password is blank (that is, field value is empty). Help screens are available through the "?" or "help" commands.

A general way to restore default settings and password is to make a loop between port 1 and 2 during power-on (or simply press and hold the **Reset** button) and wait for the Switch Application to complete its boot-up.

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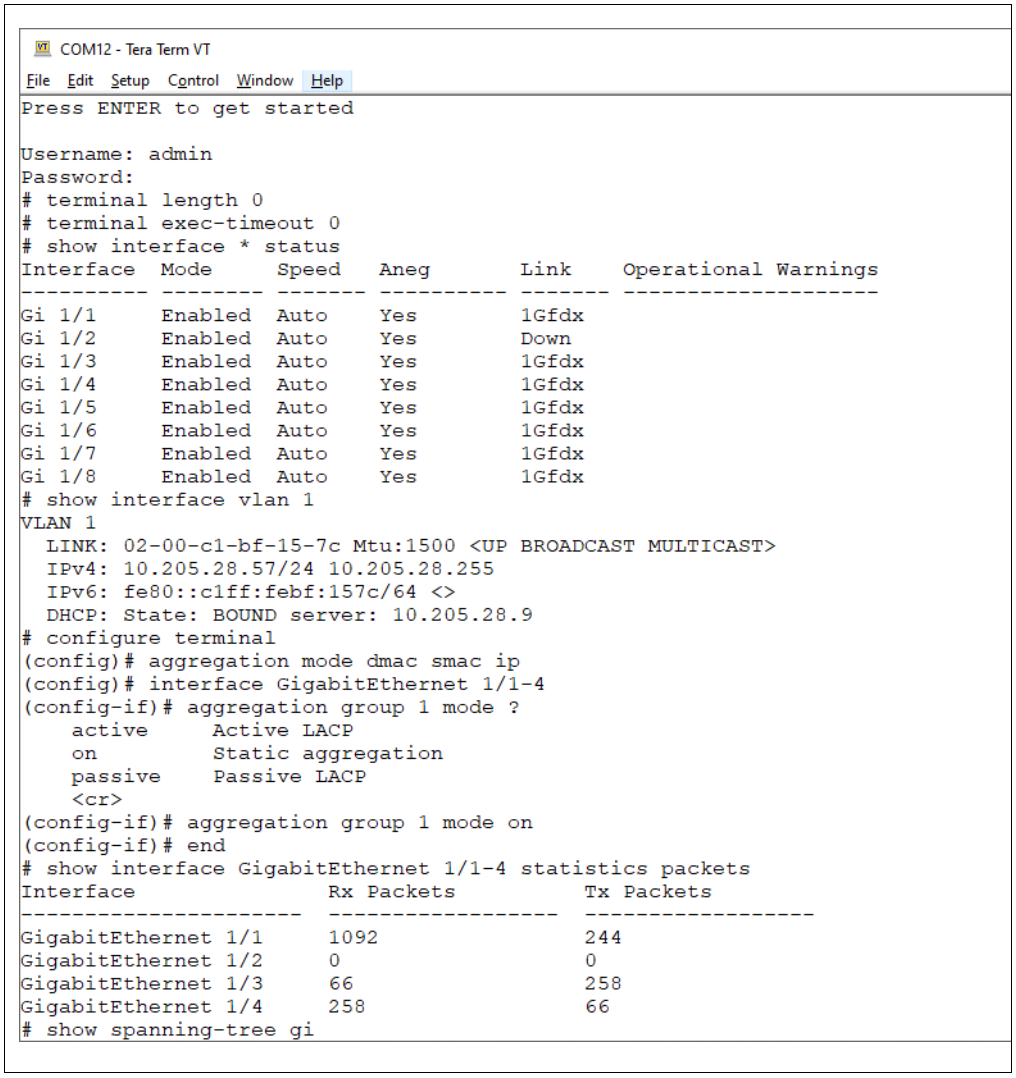
FIGURE 2-1: CLI SCREENSHOT EXAMPLE



One important use of the CLI is to determine the IP address of the switch, if DHCP is enabled. This is done through the `show interface vlan 1` command. The command displays the IP address that the WebGUI is available on.

An example of the CLI output when setting up Static Aggregation on four 1G ports is shown in Figure 2-1.

2.3 WEBGUI FOR MANAGEMENT

The WebStaX turnkey programs VSC6816-VSC6819 offers WebGUI access to manage the switch setup and to get current status.

The WebGUI is available from, for example, a PC connected to a network port. Ensure that the PC and switch are on the same subnet.

Start the PC's browser, point the browser at the switch's IP address (default static IP address is 192.0.2.1), and enter the login credentials when prompted. Default username is *admin*, and the default password is blank (that is, field value is empty). A graphical representation of the switch ports will appear.

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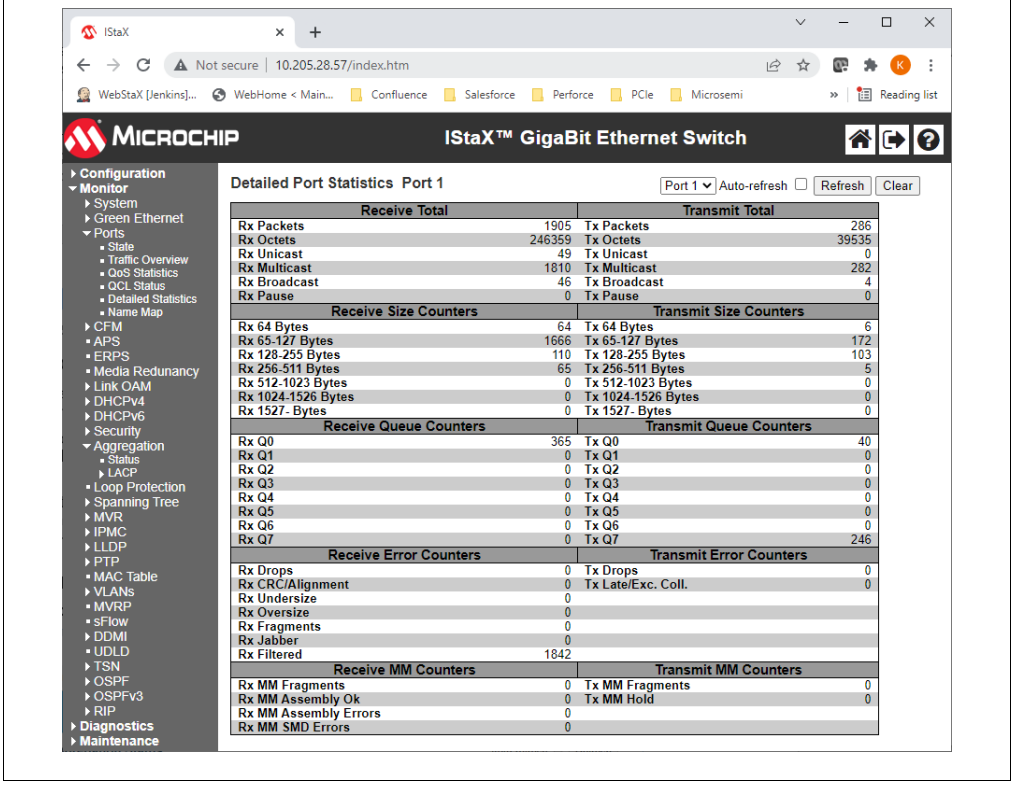
Setup is done by selecting the configuration menu at the top left and selecting an appropriate submenu. Likewise, the status can be displayed through the Monitor menu. New versions of the Switch Application can be uploaded through the Maintenance menu. Help screens are available through the "**?**" button at the top right.

Figure 2-2 shows the Port 1 RMON statistics.

FIGURE 2-2: WEBGUI SCREENSHOT EXAMPLE



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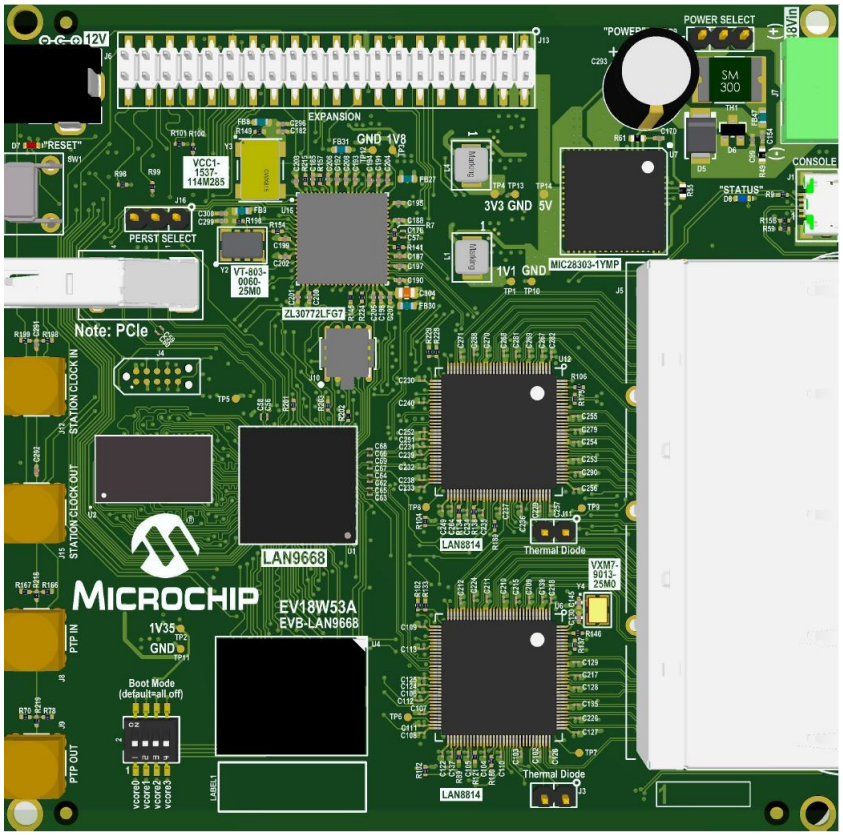
Chapter 3. Board Details

3.1 EVB-LAN9668 REFERENCE BOARD

3.1.1 Board Overview

Figure 3-1 shows the component placement on the EVB-LAN9668B PCB.

FIGURE 3-1: EVB-LAN9668 REFERENCE BOARD



3.1.2 Power DC Input and LED

The reference board is powered through either a standard 12VDC/1.5A PSU or through 12V-48VDC PSU. Pin strapping is used (J14) to select between the two power sources going to an on-board 5V, 3.0A power module. The power module then supplies different local DC/DC converters.

A single green LED (D9) indicates power-on using the 3.3V supply.

3.1.3 Reset Button and LED

A reset button is available on the reference board. When pressed, it drives the input of the voltage supervisor low, and thus creating a hard reset to the board. A red LED (D7) is used for indication.

If the reset button is held, reset is released. The state of the reset button can be read by software once it is running again to determine long press and configuring the board back to the default setup.

3.1.4 System Status LED

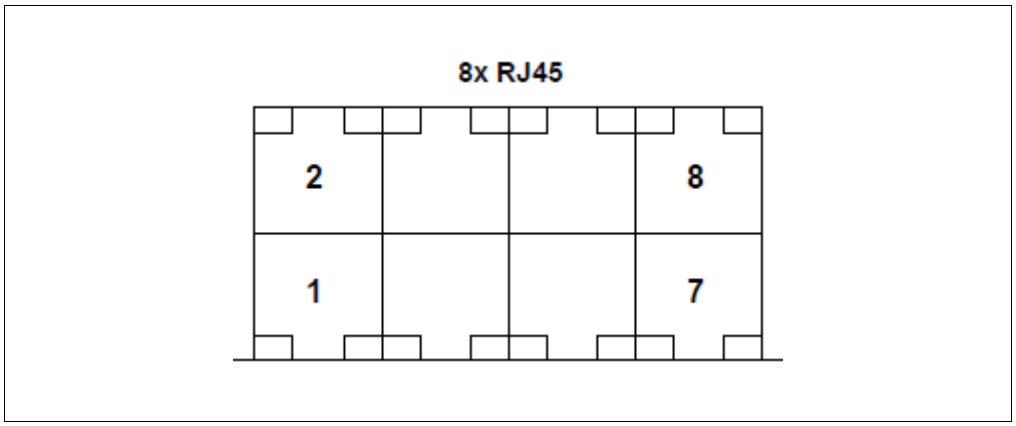
A blue LED (D8) shows the system status. It is controlled by software and is off during board reset.

3.1.5 Front Port Layout and LEDs

Software mapping is used to compensate for the physical board routing of PHY ports to the front ports together with their MIIM addresses.

Figure 3-2 shows the software mapping result to the front port layout on the EVB-LAN9668B PCB.

FIGURE 3-2: FRONT PORT LAYOUT ON EVB-LAN9668B



Two LEDs (green/yellow) are available on each RJ45 slot in the magnetic jack. The port status LEDs are automatically controlled by the LAN8814. The left LED signals 1G link/traffic (green solid/blinks) and the right LED signals 10/100M link/traffic (yellow solid/blinks).

3.1.6 Rear SMA Connectors

There are four SMA connectors, of which two are used as inputs and two as outputs.

One of the SMA input connectors is available for 1PPS into the LAN9668 PTP0 and optional to the board DPLL and Expansion header. The other SMA input (Station Clock Input) is for various frequencies (for example, 1.544 MHz, 2.048 MHz, and 10 MHz) into the board DPLL.

Note:	The SMA inputs are LVTTL and are 3V3-tolerant (not 5V-tolerant). The Station Clock Input is AC-coupled.

One of the SMA output connectors is used for 1PPS from the LAN9668. Optionally, it can be driven by the board DPLL. The other SMA output (Station Clock Output) is for various frequencies (for example, 1.544 MHz, 2.048 MHz, and 10 MHz) from the board DPLL. The 1PPS output uses LVTTL levels, and the Station Clock Output uses LVTTL levels and is AC-coupled.

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3.1.7 USB 2.0 Serial Port

The reference board can be controlled through a standard serial micro-USB 2.0 port using CLI commands from a terminal application, like PuTTY or TeraTerm.

3.1.8 PCIe® 2.0 End Point

The reference board offers a standard PCIe 2.0 End Point through a non-standard USB3 type of connection. It can be used together with the PCE2PCE-N07 adapter from the PCE164P-N07 kit.

3.1.9 ARM® CPU JTAG Connector

The reference board offers a standard 10-pin (0.05”) ARM CPU JTAG header to be used for boundary scan and In-Circuit Emulator (ICE). ICE can be used for debugging functions, such as downloading code and single-stepping through programs.

3.1.10 Expansion Header

The Expansion header is targeting Raspberry PI compatibility. It is a 2x10, 0.1” pin header. It can also be used for programming the on-board NOR Flash device, can give an external CPU control over the SPI client register access interface, and can expose various GPIO signals being in Alternate mode:

- UART: RXD, TXD (FLEXCOM 0, mode B)
- I2C: SCL, SDA (FLEXCOM 1, mode C)
- I2C: SCL, SDA (FLEXCOM 4, mode B)
- SPI: SCLK, MISO, MOSI + 5/6 Flex_Shared nCS (FLEXCOM 2, mode B)
- QSPI0: SPI.SCK, SPI.D1, SPI.D0 and SPI.nCS (NOR Flash/LAN9668)

The remaining Expansion header GPIO signals can function as normal GPIO pins when using default software settings. However, they can also be enabled with LAN9668-specific functionality, which is not found in the original Raspberry PI header.

- CAN0: RX, TX
- CAN1: RX, TX or Recovered clock 0/1
- MIIM (mode B — enabling MIIM in mode B will disable mode A to the LAN8814)
- IRQ or TRG
- PWM
- PTP

Likewise, the on-board Boot mode strapping, VCORE_CFG[3:0], can be overruled through the Expansion header.

3.1.11 Boot Modes and Reference Clock

The LAN9668 Boot mode can be selected through a 4-pin DIP switch. The system is default ‘0001’ set to boot from the serial NOR Flash device. Additionally, it is possible to strap the switch core and SerDes/PHY reference clock mode and frequency through strapping pins using resistors. The default setup is 25 MHz core clock and 125 MHz SerDes/PHY clock.

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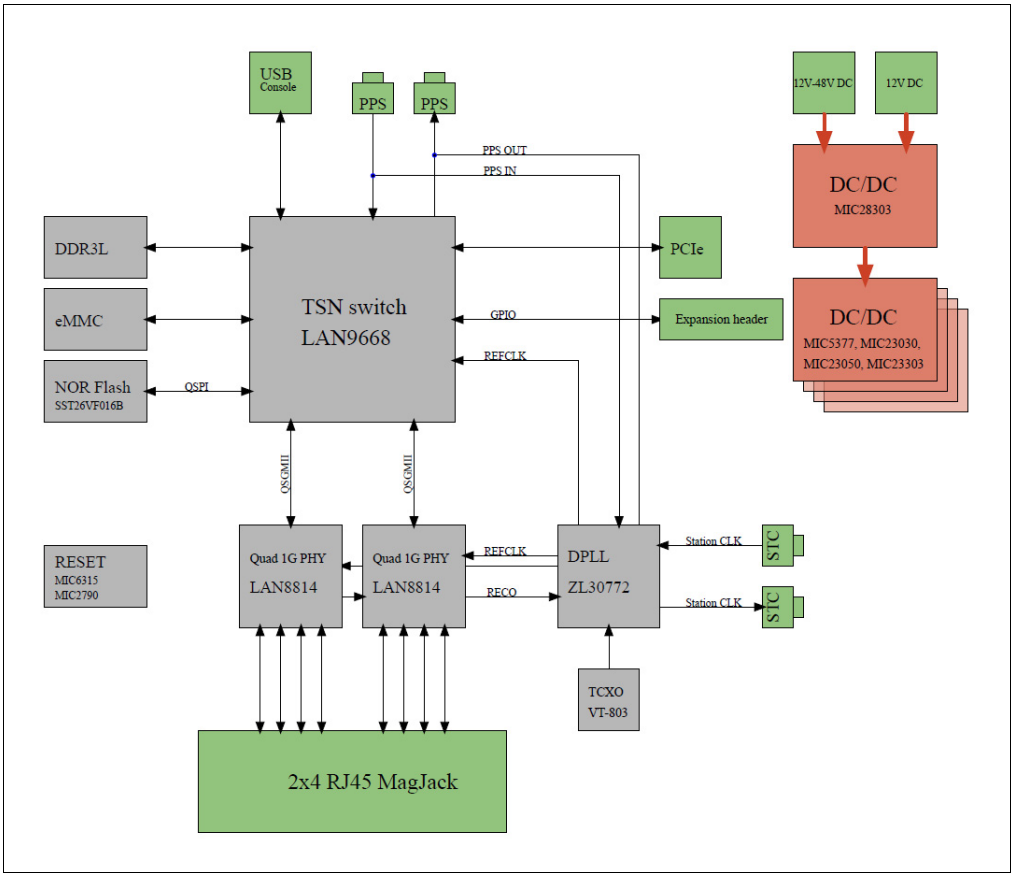
Chapter 4. Hardware Details

4.1 BLOCK DIAGRAMS

Figure 4-1 illustrates the block diagram of the reference board with its eight copper front ports and on-board DPLL.

FIGURE 4-1: EVB-LAN9668 BLOCK DIAGRAM



The design is based on the LAN9668 TSN switch, which includes a single core ARM Cortex A7 CPU that externally connects to 1 GB SDRAM, 4 GB e-MMC, and 2 MB NOR Flash memories — both can be used as second stage bootloader in a Secure Boot environment. The larger e-MMC memory is also used for bulk storage.

Optionally, an external CPU system can be connected and control the switch through a PCIe 2.0 End Point interfaces and/or through an SPI client interface found in the Expansion header.

A SyncE-capable DPLL ZL30772 generates all required reference clocks. The clock source can be either a free-running oscillator (XO) or a recovered clock from one of the CuPHY ports on the two LAN8814. The selected recovered clocks are daisy-chained through the two LAN8814 to the DPLL.

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The DPLL jitter attenuates the selected source clock and provides as reference clock to the LAN9668 switch and the two LAN8814 QuadPHYs. The generated clocks can be sourced individually to make two independent clock domains: one domain for SyncE and one domain for IEEE 1588.

There are four SMA connectors, which can be used for SyncE and IEEE 1588 applications.

Local management and software debugging can be made through the LAN9668 built-in USB 2.0 port.

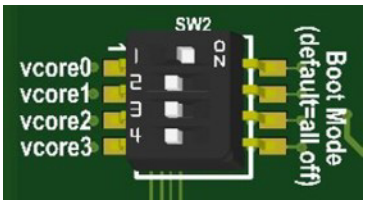
4.2 LAN9668 VCORE CPU SYSTEM

By default, the LAN9668 switch core is managed by its embedded CPU system with on-board SDRAM.

4.2.1 Boot Mode Strapping

LAN9668 uses strapping pins to select the initial boot mode. These pins are named VCORE_CFG[3:0] and located on GPIO[65, 42:40]. A four-pin DIP switch, SW2, is used to make the actual strapping.

FIGURE 4-2: 4-PIN DIP SWITCH, SW2



When SW2 is set to '0001', the embedded CPU uses the QSPI boot interface connected to a NOR Flash device, as second bootloader in a Secure Boot environment. Setting SW2 to '0000', the e-MMC is being used. Both settings require the Flash device to be pre-/programmed with a suitable bootloader.

The NOR Flash device can be programmed through the Expansion header using a Flash device programmer. Therefore, for production reasons, using the NOR Flash device is the board's default setup.

TABLE 4-1: BOOT MODES

SW2	VCORE_CFG[3:0] Description
0000	Boot from e-MMC. Boot traces on FLEXCOM3 mode B.
0001	Boot from QSPI0. Boot traces on FLEXCOM3 mode B. (Default)
0110	PCIe 2.0 End Point. Internal CPU is disabled.
1111	QSPI0/SI client and MIIM client interfaces are enabled. Internal CPU is disabled.

Using an external CPU, SW2 can be set to either '0110' to enable the PCIe 2.0 End Point controller found on the USB3 female connector, or to '1111' for register access through the SPI client or MIIM client interfaces, which are both found in the Expansion header.

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4.2.2 PLL Strapping

LAN9668 PLL strapping, PLL_STRP[1,0] located on GPIO[36,27], is set to have 25 MHz on switch core (and internal CuPHYs — not used in this design) and 125 MHz to the SerDes.

The same 125 MHz clock source is distributed to each of the LAN8814 QuadPHYs. Thus, the DPLL generated 125 MHz supports SyncE on the Ethernet ports and the 25 MHz supports IEEE 1588 timing domain in the switch core for its PTP engines.

TABLE 4-2: PLL STRAPPING MODES

Pulls	PLL_STRP[1:0] Description
00	SerDes: 25 MHz, Cu PHY: 25 MHz
01	SerDes: 125 MHz, Cu PHY: 125 MHz
10	SerDes: 125 MHz, Cu PHY: 25 MHz (default)
11	Reserved

Optionally, the board is prepared to use a local 25 MHz XTAL as reference input instead of the DPLL.

4.2.3 DDR3L SDRAM

The LAN9668 SDRAM interface is 16 bits wide and is targeted to operate at a clock rate of 600 MHz, requiring an SDRAM of speed grade 1200 MT/s or better.

The reference board is equipped with one 800 MHz 1 GB DDR3L SDRAM (x16) and has been tested up to 1325 MT/s. Lower densities can be substituted depending on the application. The minimum is 128 MB.

The reference design uses resistor dividers to generate the DDR_VRE, instead of using a dedicated DDR Power Manager device, like the MIC5166YML, as there is no need for driving DDR termination. DDR termination resistors can be avoided when keeping the maximum trace length below 35 mm.

4.2.4 SPI NOR Flash Device

The reference board is equipped with a 2 MB NOR QSPI boot Flash device (8-pin SOIC), which is solely intended to hold a second stage bootloader in a Secure Boot environment. The NOR Flash device can be removed if using e-MMC or SD Card for boot-up.

4.2.5 SPI NOR Flash Programming

The NOR Flash device can be programmed using an external Flash programmer connected to the pins in the Expansion header. This includes a reset signal through pin header J16.2, on which the programmer can keep the LAN9668 in reset, so it will not drive the SI_CLK and SI_DO outputs while programming the SPI Flash device. Alternatively, the LAN9668 can be set into SPI Client mode ‘1111’ using the SW2, DIP switch.

To connect the Universal Programmer from ASIX (Forte or Presto), see Table 4-3.

TABLE 4-3: PROGRAMMING SIGNALS

Expansion Header	Universal Programmer from ASIX
Pin 1 (VccSPI)	P3 (VDD) (Red)
Pin 35 (SI.D1)	P7 (DO/I) (White)
Pin 36 (SPI.nCS0)	P1 (P) (Yellow)

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TABLE 4-3: PROGRAMMING SIGNALS (CONTINUED)

Expansion Header	Universal Programmer from ASIX
Pin 38 (SI.D0)	P5 (DI/D) (White)
Pin 39 (GND)	P4 (GND) (Blue)
Pin 40 (SI.CLK)	P6 (C) (Green)

4.2.6 e-MMC™ Flash Device, Bulk Storage

The reference board is equipped with a 4 GB e-MMC for bulk storage.

Alternatively, it can be used as a second stage boot ROM instead of the NOR Flash device, and thus avoids having the NOR Flash device mounted. For production, it is then recommended to use a preprogrammed e-MMC device, or to have an additional test connector, like TC2050, placed between LAN9668 and the e-MMC for on-board programming. FLEXCOM 3 mode B can also be used for programming the e-MMC.

Note: This has not yet been validated as the current design uses FLEXCOM3 in mode A.

4.2.7 PHY Interrupts

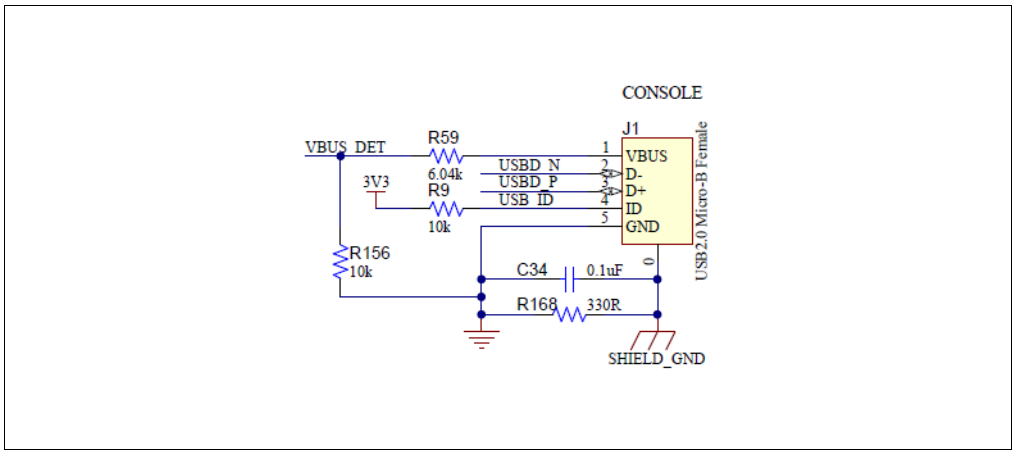
A dedicated PHY interrupt input signal, MIIM_INT#, is connected to the LAN9668 GPIO 24/IRQ_IN_5C. The MIIM_INT# is a shared (open collector) interrupt from the two LAN8814 QuadPHYs. Hence, when an interrupt occurs, software must poll the possible sources for the current interrupt status through their respective MIIM interface, because it is not possible to distinguish which PHY source has activated the shared interrupt signal.

4.2.8 Micro USB Serial Port

In the LAN9668, the USB device and host interface share the same internal UTMI transceiver, and the same data pins, USBD_P and USBD_N. The interface supports up to 480 MHz USB 2.0 high-speed transmission speed.

On the reference board, the USB port, J1, is configured in Device mode and is used as the console port.

FIGURE 4-3: USB DEVICE MODE CONNECTION



VBUS_DET is divided by a resistor network to reduce the voltage from 5.0V to 3.125V and connects to GPIO_8, which has the overlaid function of VBUS detection. When GPIO_8 detects the VBUS, an interrupt can be generated, thus software can enable the USB transceiver. The USB ID from the USB connector is connected to GPIO_9 to enable the reference board to change between being a USB device and being an initiator (host).

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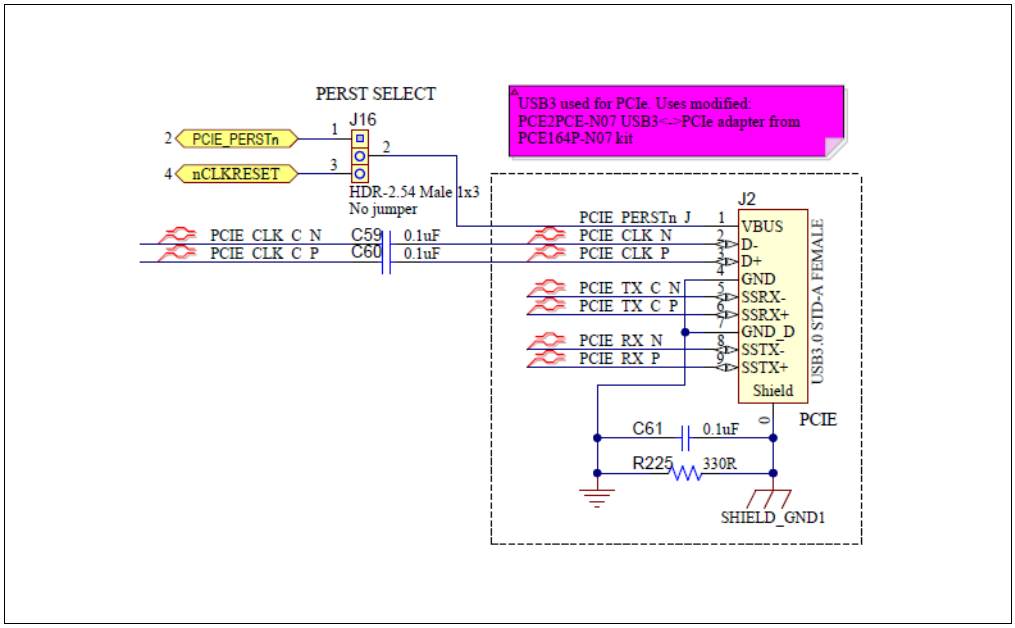
4.2.9 PCIe® 2.0 End Point

LAN9668 implements a single-lane PCIe Gen2 End Point controller, that can be hooked up to any PCIe-capable system. The PCIe client interface can be used by an external CPU to read or write switch registers.

The reference board offers the PCIe 2.0 client through a non-standard USB3 type of connection. It can be used together with the PCE2PCE-N07 adapter from the PCE164P-N07 kit.

FIGURE 4-4: PCIE® CLIENT INTERFACE USING USB3 FEMALE CONNECTOR



Note:	The switch TX direction has AC coupling. It is expected that the PCIe host has similar setup. Likewise, the received PCIe_CLK is AC-coupled with on-board biasing to VPTX/2.

Optionally, an external reset signal can be routed to LAN9668 — either as PERST# signal or nCLKRESET by using J16. Using the later may not comply to the PCIe reset timing.

Note:	The LAN9668 has some frame-DMA capabilities, but the injection and extraction rates highly depend on the frame size as the major overhead is in setting up the DMA. The rule of thumb is that injection from the CPU queues is twice as fast as extraction to the CPU queues when using the internal CPU system. A powerful external CPU system can however easily make it opposite and much faster.

4.2.10 ARM® CPU JTAG Connector

The reference board offers a standard 10-pin (0.05”) ARM CPU JTAG header, J10, to be used for boundary scan and In-Circuit Emulator (ICE). ICE can be used for debugging functions, such as downloading code and single-stepping through programs.

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FIGURE 4-5: JTAG INTERFACE

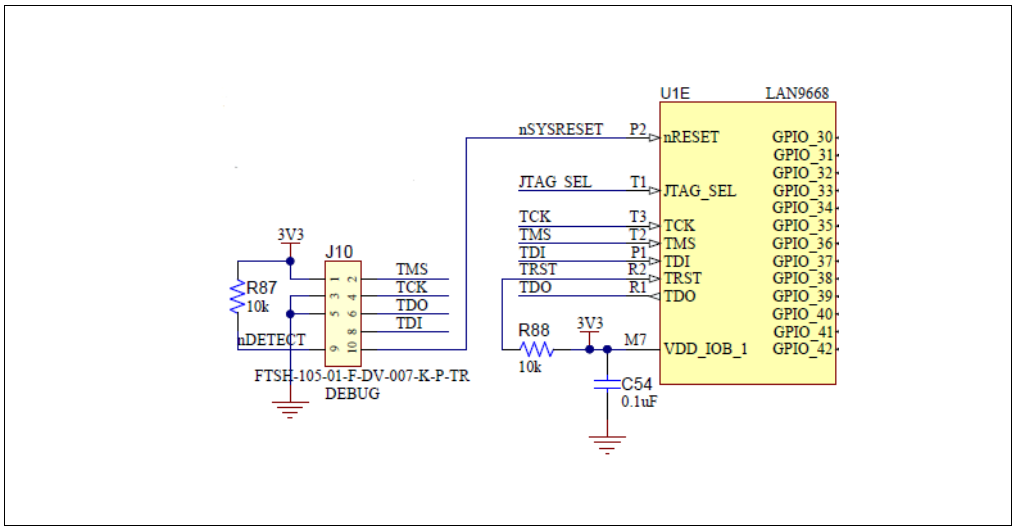

TABLE 4-4: JTAG HEADER, J10

Pin	JTAG	In/Out	Remarks
1	3.3V	—	Power
2	TMS	VIS (PU)	Test mode select input
3	GND	—	Ground
4	TCK	VIS (PU)	Test clock input
5	GND	—	Ground
6	TDO	VO (PU)	Test data output
7	—	—	NC
8	TDI	VIS (PU)	Test data input
9	nDETECT	VIS (PU)	Voltage sense
10	nSYSRESET	VIS (PU)	HW reset

Note: The JTAG signals are not 5V-tolerant. JTAG signal levels are determined by the VDD_IOB power supply pin, and can be 1.8V, 2.5V, or 3.3V.

The JTAG_SEL input pin controls the mapping of the chip-level JTAG to select between the CPU subsystem TAP controller or the Test TAP controller. The default resistor setting is pull-up for CPU.

4.2.11 Expansion Header

The Expansion header, J13, is targeting Raspberry Pi compatibility. It is a 2x10, 0.1" pin header. It can also be used for programming the on-board NOR Flash device, give an external CPU control over the SPI client register access interface, and expose various LAN9668 GPIO signals in Alternate mode.

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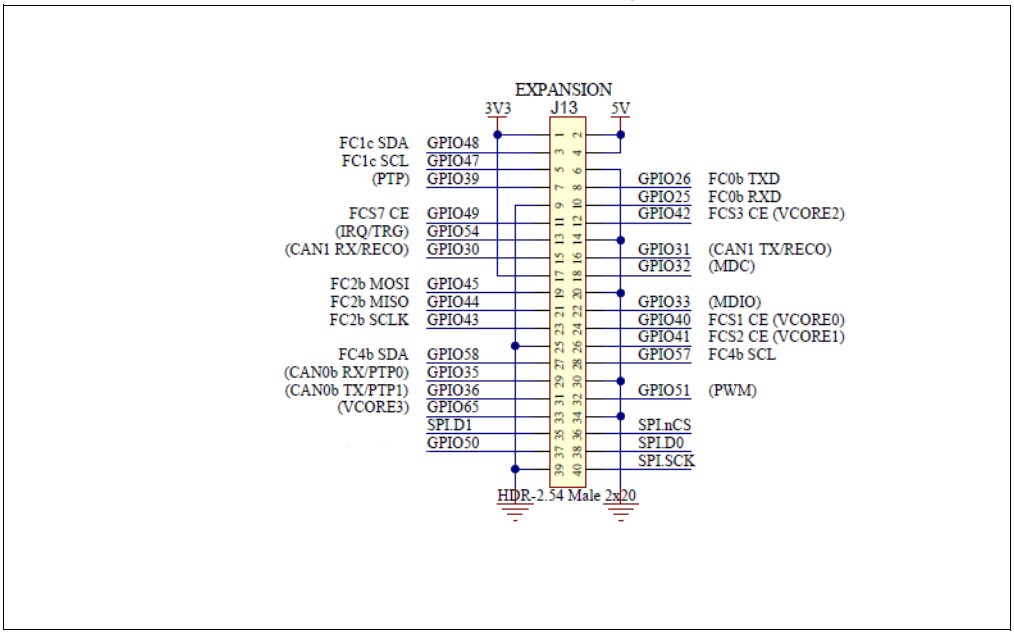
FIGURE 4-6: EXPANSION HEADER LAYOUT, J13



Note: An add-on board using the Expansion header *must* have its own Power-On-Reset (POR), and ensure that the VCORE_CFG strap settings are not overridden unintentionally (GPIO 36, 40, 41, 42, and 65).

The I/O functionality, which is not compatible with Raspberry Pi is marked yellow in Table 4-5. For these, the GPIO signals function as normal GPIO pins when using default software settings.

TABLE 4-5: EXPANSION HEADER — PIN DESCRIPTION

Pin	Signal	Description
1	3V3	VccSPI
2	5V	—
3	GPIO 48	I^2C SDA (FLEXCOM 1C)
4	5V	—
5	GPIO 47	I^2C SCL (FLEXCOM 1C)
6	GND	—
7	GPIO 39	(PTP0 IN)
8	GPIO 26	UART TX (FLEXCOM 0B)
9	GND	—
10	GPIO 25	UART RX (FLEXCOM 0B)
11	GPIO 49	CE (FLEXCOM shared 7)
12	GPIO 42	CE (FLEXCOM shared 3) (VCORE_CFG2 strap.)
13	GPIO 54	(IRQ or TRG)
14	GND	—
15	GPIO 30	(CAN1 RX or Recovered clock 0)
16	GPIO 31	(CAN1 TX or Recovered clock 1)
17	3V3	—
18	GPIO 32	(MDC_B)

TABLE 4-5: EXPANSION HEADER — PIN DESCRIPTION (CONTINUED)

Pin	Signal	Description
19	GPIO 45	MOSI (FLEXCOM 2B)
20	GND	—
21	GPIO 44	MISO (FLEXCOM 2B)
22	GPIO 33	(MDIO_B) When enabling mode B, mode A should be disabled.
23	GPIO 43	SCLK (FLEXCOM 2B)
24	GPIO 40	CE (FLEXCOM shared 1) (VCORE_CFG0 strap)
25	GND	—
26	GPIO 41	CE (FLEXCOM shared 2) (VCORE_CFG1 strap)
27	GPIO 58	I^2C SDA (FLEXCOM 4B)
28	GPIO 57	I^2C SCL (FLEXCOM 4B)
29	GPIO 35	(CAN0b RX/PTP0 IN)
30	GND	—
31	GPIO 36	(CAN0b TX/PTP1 OUT) (PLL_STRP1 strap)
32	GPIO 51	(PWM_B)
33	GPIO 65	(VCORE_CFG3 strap)
34	GND	—
35	SPI.D1	SPI.D1
36	SPI.nCS0	SPI.nCS0
37	GPIO 50	Must be an input. Chip select to LAN9668 and/or NOR Flash
38	SPI.D0	SPI.D0
39	GND	—
40	SPI.CLK	SPI.CLK

4.2.12 GPIO Overview Usage

Each GPIO pin in LAN9668 can be assigned to one of up to eight functions. Table 4-6 shows which GPIOs and functionality have been used in the EVB-LAN9668 design. Yellow indicates strapping pins.

TABLE 4-6: GPIO USAGE

GPIO	Index/Strap	Overlaid	Interface	Exp. Header	Remark
GPIO8	B	ALT4	VBUS_DET	—	USB VBUS detect
GPIO9	—	—	—	—	USB_ID
GPIO17	A	ALT1	FLEX3_SCK	—	DPLL SPI.
GPIO18	A	ALT1	FLEX3_RXD	—	DPLL SPI.
GPIO19	A	ALT1	FLEX3_TXD	—	DPLL SPI.
GPIO24	C	ALT5	IRQ_IN	—	PHY MIIM_INTn
GPIO25	B	ALT1	FLEX0_RXD	x	UART RX
GPIO26	B	ALT1	FLEX0_TXD	x	UART TX
GPIO27	PLL_STRP0	—	—	—	—
GPIO28	A	ALT1	MDC	—	PHY MIIM
GPIO29	A	ALT1	MDIO	—	PHY MIIM
GPIO30	—	ALT2	CANRX1	x	(CANRX1/RC0)
GPIO31	—	ALT2	CANTX1	x	(CANTX1/RC1)
GPIO32	B	ALT6	MDC	x	(MDC)

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TABLE 4-6: GPIO USAGE (CONTINUED)

GPIO	Index/Strap	Overlaid	Interface	Exp. Header	Remark
GPIO33	B	ALT6	MDIO	x	(MDIO)
GPIO35	B	ALT4	PTPSYNC_0	x	(PTP0 IN/CAN-RX0)
GPIO36	PLL_STRP1	ALT4	PTPSYNC_1	x	(PTP1 OUT/CANTX0)
GPIO37	JTAG_STRP0	—	PTPSYNC_2	—	—
GPIO38	JTAG_STRP1	—	PTPSYNC_3	—	PTP3 OUT SMA
GPIO39	—	—	PTPSYNC_4	x	(PTP0 IN DPLL)
GPIO40	VCORE_CFG0	ALT1	FLEX-_SHARED_1	x	CE
GPIO41	VCORE_CFG1	ALT1	FLEX-_SHARED_2	x	CE
GPIO42	VCORE_CFG2	ALT1	FLEX-_SHARED_3	x	CE
GPIO43	B	ALT1	FLEX2_SCK	x	SCLK
GPIO44	B	ALT1	FLEX2_RXD	x	MISO
GPIO45	B	ALT1	FLEX2_TXD	x	MOSI
GPIO46	—	ALT5	FLEX-_SHARED_4	—	DPLL SPI_CK.CSn
GPIO47	C	ALT1	FLEX1_RXD	x	I2C SCL
GPIO48	C	ALT1	FLEX1_TXD	x	I2C SDA
GPIO49	—	ALT1	FLEX-_SHARED_7	x	CE
GPIO50	—	ALT1	FLEX-_SHARED_16	x	(GPIO50/nCS)
GPIO51	B	ALT5	PWM	x	(PWM)
GPIO52	B	ALT6	IRQ_IN1	—	DPLL nCK_Valid
GPIO53	—	—	—	—	nPHYRESET
GPIO54	—	ALT2-6	IRQ3	x	(IRQ or TRG)
GPIO55	—	—	—	—	nBUTTON
GPIO56	—	—	—	—	nMR
GPIO57	B	ALT1	FLEX4_RXD	x	I2C SCL
GPIO58	B	ALT1	FLEX4_TXD	x	I2C SDA
GPIO60	—	—	—	—	COMA
GPIO61	C	ALT2	PCIe PERST#	—	PCIE_PERSTn
GPIO62	—	—	—	—	CPU_ACT
GPIO65	VCORE_CFG3	—	—	x	—

TABLE 4-7: GPIO USAGE - EMMC INTERFACE

GPIO	Index	Overlaid	Interface	Remark
GPIO67	—	ALT1	SD/MMC_CMD	—
GPIO68	—	ALT1	SD/MMC_CK	—
GPIO69	—	ALT1	SD/MMC_D0	—
GPIO70	—	ALT1	SD/MMC_D1	—
GPIO71	—	ALT1	SD/MMC_D2	—
GPIO72	—	ALT1	SD/MMC_D3	—
GPIO73	—	ALT1	SD/MMC_D4	—
GPIO74	—	ALT1	SD/MMC_D5	—
GPIO75	—	ALT1	SD/MMC_D6	—
GPIO76	—	ALT1	SD/MMC_D7	—
GPIO77	—	ALT1	SD/MMC_RSTN	—

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4.3 ETHERNET PORTS

LAN9668 has eight logical Ethernet ports. Two SerDes interfaces running QSGMII are used to connect each LAN8814 QuadPHY. The QSGMII signals are AC-coupled to ensure Common-mode voltage compatibility.

4.3.1 Port Mapping

Software mapping between internal ports and front ports compensates for the physical board routing of PHY ports in the 2x4 ICM together with their MII-Management addresses, so ports appear like in Figure 3-2 from a user-management perspective.

```
Mapping:
```

Port	Chip Port	MIIM Bus	MIIM Addr
0	2	0	9
1	3	0	10
2	0	0	7
3	1	0	8
4	6	0	17
5	7	0	18
6	4	0	15
7	5	0	16

4.3.2 PHY Copper Interface

The LAN8814 QuadPHY integrates all passive components required to connect the PHYs' line-side interface to an external 1:1 transformer and Common-mode choke. This reduces the number of components in a design and greatly simplifies the layout of this interface.

The PHYs support auto-negotiation and downshift, and can automatically detect the speed of a link if auto-negotiation is disabled, and hereby provides the appropriate connection (parallel detect).

The PHYs include Automatic Crossover Detection functionality for all speeds (HP Auto MDI/MDI- X™ function) and the ability to detect and correct polarity errors on all MDI pairs. These functions are normally enabled but can be disabled.

Instead of separate magnetic modules and RJ45 connectors, the reference board uses RJ45 connectors with integrated magnetics. This reduces the number of components on the board and the actual board area.

All PHYs support the IEEE standard range of 1m to 100m twisted pair cable; however:

- 1000BASE-T mode requires Category 5 enhanced cable in accordance to the cabling specifications defined by IEEE802.3-2005.
- 100BASE-TX mode requires Category 5 cable and 10BASE-T requires Category 3 cable as specified in ISO/IEC 11801.

4.3.3 ICM - Integrated Magnetics

The reference board uses a 2x4 RJ45 ICM with integrated LEDs.

Note: The magnetics have huge influence on the EMI performance.

4.3.4 MII-Management

The LAN9668 serves the LAN8814 QuadPHYs over a MIIM bus interface available as alternate function on its GPIO pins. The MIIM is daisy-chained to the two LAN8814 QuadPHYs covering front ports 1-8 and terminated at the end using pull-up on MDIO0 and split end-termination on MDC0. The drive strength for MDC0 is 3.

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4.3.5 Thermal Diode (Optional)

The reference board can optionally provide a probe point using a 2-pin header to access the LAN8814 QuadPHY built-in thermal diode.

4.3.6 Port LEDs and COMA Signal

Port LEDs are automatically controlled by the LAN8814 QuadPHY. There are two LEDs per port. One LED is for 1G traffic and the other is for 10/100M traffic. A solid ON LED means linkup, while blinking means traffic.

The PHY COMA input signal is used to suppress all errors, alarms, link-up/-down notifications until the PHY or the whole system has been properly initialized. The COMA signal is also being used to 'synchronize' the two LAN8814 LED blink rates.

The COMA signal can be controlled by software from either the LAN9668 or the two LAN8814.

4.3.7 Optional Clock Scheme

The EVB-LAN9668 reference design provides an optional clocking scheme, where SyncE and IEEE 1588 timestamping are not an application requirement, and thus avoid populating the ZL30772 DPLL.

The clocking scheme leverages on the LAN8814 ability to provide an output clock from its internal PLL circuitry. This means:

25 MHz crystal → LAN8814#1 → CK25OUT → LAN8814#2 → CK25OUT → LAN9668

Using only one clock source and no clock buffer saves costs, and all devices still run on the same frequency, which prevents inter-packet gap shrinks in the TX direction and only one rate adaptation in the RX direction incoming traffic.

The default board setup is to use the ZL30772 DPLL provided reference clocks.

Note:	Currently an errata prevents this clock scheme to work, as both LAN9668 and LAN8814 require a 125 MHz reference clock when using QSGMII.

4.4 TIMING AND SYNCHRONIZATION

The reference board includes a factory preprogrammed DPLL, ZL30772-LFG7Q091 for frequency multiplier and clock buffer. It provides 25 MHz LVCMOS to the LAN9668 and 125 MHz LVDS-level reference clocks to LAN9668 and LAN8814. The ZL30772 is using a 114.285 MHz oscillator. For increased frequency stability, it can also operate in split-XO mode (see the *ZL30772 Data Sheet*) together with a 25 MHz TCXO.

The ZL30772 is controlled through the SPI interface using FLEXCOM 3 mode A. Optionally, it can be setup for I^2C.

4.4.1 SyncE

For SyncE, the ZL30772 DPLL prioritizes and selects the clock source under software control and attenuates jitter before presenting the resulting clocks. The clock source can be either the free-running oscillators or a clock recovered from one of the CuPHY ports.

4.4.2 Recovered Clock Multiplexing

Each LAN8814 QuadPHY can do clock multiplexing and daisy-chaining of two selected recovered clocks to the ZL30772 DPLL inputs, as depicted in Figure 4-7.

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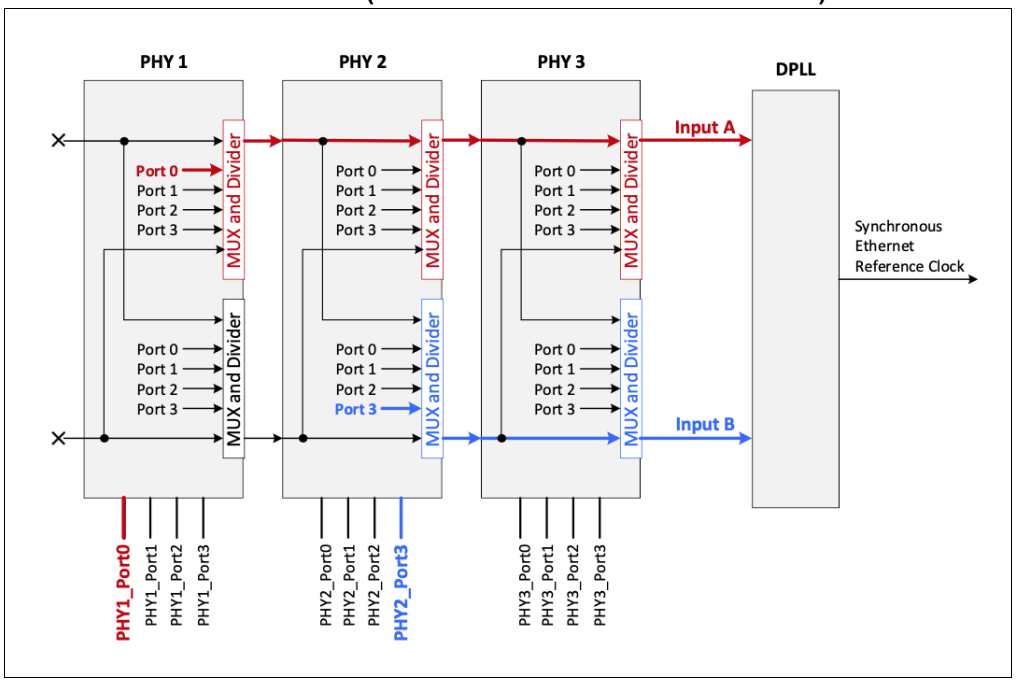
FIGURE 4-7: DAISY-CHAINING RECOVERED OUTPUT CLOCKS USING LAN8814 (EXAMPLE SHOWING THREE PHYS)



4.4.3 PTP/IEEE1588v2

The free-running oscillators provide the base clock to the board DPLL. The XO can be exchanged with an OCXO for applications with higher requirements, and thus offering Stratum-3 holdover.

PTP interfacing is available through all network ports with timestamping in the LAN8814 QuadPHY and through input and output of 1PPS SMA connectors.

The LAN9668 GPIO39 controls loading and adjusting the PHY 1588 local time counter LTC. It is used to synchronize both LAN8814 1588 LTCs with the system 1588 TOD. It controls the initial setting (load) and incremental update (adjust) of the internal 1588 LTC.

The LAN9668 can be configured as boundary clock, transparent clock, PTP master, or PTP slave.

4.4.4 ZL30772 Frequency Plan

The frequency plan is selected during reset. By pin strapping, the AC[1:0] selects plan 01 as the default. Table 4-8 shows the frequency plans for the factory preprogrammed ZL30772LFG7Q091

TABLE 4-8: ZL30772 FREQUENCY PLAN 01

Signal	Frequency	Description
MCLKIN/OSCI	114.285 MHz	From XO
REF0P	125 MHz	RCVRD_CKO1 from LAN8814
REF0N	125 MHz	RCVRD_CKO2 from LAN8814
REF1	—	—
REF2P	10 MHz	Station Clock input from SMA/J12, AC-coupled
REF2N	1PPS/GPIO35	PTP input SMA/J8
REF3P	1PPS/GPIO36	PTP input feedback from DPLL

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TABLE 4-8: ZL30772 FREQUENCY PLAN 01 (CONTINUED)

Signal	Frequency	Description
REF3N	1PPS/GPIO38	PTP output SMA/J9 feedback from LAN9668 or DPLL
REF4P	25 MHz	Feedback from DPLL
REF4N	25.000 MHz	HCMOS from TCXO
GPO0	25 MHz/GPIO36	LVCMOS, ePPS PTP1 LDSV (disabled)
GPO1	25 MHz/GPIO39	LVCMOS, ePPS PTP0 LDSV (disabled)
HPOUT0P	25.00 MHz	LVCMOS, local feedback to REF4P
HPOUT0N	1PPS/GPIO38	LVCMOS Local feedback to REF3N, alternate PTP_OUT to SMA (disabled – JTAG strapping pin, must be disabled during reset)
HPOUT1	—	(disabled)
HPOUT2	—	(disabled)
HPOUT3P	10 MHz/2.048 MHz	LVCMOS, Station Clock out to SMA/J15
HPOUT3N	—	(disabled)
HPOUT4	125 MHz	LVDS, differential clock to LAN9668
HPOUT5P	25.00 MHz	LVCMOS, single clock to LAN9668
HPOUT5N	—	(disabled)
HPOUT6	125 MHz	LVDS, differential clock to LAN8814
HPOUT7	125 MHz	LVDS, differential clock to LAN8814

The EVB-LAN9668 schematic provides an optional Programming header for reprogramming the frequency plan.

4.4.5 SMA Connectors

The reference board has two input and two output SMA connectors as detailed in Table 4-9.

PTP IN is available for 1PPS signal into one of the LAN9668 PTP engines and is optional to the board DPLL. PTP OUT is controlled by another LAN9668 PTP engine. This can optionally be controlled by the DPLL.

STATION CLOCK IN is used for various input frequencies (1.544 MHz, 2.048 MHz, or 10 MHz) into the DPLL. STATION CLOCK OUT is solely controlled by the board DPLL to provide 10 MHz, 2.048 MHz, or 1.544 MHz for SyncE. By default, the input and output frequencies are 10 MHz. If other frequencies are desired, this can be controlled by the running the SyncE application.

TABLE 4-9: SMA CONNECTORS

SMA	Connector	Description
PTP IN	J8	PTP, 1PPS input to LAN9668 Can be biased
PTP OUT	J9	PTP, 1PPS output from LAN9668
STATION CLK IN	J12	Sync-E, clock input to DPLL, AC-coupled Can be biased
STATION CLK OUT	J15	Sync-E, 10 MHz (default) clock output from DPLL, AC-coupled

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Note: SMA inputs are LVTTL and 3V3-tolerant, and not 5V-tolerant. All SMAs have TVS protection diodes.

4.5 RESET AND RESET BUTTON

The reference board Reset scheme consists of two reset signals: nCLKRESET and nSYSRESET.

The nCLKRESET is generated by a voltage supervisor, MIC6315, when the 3.3V supply falls below the threshold or the reset button (SW1) is being pressed. The other supply voltages are not monitored, but reset is first released, when all power supplies are stable — signaled through POK_1V1. The nCLKRESET is used as a master reset to the on-board SyncE DPLL.

The nSYSRESET is the board reset and is controlled by the nCLKRESET. The nSYSRESET is simply delayed 600 ms from nCLKRESET by using MIC2790L to ensure that the 25 MHz reference clock from the SyncE DPLL to LAN9668 core is stable.

Optionally, the EVB-LAN9668 schematic design allows a 25 MHz crystal to be used as core clock for fast boot (due to lower reset delay).

The reset button is available at the back of the reference board. When pressed, it drives the input of the voltage supervisor low, and thus creating a hard board reset. It functions as a one-shot, so pressing it causes a reset, and it can afterward be sampled by firmware to determine if it is still pressed during boot (for example, causing a "reset to factory defaults").

A red LED, D7, is controlled through the nSYSRESET signal and is used to indicate the reset state.

4.6 POWER SUPPLY

The reference board is powered through either a standard 12VDC/1.5A PSU or through 12V-48VDC PSU. Three-pin jumper is used (J14) to select between the two power sources going to an on-board 5sV, 3.0A power module. The power module then supplies different local DC/DC converters.

4.6.1 DC/DC Converters

Table 4-10 shows how the MIC28303 power module supplies different local DC/DC converters.

TABLE 4-10: DC/DC CONVERTERS

DC In	DC Out	Description
12-48V@2A	5V@3A	MIC28303-1 power module 50V, 3A adjustable switching regulator
5V@3A	1.1V@2.9A	MIC23303-YML/ADJ 3A switching regulator LAN9668 (1.2A), 2xLAN8814 (1.7A)
	1.35V@0.4A	MIC23030 400 mA switching regulator DDR (175 mA), RAM (225 mA)
	1.8V@0.6A	MIC23050-GYML 600 mA switching regulator ZL30772 (540 mA)
	3.3V@2.1A	MIC23303-YML/ADJ 3A switching regulator LAN9668 (0.2A), 2xLAN8814 (1.2A), ZL30772 (0.4A), misc (0.3A)

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TABLE 4-10: DC/DC CONVERTERS (CONTINUED)

DC In	DC Out	Description
3.3V@0.5A	2.5V@0.1A	MIC5377-YC5-TR linear regulator DDR PLL (40 mA)

Total, including conversion loss: 14.5W 5V@2.9A

4.6.2 Power Supply Sequencing

The overall strategy for the switch power supply sequencing is to prevent a higher-powered supply feeding lower-level powered grids through the internal protection diode network. The general power sequence is:

1V1 → 1V35/3V3

ZL30772 dictates a sequence where the I/O supply must be brought up before the 1.8V core supply.

3V3 → 1V8/2V5

A single green LED (D9) indicates Power-ON using the 3.3V supply.

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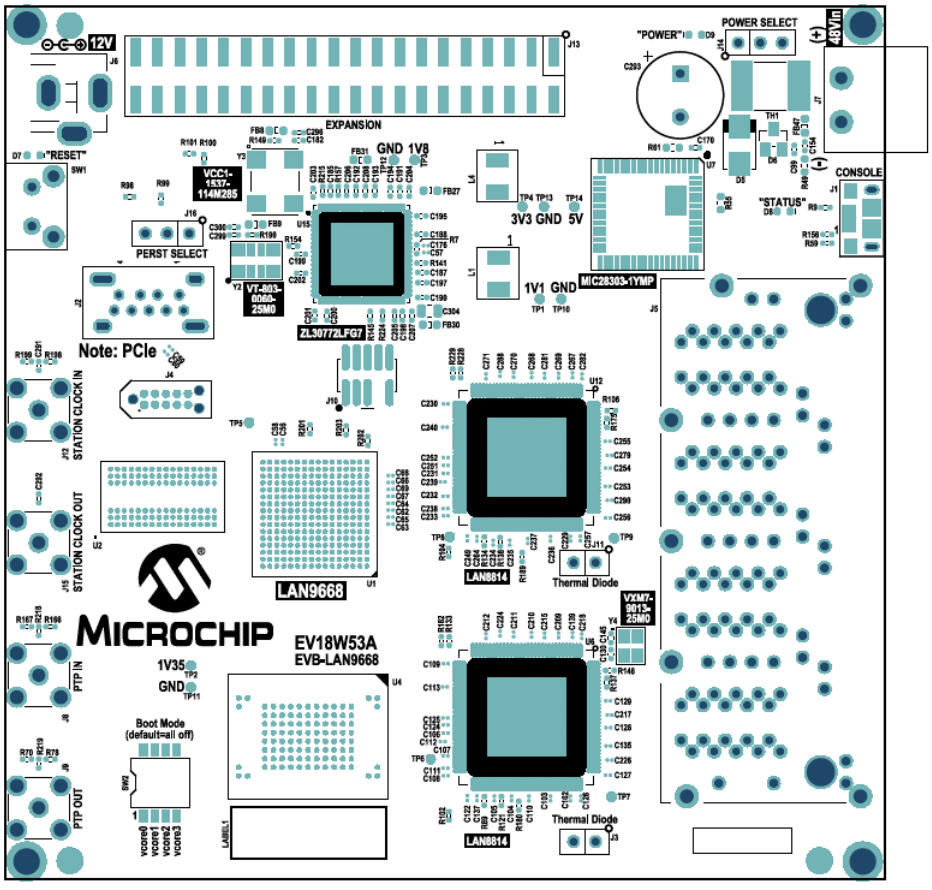
Chapter 5. PCB Layout

5.1 INTRODUCTION

Figure 5-1 shows the board outline. The board dimensions and holes follow previous designs, like the VSC5635EV Metal chassis — a holder for DIN rail mounting, for brackets and chassis holes for reuse reasons across reference board designs.

FIGURE 5-1: EVB-LAN9668 REFERENCE BOARD OUTLINE



LAN9668 and LAN8814 devices package pinout is specifically optimized for low-cost PCB designs. As a result, the EVB-LAN9668 reference design requires only six PCB layers.

Most signals are routed on the top and bottom layers, 1 and 6. However, it is necessary to route some signals on layer 3 and layer 4.

There are two solid ground planes, layer 2 and 5, which are also used to remove heat from components, and it must (also for this reason) be ensured that there is good connection between the outer layer ground fills and that ground planes are established.

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5.2 PCB LAYERS

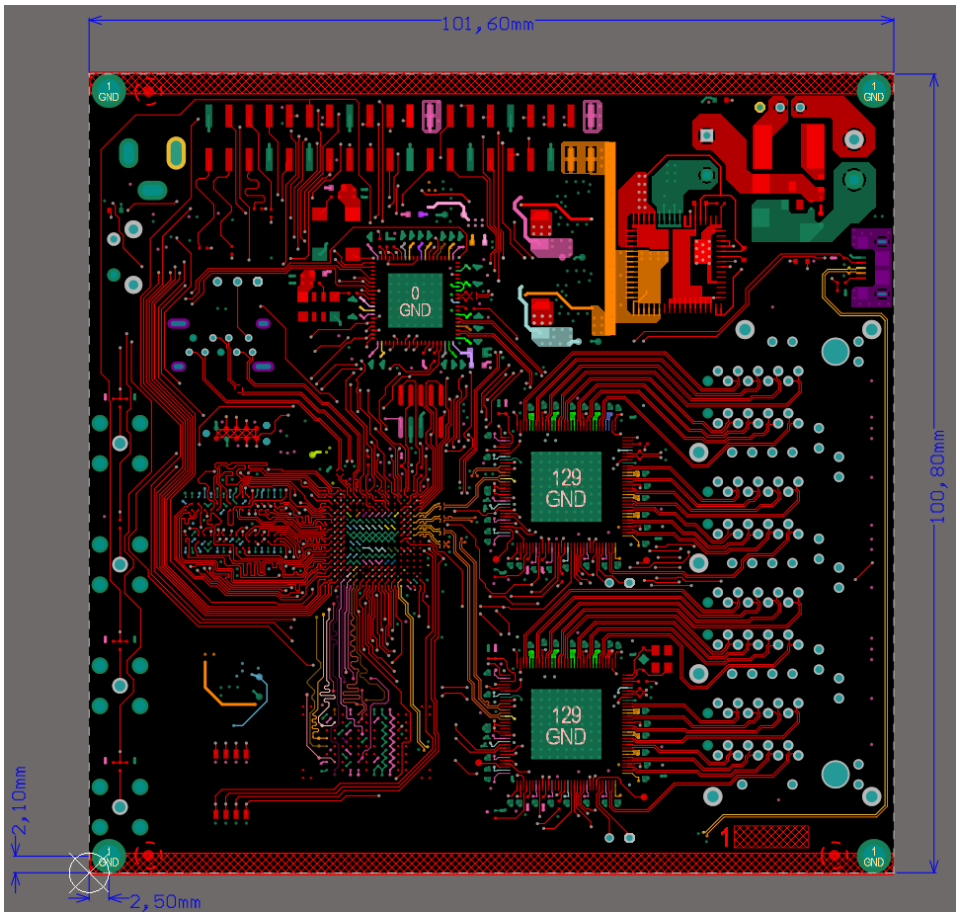
TABLE 5-1: PCB LAYERS AND DESCRIPTIONS

Layer	Description
1 (TOP)	LAN9668 signal traces for DDR3L and SerDes TX paths
2 (GND)	Solid ground plane. LAN8814 ground shield.
3 (POWER)	Power planes for LAN9668 and LAN8814, 1V1
4 (POWER)	Power planes, 1V8, 2V5, 1.35V DDR3L power planes.
5 (GND)	Solid ground plane
6 (BOTTOM)	LAN9668 signal traces for DDR3L and SerDes RX paths

The ground shield serves as a "quiet" ground for PHY copper media signals. It couples capacitively to the ground plane, providing a low-impedance return path for high-frequency noise.

5.2.1 Layer 1 — Top

FIGURE 5-2: LAYER 1



Most are signal traces for DDR3L and SerDes macros, SFP slots.

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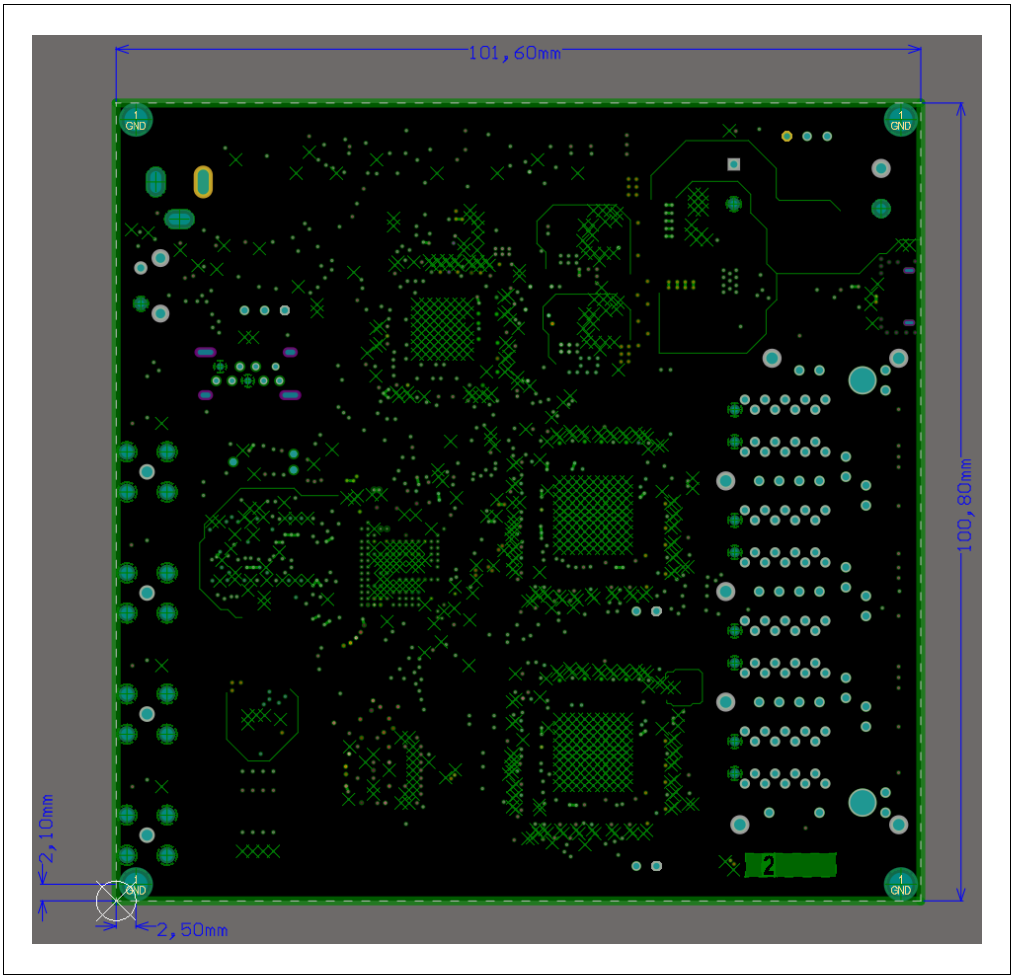
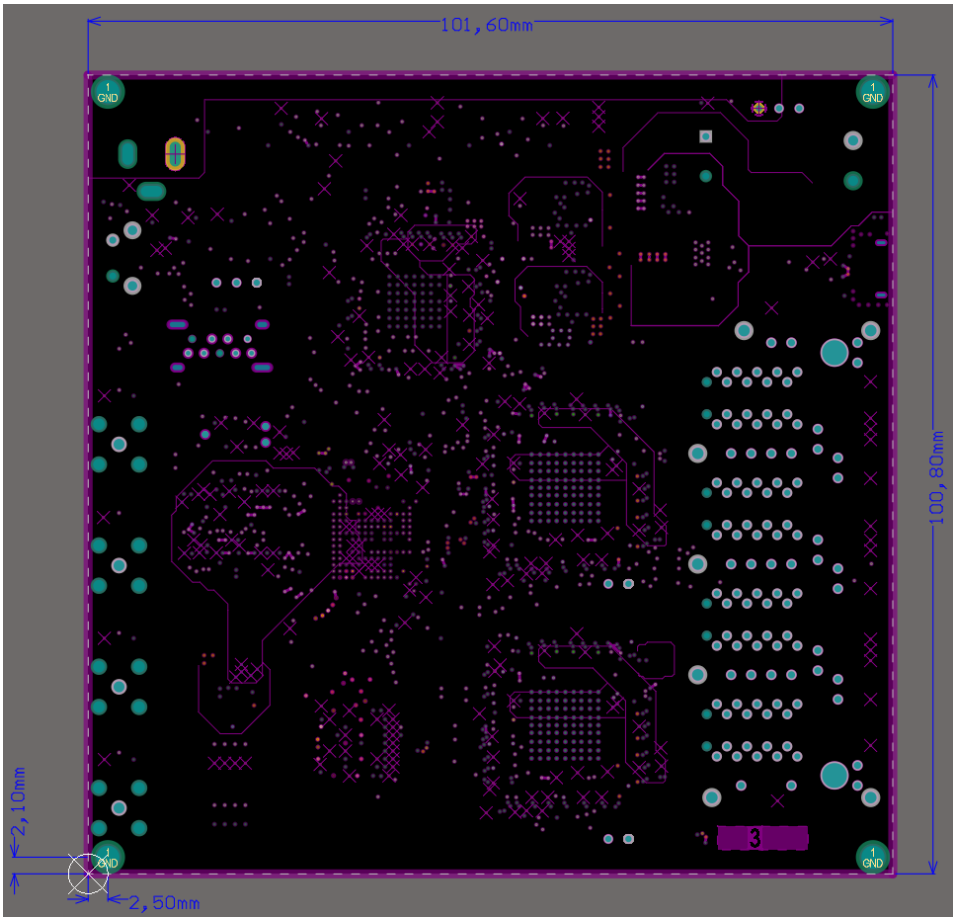
5.2.2 Layer 2 — Ground Plane

FIGURE 5-3: LAYER 2



5.2.3 Layer 3 — Power

FIGURE 5-4: LAYER 3



Layer 3 is used to distribute the different power supplies: 1.35V to DDR3L, 1.1V to the 2x LAN8814, and 1.8V to the DPLL.

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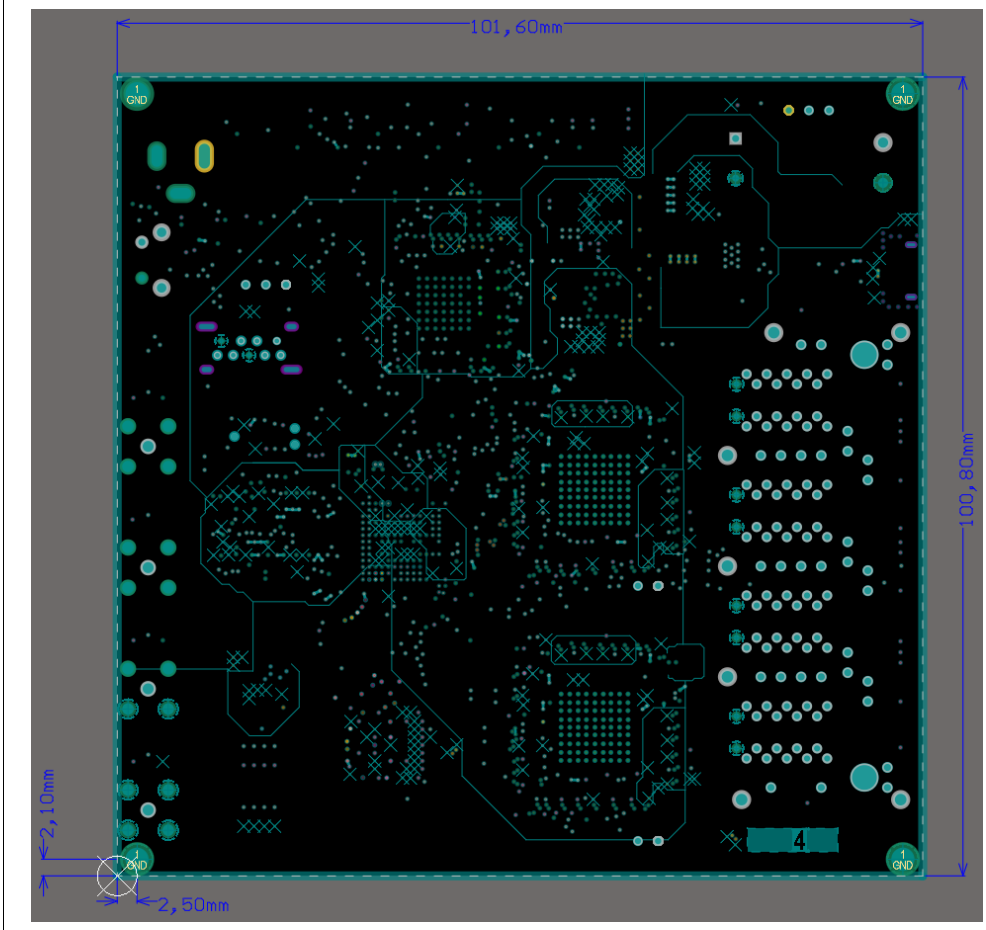
5.2.4 Layer 4 — Power

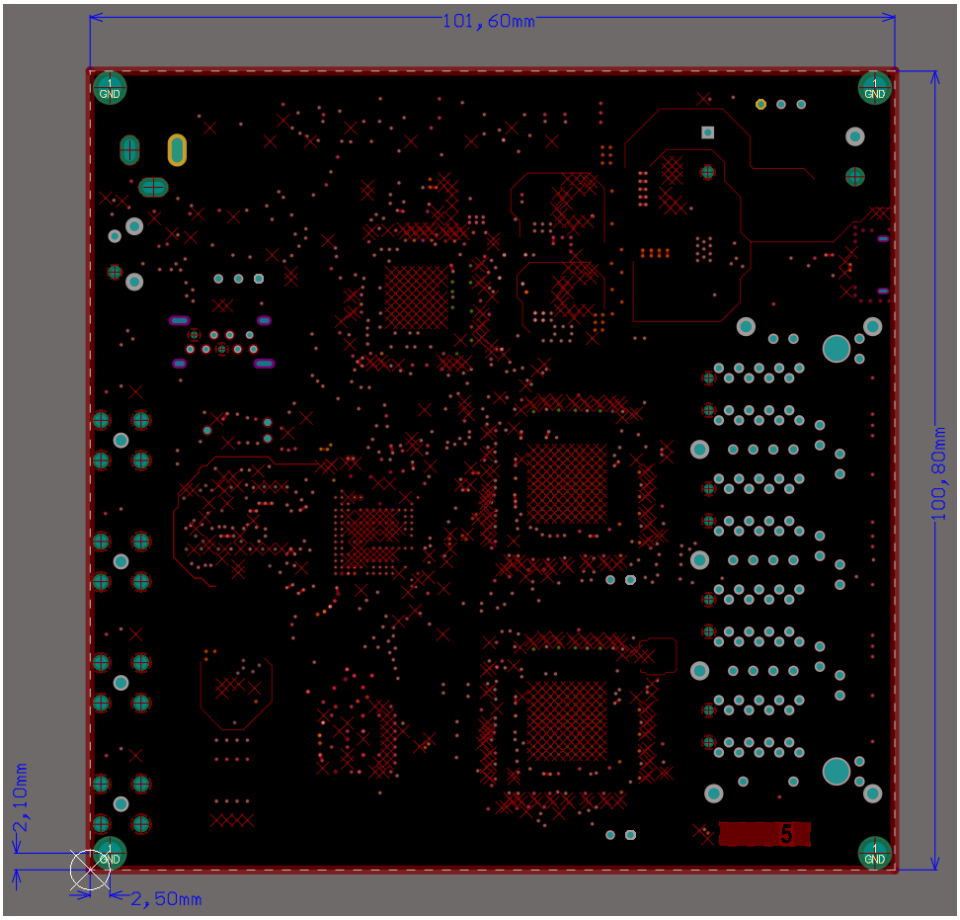
FIGURE 5-5: LAYER 4



Layer 4 is mainly used to distribute the 3.3V and 5V power planes. The 1.1V power to the LAN9668 is made ‘short and wide’ as possible. The DDR3L DDR_VT power plane is also found here.

5.2.5 Layer 5 — GND

FIGURE 5-6: LAYER 5



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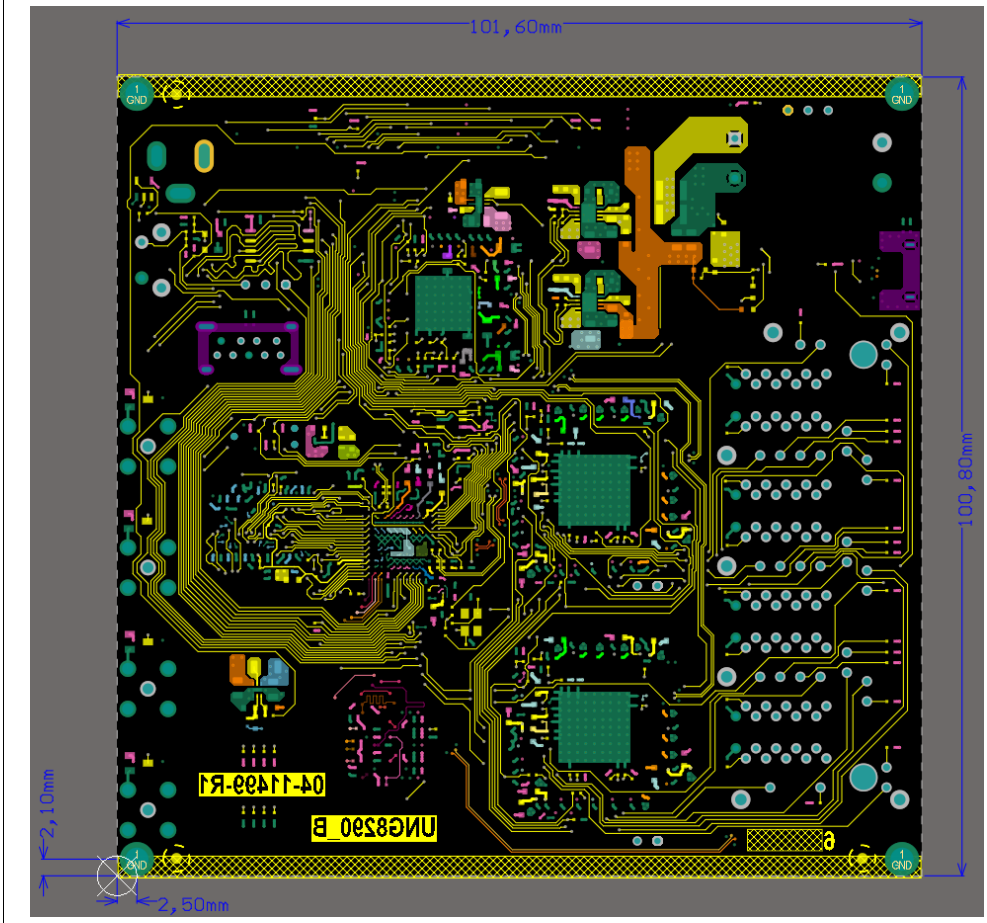
5.2.6 Layer 6 — Bottom

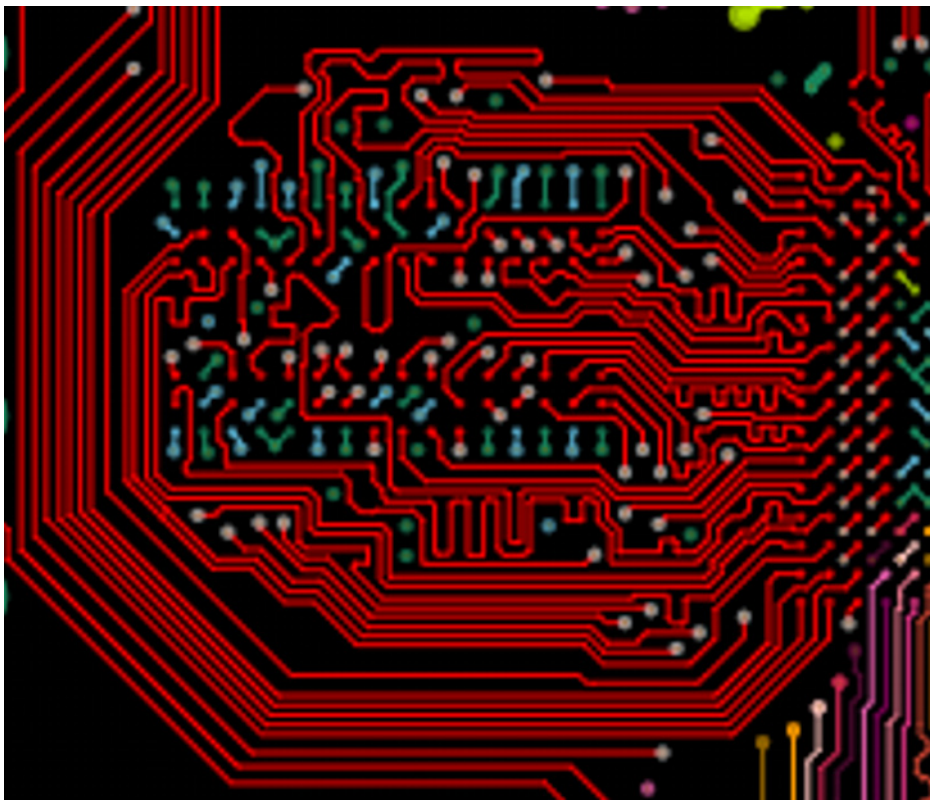
FIGURE 5-7: LAYER 6



Bottom layer is used for copper PHY MDI signals and PHY ground shield. Likewise, the inner layer signal path for the SerDes macros can be found here.

5.2.7 DDR Close Up on Top Layer

FIGURE 5-8: LAYER 1 — DDR3L CLOSE UP



Close up to see how the DDR length matching is acquired.

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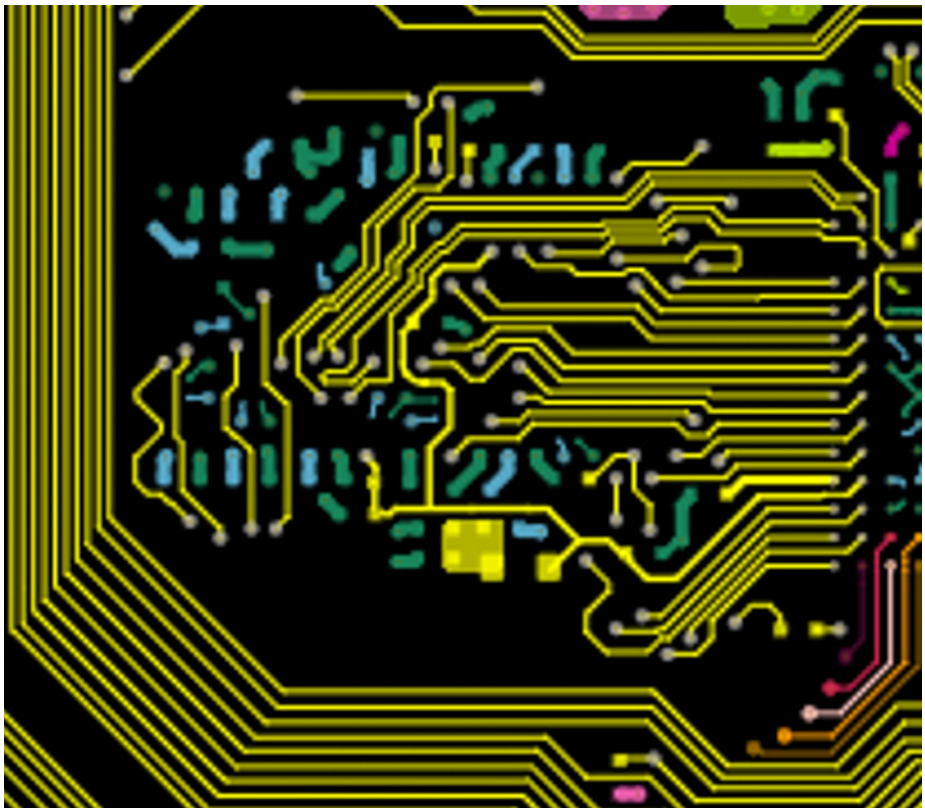
5.2.8 DDR Close Up on Bottom Layer

FIGURE 5-9: LAYER 8 — DDR3L CLOSE UP



Close up to see how the DDR length matching is acquired.

5.2.9 PCB Layer Stack-up

The reference board is a six-layer impedance-controlled PCB. The stack-up is shown in Figure 5-10.

FIGURE 5-10: PCB STACK-UP

#	Name	Material	Type	Weight	Thickness	Dk	Df
	Top Overlay		Overlay				
	Top Solder	Solder Resist	Solder Mask		0.394mil	3.5	
	Top Surface Finish	ENIG_3-6um Nickel (Ni), 0.05-0....	Surface Finish		0.18mil		
1	Top Layer 1	CF-003	Signal	1/2oz	2.008mil		
	Dielectric 1	PP-370HR-2113_59	Prepreg		4.016mil	4.02	0.021
2	Inner Layer 2	CF-003	Plane	1/2oz	0.709mil		
	Dielectric 3	CR-370HR-2x1080_7628	Core		12.008mil	4.24	0.018
3	Inner Layer 3	CF-003	Plane	1/2oz	0.709mil		
	Dielectric1	PP-370HR	Prepreg		22mil	4.3	0.018
4	Inner Layer 4	CF-003	Plane	1/2oz	0.709mil		
	Dielectric 4	CR-370HR-2x1080_7628	Core		12.008mil	4.24	0.018
5	Inner Layer 5	CF-003	Plane	1/2oz	0.709mil		
	Dielectric 2	PP-370HR-2113_59	Prepreg		4.016mil	4.02	0.021
6	Bottom Layer 6	CF-003	Signal	1/2oz	2.008mil		
	Bottom Surface Finish	ENIG_3-6um Nickel (Ni), 0.05-0....	Surface Finish		0.18mil		
	Bottom Solder	Solder Resist	Solder Mask		0.394mil	3.5	
	Bottom Overlay		Overlay				

5.3 PCB TRACE WIDTHS AND CLEARANCE

- Board thickness 1.6 mm ±10%
- Characteristic impedance single-ended 70Ω
- Characteristic impedance differential signals 100Ω
- Single-ended trace width 125 µm
- Single-ended trace to trace clearance 125 µm
- 100Ω differential trace width 125 µm
- 100Ω differential trace to trace clearance 125 µm

TABLE 5-2: NET IMPEDANCE AND LENGTH MATCHING

Net Group Name	Type	Impedance	Length matching	Tolerance (mm)	Max Vias	Via type	Layers	Notes
Clock	Single-ended	50	None	—	4	All	All	—
SI	Single-ended	50	None	—	4	All	All	Daisy-chain
DDR_CMD_LANE	SE/DIFF	60	Within lane	1	2	All	All	2
DDR_DQ_LANE0	SE/DIFF	60	Within lane	1	2	All	All	2
DDR_DQ_LANE1	SE/DIFF	60	Within lane	1	2	All	All	2
USB	Differential	90	P/N only	1	2	All	All	—
DiffClock	Differential	100	P/N only	1	2	All	All	—
SerDes	Differential	100	P/N only	0	2	—	Outer	1
Sense	Analog	—	—	—	—	All	All	—
Power	Power	—	—	—	—	—	—	—
Static	Single-ended	—	—	—	—	—	All	See Note 3
Unspecified	Single-ended	60	—	—	—	—	All	See Note 4

Note 1: Differential signal on outer layers.
2: DDR SE impedance 60R between devices.
3: No impedance => 4 mil trace on any layer.
4: Any unspecified nets should be routed as 60Ω.

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Chapter 6. Initial Board Bring-Up Procedure

6.1 INTRODUCTION

The Bring-Up phase for this platform will be deemed complete when the following have been completed:

1. All regulators function correctly under loaded and no-load conditions.
2. Power LEDs function correctly.
3. Reset functions correctly.
4. Clocks are OK. Maserati/Indy PLL lock is OK.
5. SPI NOR boot Flash is OK: Flash device can be programmed, and the CPU can boot from SPI NOR (uBoot).
6. USB management (serial port) is OK.
7. DDR is OK: CPU can init and train DDR successfully
8. eMMC is OK: CPU can load SwitchApp/MESA from eMMC
9. MIIM PHY communication is OK.
10. QSGMII links are OK (local loopback).
11. PHY link LEDs are OK.
12. Traffic test is OK on all ports.
13. PHY traffic LEDs are OK.
14. PTP signals on SMA connectors are OK.
15. Expansion header signals

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