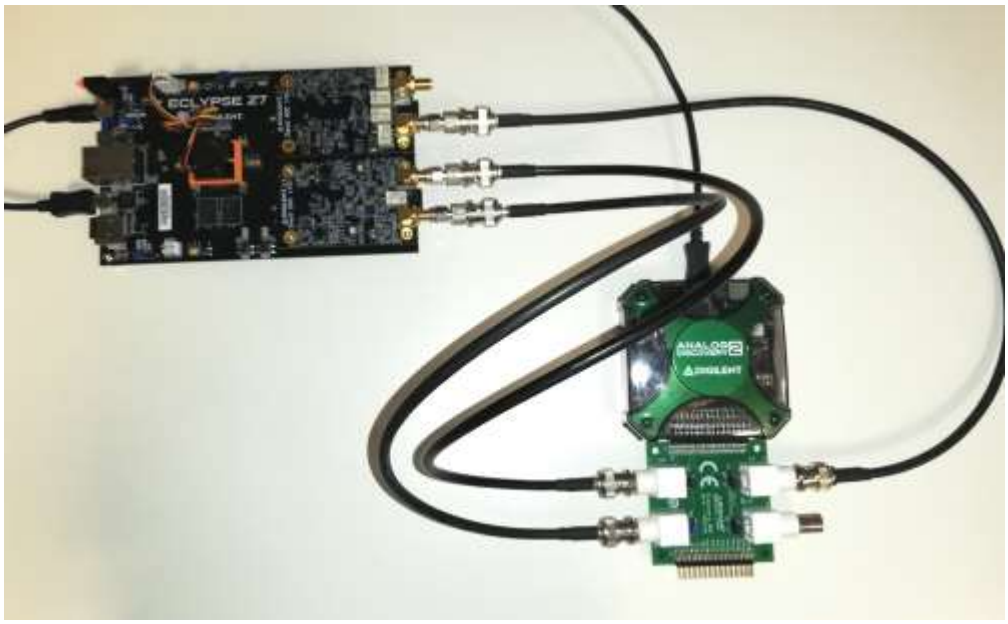
Eclypse Z7 Low Level Zmod ADC DAC Demo

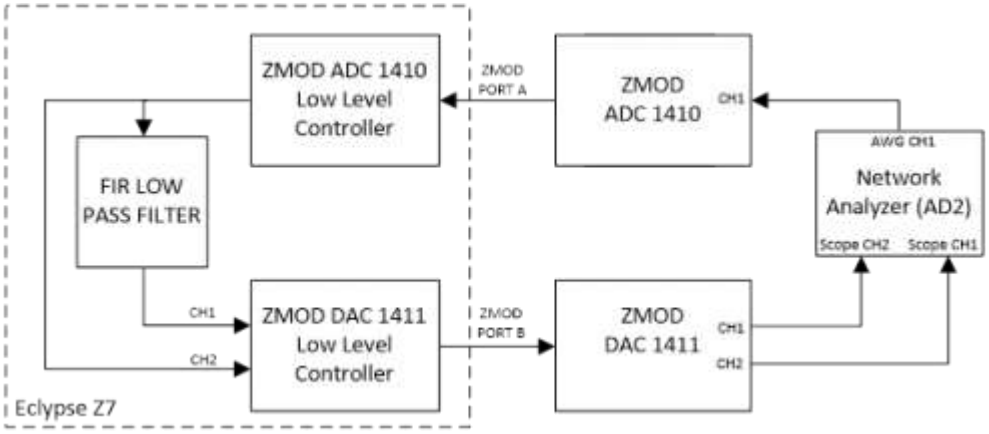


Overview

The project demonstrates the implementation of a basic signal processing application on the Eclypse platform (Eclypse Z7 + Zmod ADC + Zmod DAC).

Description

The simplified block diagram of the system implemented for this demo is shown below:



An analog input coming from the Analog Discovery 2 (AD2) is connected to the Zmod ADC 1410 CH1, converted to a digital format and passed on to the input of a digital low pass filter. The filter's output is converted back to an analog format by the Zmod DAC 1411 and can be measured/visualized on the converter channel 1.

The input signal, after the analog to digital conversion, is also looped back to the Zmod DAC 1411 and connected to CH2 output. The Analog Discovery 2's Network Analyzer instrument is then used to plot the frequency characteristic using the CH2 of the Zmod DAC 1411 as reference.

The purpose of the digital loopback is to correct the phase errors introduced by the ADC and Zmod ADC 1410 Low Level Controller latency and the gain errors caused by the mismatch between the ADC and the DAC full scale voltages.

With this setup the frequency response of the filter can be correctly measured regardless of the gain setting of the Zmod DAC 1411.

Only the Zynq's Programmable Logic (PL) is used for this project.

The IPs instantiated in the design and their functionality are described below:

- The Zmod ADC 1410 Low Level Controller - initializes the Zmod ADC 1410 hardware and synchronizes the incoming data in the user clock domain,
- A digital low pass filter – implemented using Xilinx FIR compiler 7.2 IP Core with the coefficients specified in Table 1, below.
- The Zmod DAC 1411 Low Level Controller - initializes the Zmod DAC 1411 hardware and formats the output data according to the AD9717 DAC requirements.

Inventory

Hardware

- Eclypse Z7
  - Including a **Micro-USB cable** and **12V Power Supply**
- Zmod ADC 1410
- Zmod DAC 1411
- Analog Discovery 2 (AD2)
- Discovery BNC Adapter

Software

- **Vivado Design Suite 2019.1** with **Digilent Board Support Files** installed
  - Follow the Installing Vivado, Xilinx SDK, and Digilent Board Files guide on how to install Vivado and Digilent Board Support Files.
- Waveforms Software

Skills

- **Basic familiarity with Vivado**
  - *This experience can be found by walking through our "Getting Started with Vivado" guide*

Demo Setup

Hardware Setup

1. Connect the Analog Discovery 2 board to the host computer using a MicroUSB cable.

2. Connect the Eclypse Z7 board to the host computer using a MicroUSB cable through PROG MicroUSB port and power the board using the 12V Power Supply. Flip its power switch to turn it on.

3. Connect the two Zmods ADC and DAC to the Zmod connectors of the Eclypse Z7 board as follows:

- Zmod ADC 1410 to ZMOD A connector of the board
- Zmod DAC 1411 to ZMOD B connector of the board

4. Connect the BNC adapter board to the Analog Discovery 2 board

5. Make the following physical connections:

- Analog Discovery 2 AWG1 to Zmod ADC 1410 CH1
- Zmod ADC1410 to Eclypse Z7 SYZYGY ZMOD A
- Zmod DAC1411 to Eclypse Z7 SYZYGY ZMOD B
- Zmod DAC1411 CH1 to Analog Discovery 2 SCOPE C2
- Zmod DAC1411 CH2 to Analog Discovery 2 SCOPE C1

Note: *Since the Zmods use SMA connectors, use of BNC-to-SMA cables (or BNC-to-SMA adapters with BNC or SMA cables) is recommended for the Zmod to BNC Adapter physical connections.*

Software Setup

1. Follow the instructions provided in the README file from [Digilent Vivado Scripts]() repository, to recreate the project:

- Using [git](), clone the repository on your host computer:

```
git clone --recursive https://github.com/Digilent/Eclypse-Z7-HW -b low_leve
l_zmod_adc_dac/master
```

- Open Vivado and use the instructions provided in Workflow 1 (Cloning a Repo that uses this Submodule) of the README. Make sure to change directory into the Eclypse-Z7-HW folder that was just cloned, prior to running the following command (if using the Vivado TCL Console instead of Python):

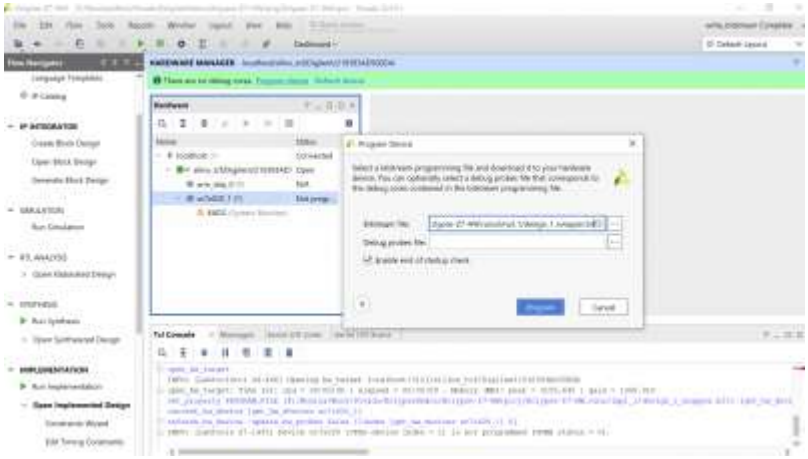
```
set argv ""; source digilent-vivado-scripts/digilent-vivado-checkout.tcl
```

2. Download and extract the demo files, linked in the Downloads section, above.

3. After recreating the project in Vivado, generate the bitstream file.

4. Make sure the boot mode jumper on the Eclypse Z7 is on the JTAG position.

5. Open Hardware Manager tool from within Vivado and click Open target, Autoconnect:



6. Select the .bit file, or make sure it is already selected and is located at the correct path in the dialog, and program the board.

7. Open WaveForms, then open the workspace, “EclypseZ7VhdlFilterDemo.dwf3work”, included in the folder extracted from the demo archive.

Hit the Run button of the Network Analyzer instrument.

Operating the Demo

The Network Analyzer will be used to generate a sinusoidal signal (perturbation) on the AWG1 channel. The bode plot (see below) is obtained considering the loopback signal (Zmod DAC 411 CH2) as reference.