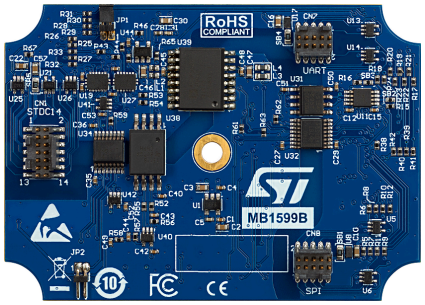
B-STLINK-ISOL

Data brief

Isolation and voltage adapter board for STLINK-V3SET



B-STLINK-ISOL top view. Picture is not contractual.

Product status link
B-STLINK-ISOL

Features

- 1.65 V - 3.3 V voltage adapter and galvanic isolation board for STLINK-V3SET
- 2.5 kV_{rms} insulation rating; 300 V_{rms} basic insulation working voltage per IEC 62368-1:2014
- Input/output isolation and level shifters for STM32 debug SWD, SWV, and JTAG signals
- Input/output isolation and level shifters for VCP Virtual COM port (UART) signals
- Input/output isolation and level shifters for bridge (SPI/UART/I^2C/CAN/GPIOs) signals
- Closed casing when using the STDC14 connector (STM32 SWD, SWV, and VCP)
- Connection compatible with the STLINK-V3SET adapter board (MB1440) for STM32 microcontrollers JTAG and bridge

Description

The B-STLINK-ISOL board is an additional module for STLINK-V3SET, performing galvanic isolation and voltage adaptation for STM32 microcontroller targets running below 3.3 V down to 1.65 V.

The module can be enclosed directly in the original STLINK-V3SET casing, when used as an STM32 debugging probe (JTAG/SWD/SWV/VCP) through the STDC14 connector. It can be also inserted between the STLINK-V3SET main board (MB1441) and its adapter board (MB1440) when providing access to bridge signals and other connectors.

B-STLINK-ISOL does not support STM8 targets, for which voltage adaptation is performed on the baseline adapter board (MB1440) provided with the STLINK-V3SET.

1 Ordering information

To order the B-STLINK-ISOL module, refer to Table 1. For details, refer to the user manual on the STLINK-V3SET product web page.

Table 1. Ordering information

Order code	Board reference	User manual	Description
B-STLINK-ISOL	MB1599	UM2448	Isolation and voltage adapter board for STLINK-V3SET

The STLINK-V3SET modular stand-alone debugging and programming probe embeds an STM32 32-bit microcontroller based on the Arm® Cortex®-M processor.

Note: Arm is a registered trademark of Arm Limited (or its subsidiaries) in the US and/or elsewhere.

Revision history

Table 2. **Document revision history**

Date	Version	Changes
14-Jan-2021	1	Initial release.