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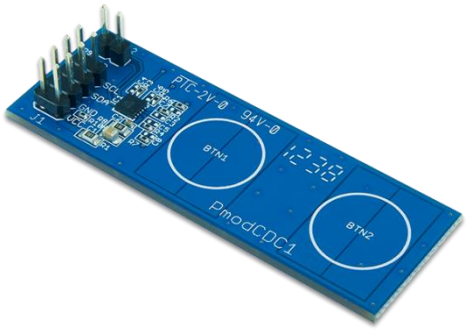
PmodCDC1™ Reference Manual

Revised December 17, 2015
This manual applies to the PmodCDC1 rev. B

Overview

The Digilent PmodCDC1 demonstrates capacitative-to-digital conversion through the use of Analog Devices AD7156. With its high input sensitivity and adaptive threshold capability, this Pmod is able to easily handle variance in environmental changes while still reporting accurate information.



The PmodCDC1.

Features include:

- Two capacitance input channels
- Fixed or adaptive threshold capability
- 400 kHz I²C communication protocol
- Sensitivity up to 3 fF

1 Functional Description

The PmodCDC1 utilizes a 12-bit capacitance-to-digital converter (CDC) to determine if the measured capacitance on a particular channel (conveniently labeled as BTN1 and BTN2 on the Pmod surface) is above, below, inside, or outside a user definable threshold level(s). Users are able to read the digital capacitance level on the most recently converted channel through I2C or can simply use the output pins on header J2 if they are only interested in knowing if a threshold has been crossed or not.

2 Interfacing with the Pmod

The PmodCDC1 communicates with the host board via the I²C protocol. The byte consisting of the 7-bit address for the on-board chip is 0x90 (10010000) for a write command and is 0x91 (10010001) for a read command.

On power-up the Pmod enters into continuous conversion mode with both of the channels alternately reporting their data. It also uses the adaptive threshold mode where the output is active (high) only when the sensed capacitance is lower than the difference of the average measured capacitance and the sensitivity (a sensitivity of

about 12 fF). Users can choose to either detect when the output of a channel crosses its threshold by "watching" its respective output pin on header J2 for a high voltage or can get more specific information by querying the device through the I²C interface.

2.1 Example: Continuous Read with Default Settings

A communication transmission example taking advantage of continuous read capability and reporting the contents of the Status (address 0x00), most recent Channel 1 and Channel 2 data, and average Channel 1 and Channel 2 data registers, is shown below. The bit names are taken from the Analog Devices datasheet and are defined after the table.

Command byte									Address byte								
1	0	0	1	0	0	0	1	(ACK)	0	0	0	0	0	0	0	0	(ACK)
Status[1]																	
PwrDown		DacStep2		OUT2		DacStep1		OUT1	C1/C2		RDY2		RDY1		(ACK)		
Ch 1 Data High									Ch 1 Data Low[2]								
b11	b10	b9	b8	b7	b6	b5	b4	(ACK)	b3	b2	b1	b0	0	0	0	0	(ACK)
Ch 2 Data High									Ch 2 Data Low								
b11	b10	b9	b8	b7	b6	b5	b4	(ACK)	b3	b2	b1	b0	X	X	X	X	(ACK)
Ch 1 Avg High									Ch 1 Avg Low								
b11	b10	b9	b8	b7	b6	b5	b4	(ACK)	b3	b2	b1	b0	0	0	0	0	(ACK)
Ch 2 Avg High									Ch 2 Avg Low								
b11	b10	b9	b8	b7	b6	b5	b4	(ACK)	b3	b2	b1	b0	X	X	X	X	(ACK)

Status Register Bit Values		
Bit	**Mnemonic**	**Description**
7	PwrDown	PwrDown = 1 indicates that the part is in a power-down
6	DacStep2	DacStep2 = 0 indicates that the Channel 2 CAPDAC value was changed after the last CDC conversion as part of the auto-DAC function. The bit value is updated after each finished CDC converion on this channel.
5	OUT2	OUT2 = 1 indicates that the Channel 2 data (CIN2 capacitance) crossed the threshold, according to the selected comparator mode of operation. The bit value is updated after each finished CDC conversion on this channel.
4	DacStep1	DacStep1 = 0 indicates that the Channel 1 CAPDAC value was changed after the last CDC conversion as part of the auto-DAC function. The bit value is updated after each finished CDC converion on this channel.
3	OUT1	OUT2 = 1 indicates that the Channel 1 data (CIN1 capacitance) crossed the threshold, according to the selected comparator mode of operation. The bit value is updated after each finished CDC conversion on this channel.
2	C1/C2	C1/C2 = 0 indicates that the last finished CDC conversion was on Channel 1. C1/C2 = 1 indicates that the last finished CDC conversion was on Channel 2.
1	RDY2	RDY2 = 0 indicates a finished CDC conversion on Channel 2. The bit is reset back to 1 when the Channel 2 data register is read via the serial interface or after a part reset or power-up.
0	RDY1	RDY1 = 0 indicates a finished CDC conversion on Channel 1. The bit is reset back to 1 when the Channel 1 data register is read via serial interface or after a part reset or power-up.

[1] The bits of the status register are defined in their own table (from the Analog Devices datasheet).
[2] The last four bits of each data set are not part of the 12-bit data conversion and so are either 0's or don't cares (X)

2.2 Pinout Description Table

Header J1		
Pins	**Signal**	**Description**
1 & 5	SCL	Serial Clock
2 & 6	SDA	Serial Data
3 & 7	GND	Power Supply Ground
4 & 8	VCC	Power Supply (3.3V/5V)

Header J2		
Pin	**Signal**	**Description**
1	O1	Output of BTN1
2	O2	Output of BTN2

Any external power applied to the PmodCDC1 must be within 1.8V and 3.6V; it is recommended that Pmod is operated at 3.3V.

3 Physical Dimensions

The pins on the main pin header are spaced 100 mil apart. The PCB is 2.3 inches long on the side parallel to the pins on the pin header and 0.8 inches long on the side perpendicular to the pin header.