Memory Module Specifications

NTBSD3N16SP-08

8GB (2Rx8 512M x 64-Bit) PC3L-12800
CL11 204-Pin SO-DIMM

DESCRIPTION

NTBSD4N16SP-08 is a 512M x 64-bit (8GB) DDR3L-1600 CL11 SDRAM (Synchronous DRAM), 2Rx8, memory module, based on sixteen 512M x 8-bit FBGA components per module. The SPD is programmed to JEDEC standard latency DDR3-1600 timing of 11-11-11 at 1.35V. Each 204-pin DIMM uses gold contact fingers. The electrical and mechanical specifications are as follows:

FEATURES

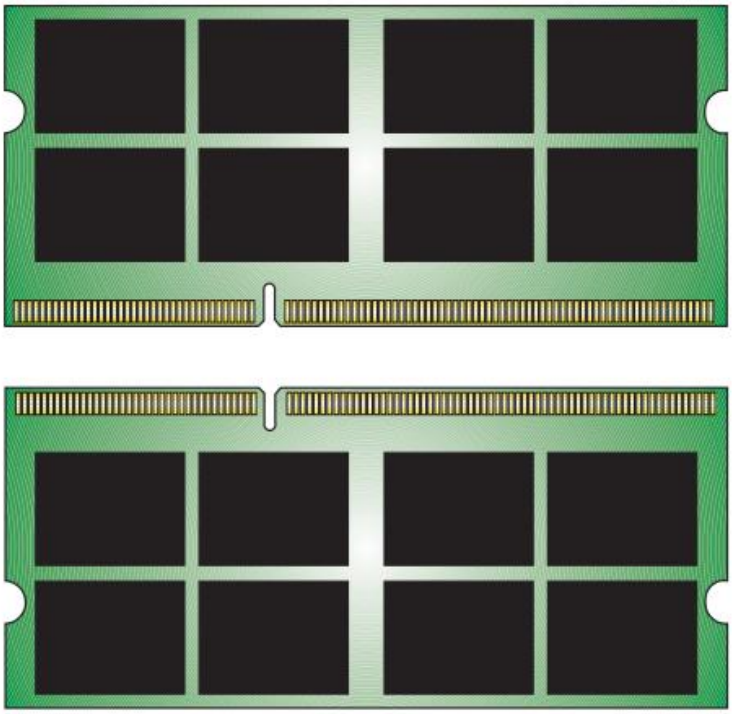
- JEDEC standard 1.35V (1.28V ~ 1.45V) and 1.5V (1.425V ~1.575V) Power Supply
- V_{DDQ} = 1.35V(1.28V~1.45V)and 1.5V (1.425V ~ 1.575V)
- 800MHz fCK for 1600Mb/sec/pin
- 8 independent internal bank
- Programmable CAS Latency: 11, 10, 9, 8, 7, 6
- Programmable Additive Latency: 0, CL - 2, or CL - 1 clock
- 8-bit pre-fetch
- Burst Length: 8 (Interleave without any limit, sequential with starting address “000” only), 4 with t_{CCD} = 4 which does not allow seamless read or write [either on the fly using A12 or MRS]
- Bi-directional Differential Data Strobe
- Internal(self) calibration : Internal self calibration through ZQ pin (RZQ : 240 ohm ± 1%)
- On Die Termination using ODT pin
- Average Refresh Period 7.8us at lower than TCASE 85°C, 3.9us at 85°C < TCASE ≤ 95°C
- Asynchronous Reset
- PCB : Height 1.18” (30mm), double sided component
- RoHS Compliant and Halogen-Free

SPECIFICATIONS

CL(IDD)	11 cycles
Row Cycle Time (tRCmin)	48.125ns(min.)
Refresh to Active/Refresh Command Time (tRFCmin)	260ns(min.)
Row Active Time (tRASmin)	35ns(min.)
Maximum Operating Power	TBD W*
UL Rating	94V-0
Operating Temperature	0º C to +70º C
Storage Temperature	-40º C to +85º C

*Power will vary depending on the SDRAM used.

MODULE DIMENSIONS



All measurements are in millimeters.
(Tolerances on all dimensions are ±0.12 unless otherwise specified)