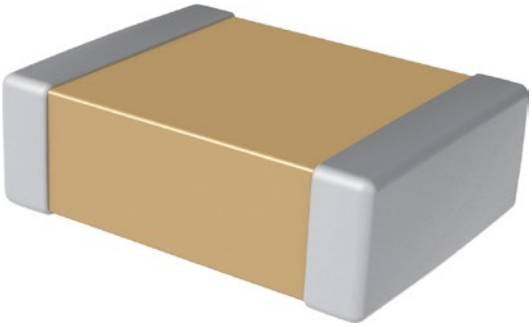
Multilayer Capacitors, SMD

Multilayer Ceramic Capacitors, 0805, Y5V



SPECIFICATION:

Construction form	0805
Ceramic type	Y5V
Capacitance tolerance	-20...+80%
Height	1.25 mm
Length	2.0 mm
Temperature range	-25...+85 °C
Width	1.25 mm

PRODUCT RANGE:

Art. Nr.	Capacitance	Rated voltage
RND 1500805Y103Z500NT	10 nF	50 VDC
RND 1500805Y104Z160NT	100 nF	16 VDC
RND 1500805Y104Z250NT	100 nF	25 VDC
RND 1500805Y104Z500NT	100 nF	50 VDC
RND 1500805Y105Z500N3	1.0 µF	50 VDC
RND 1500805Y106Z063N3	10 µF	6.3 VDC
RND 1500805Y106Z100N3	10 µF	10 VDC
RND 1500805Y154Z250NT	150 nF	25 VDC
RND 1500805Y154Z500NT	150 nF	50 VDC
RND 1500805Y155Z160N3	1.5 µF	16 VDC
RND 1500805Y223Z500NT	22 nF	50 VDC
RND 1500805Y224Z160NT	220 nF	16 VDC
RND 1500805Y224Z250NT	220 nF	25 VDC
RND 1500805Y224Z500NT	220 nF	50 VDC
RND 1500805Y225Z160N3	2.2 µF	16 VDC
RND 1500805Y333Z500NT	33 nF	50 VDC
RND 1500805Y334Z250NT	330 nF	25 VDC
RND 1500805Y335Z100N3	3.3 µF	10 VDC
RND 1500805Y473Z500NT	47 nF	50 VDC
RND 1500805Y474Z160NT	470 nF	16 VDC
RND 1500805Y475Z100N3	4.7 µF	10 VDC
RND 1500805Y475Z160N3	4.7 µF	16 VDC
RND 150C0805X106K100N3	10 µF	10 VDC

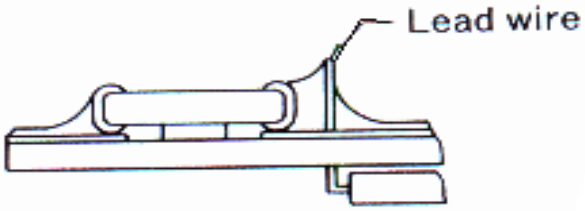
PCB design

Chip components are susceptible to board stress since the component itself is mounted directly on the board. They are also sensitive to mechanical and thermal stress when solder, which may cause chip cracked.
Please take solder form and component layout into consideration to eliminate stress.

Pattern form

(1) Placing of chip components and component.

incorrect



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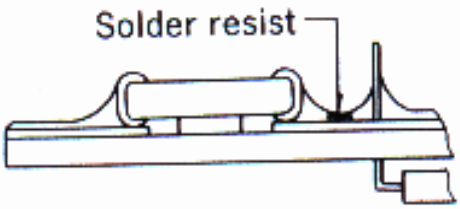
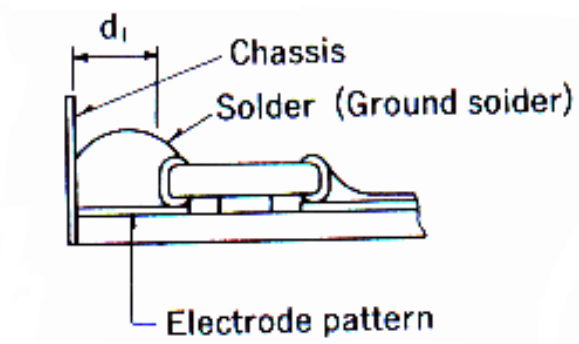
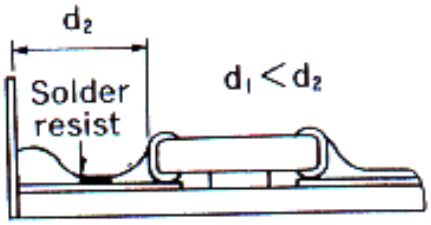


(2) Placing close to chassis.

incorrect

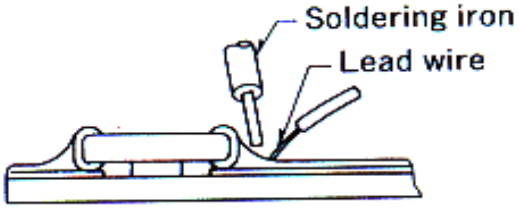


correct



(3) Placing leaded components after chip component.

incorrect



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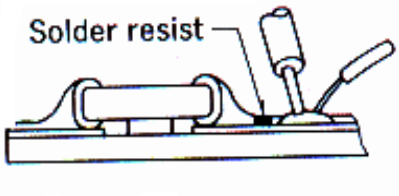
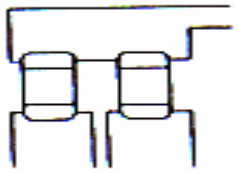


(4) Lateral mounting

incorrect



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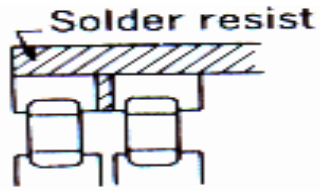
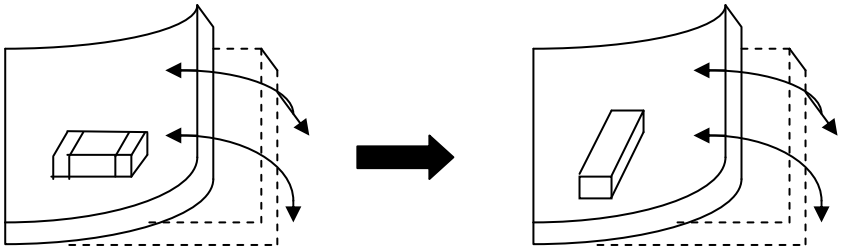


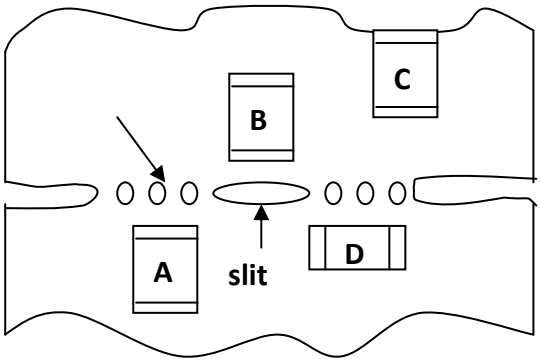
Component direction

To design a mounting position that minimizes the stress imposed on the chip during flexing or bending of the board.

(1) put the component lateral to the direction in which stress acts.



(2) Component layout close to board separation point.
Susceptibility to stress in the order: A＞C＞B＝D



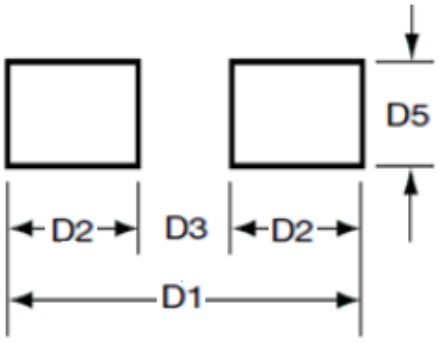
12.3. Land Pattern

When capacitors are mounted on P.C. board, the amount of solder directly affect the performance of capacitors. Therefore, the following items should be carefully considered in the design of solder land pattern.

(1) The greater the amount of solder, the higher the stress on the chip capacitors, and lead to cracking and breaking likely. It is necessary the appropriate size and configuration of the solder pads should be designed to have proper amount of solder on the termination.

(2) When two or more capacitors are soldered together onto the same land or pad, the pad must be designed so that each capacitor's soldering point is separated by solder-resist.

The following diagram and table for recommended pad dimensions.



Dimensions in millimeters

Type	0201	0402	0603	0805	1206	1210	1808	1812	1825	2220	2225
D1	0.65	1.50	2.30	2.80	4.00	4.00	5.40	5.30	5.30	7.00	7.00
D2	0.21	0.50	0.80	0.90	0.90	0.90	1.05	0.90	0.90	1.35	1.35
D3	0.23	0.50	0.70	1.00	2.20	2.20	3.30	3.50	3.50	4.30	4.30
D5	0.30	0.50	0.80	1.30	1.60	2.50	2.30	3.80	6.50	5.00	6.50

Unit: mm