Taiwan Semiconductor



N-Channel Power MOSFET

100V, 6.5A, 95mΩ

FEATURES

- Fast switching
- Pb-free plating
- RoHS compliant
- Halogen-free mold compound

APPLICATION

- Networking
- Load Switch
- Lighting

KEY PERFORMANCE PARAMETERS				
PARAM	ETER	VALUE	UNIT	
V _{DS}		100	V	
R _{DS(on)} (max)	$V_{GS} = 10V$	95		
	$V_{GS} = 4.5V$	110	mΩ	
Q_g		9.3	nC	





Note: MSL 3 (Moisture Sensitivity Level) per J-STD-020

ABSOLUTE MAXIMUM RATINGS (T _A = 25°C unless otherwise noted)					
PARAMETER		SYMBOL	LIMIT	UNIT	
Drain-Source Voltage		V _{DS}	100	V	
Gate-Source Voltage		V _{GS}	±20	V	
Q (Note 1)	$T_{\rm C} = 25^{\circ}{\rm C}$	- I _D	6.5	А	
Continuous Drain Current (Note 1)	$T_{\rm C} = 100^{\circ}{\rm C}$		4.1		
Pulsed Drain Current (Note 2)		I _{DM}	26	А	
Total Power Dissipation @ $T_C = 25^{\circ}C$		P _{DTOT}	9	W	
Operating Junction and Storage Tempera	ature Range	T_J,T_STG	- 55 to +150	°C	

Pin 3

THERMAL PERFORMANCE				
PARAMETER	SYMBOL	LIMIT	UNIT	
Junction to Case Thermal Resistance	R _{eJC}	14	°C/W	
Junction to Ambient Thermal Resistance	R _{ƏJA}	62	°C/W	

Notes: $R_{\Theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistances. The case thermal reference is defined at the solder mounting surface of the drain pins. $R_{\Theta JC}$ is guaranteed by design while $R_{\Theta CA}$ is determined by the user's board design. $R_{\Theta JA}$ shown below for single device operation on FR-4 PCB in still air

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PARAMETER	CONDITIONS	SYMBOL	MIN	ТҮР	MAX	UNIT
Static (Note 3)		1		1	1	
Drain-Source Breakdown Voltage	$V_{GS} = 0V, I_D = 250 \mu A$	BV _{DSS}	100			V
Gate Threshold Voltage	$V_{DS} = V_{GS}, I_{D} = 250 \mu A$	V _{GS(TH)}	1.2	1.6	2.5	V
Gate Body Leakage	$V_{GS} = \pm 20V, V_{DS} = 0V$	I _{GSS}			±100	nA
Zero Gate Voltage Drain Current	$V_{DS} = 100V, V_{GS} = 0V$	I _{DSS}			1	μA
	$V_{GS} = 10V, I_{D} = 5A$	_		80	95	mΩ
Drain-Source On-State Resistance	$V_{GS} = 4.5V, I_D = 3A$	R _{DS(on)}		85	110	
Dynamic (Note 4)	·					
Total Gate Charge		Qg		9.3		
Gate-Source Charge	$V_{DS} = 48V, I_D = 5A,$	Q _{gs}		2.1		nC
Gate-Drain Charge	- V _{GS} = 10V	Q _{gd}		1.8		-
Input Capacitance	$V_{DS} = 50V, V_{GS} = 0V,$ f = 1.0MHz	C _{iss}		1480		
Output Capacitance		C _{oss}		480		pF
Reverse Transfer Capacitance		C _{rss}		35		
Gate Resistance	f = 1MHz, open drain	R _g		1.3		Ω
Switching (Note 5)						•
Turn-On Delay Time	$V_{DD} = 30V,$ $R_{GEN} = 3.3\Omega,$ $I_D = 1A, V_{GS} = 10V,$	t _{d(on)}		2.9		
Turn-On Rise Time		t _r		9.5		
Turn-Off Delay Time		t _{d(off)}		18.4		ns
Turn-Off Fall Time		t _f		5.3		
Source-Drain Diode (Note 3)						
Forward On Voltage	$I_{S} = 3.3A, V_{GS} = 0V$	V _{SD}			1	V
Continuous Drain-Source Diode		I _S			6.5	Α
Pulse Drain-Source Diode		I _{SM}			26	А

Notes:

Current limited by package 1.

2. Pulse width limited by the maximum junction temperature

3. Pulse test: PW \leq 300µs, duty cycle \leq 2%

4. For DESIGN AID ONLY, not subject to production testing.

Switching time is essentially independent of operating temperature. 5.



ORDERING INFORMATION

ORDERING CODE	PACKAGE	PACKING
TSM950N10CW RPG	SOT-223	2,500pcs / 13" Reel

Note:

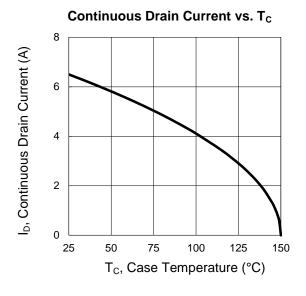
1. Compliant to RoHS Directive 2011/65/EU and in accordance to WEEE 2002/96/EC

2. Halogen-free according to IEC 61249-2-21 definition

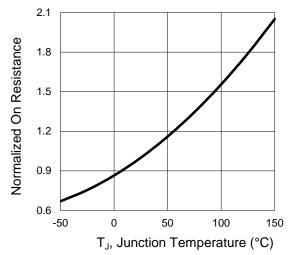


CHARACTERISTICS CURVES

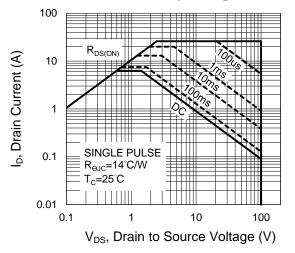
 $(T_C = 25^{\circ}C \text{ unless otherwise noted})$

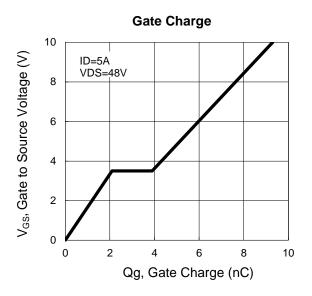


On-Resistance vs. Junction Temperature

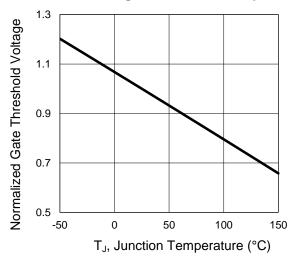


Maximum Safe Operating Area

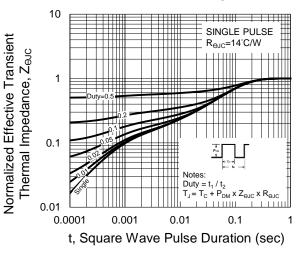




Threshold Voltage vs. Junction Temperature



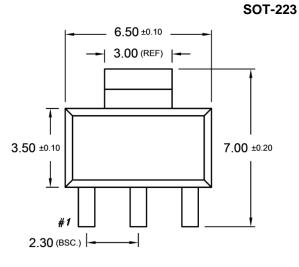
Normalized Thermal Transient Impedance Curve

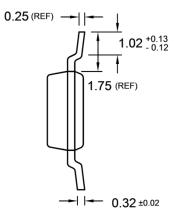


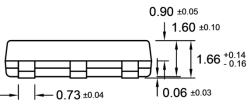


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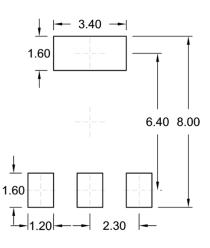
PACKAGE OUTLINE DIMENSIONS (Unit: Millimeters)







SUGGESTED PAD LAYOUT (Unit: Millimeters)



MARKING DIAGRAM

	Y = Year CodeM = Month Code for Halogen Free Production	uct		
950N10 YML	\mathbf{O} = Jan \mathbf{P} = Feb \mathbf{Q} = Mar			
	S = May T = Jun U = Jul	•		
	W =Sep X =Oct Y =Nov	Z =Dec		
L = Lot Code (1~9, A~Z)				



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