



# VN340SP-E

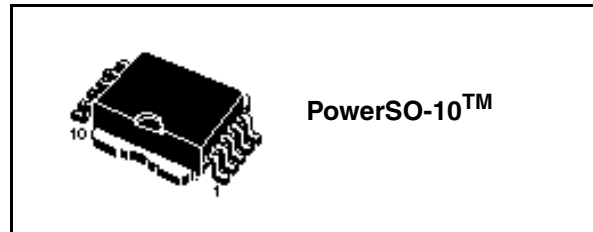
Quad high side smart  
Power solid state relay

## Features

Type	$V_{\text{demag}}^{(1)}$	$R_{\text{DSon}}^{(1)}$	$I_{\text{out}}^{(1)}$	$V_{\text{CC}}$
VN340SP-E	$V_{\text{CC}}-55\text{V}$	$0.2\Omega$	0.7A	36V

1. Per channel.

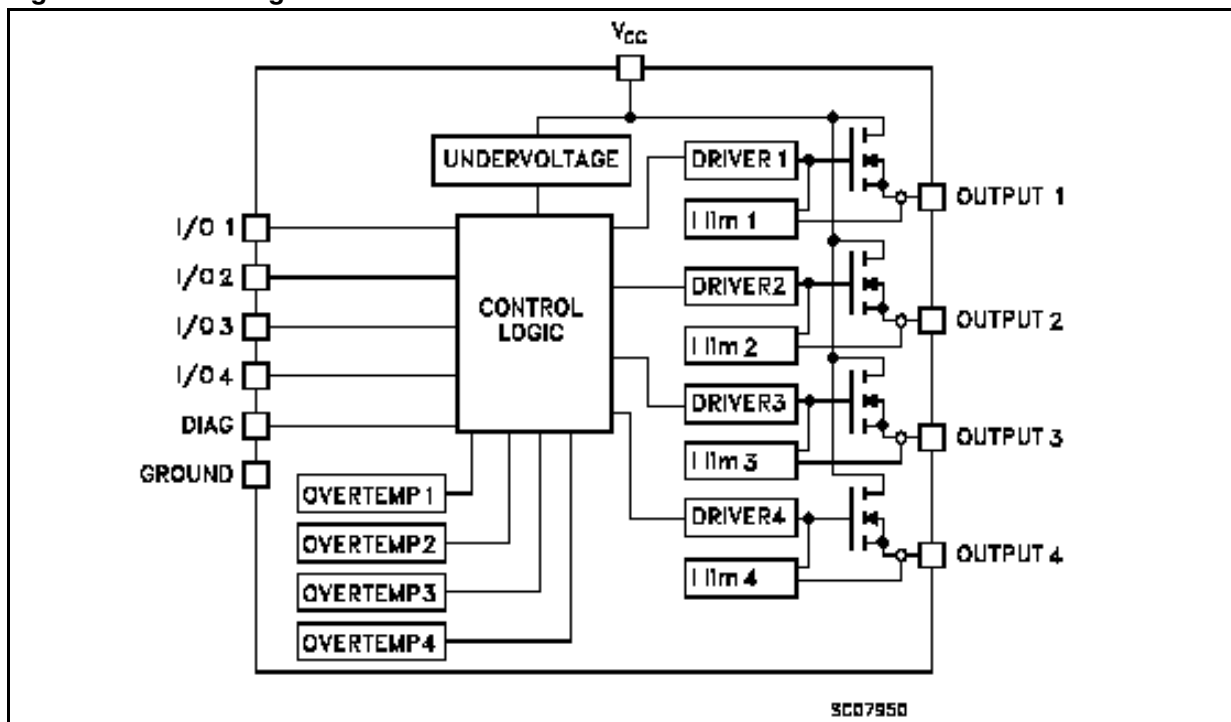
- Output current : 0.7A per channel
- Digital I/O's clamped at 32V minimum voltage
- Shorted load and overtemperature protections
- Protection against loss of ground
- Built-in current limiter
- Undervoltage shut-down
- Open drain diagnostic output
- Fast demagnetization of inductive loads
- Conforms to IEC 61131-2



## Description

The VN340SP-E is a monolithic device made using STMicroelectronics VIPower technology, intended for driving four independent resistive or inductive loads with one side connected to ground. Active current limitation avoids dropping the system power supply in case of shorted load. Built-in thermal shut-down protects the chip from overtemperature and short circuit. The open drain diagnostic output indicates overtemperature conditions. Each I/O is pulled down when overtemperature condition of the relative channel is verified.

Figure 1. Block diagram



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# 1 Maximum ratings

**Table 1. Absolute maximum rating**

Symbol	Parameter	Value	Unit
$V_{CC}$	Power supply voltage	45	V
$-V_{CC}$	Reverse supply voltage	-4	V
$I_{OUT}$	Output current (continuous)	Internally limited	A
$I_R$	Reverse output current (per channel)	-6	A
$I_{IN}$	Input current (per channel)	$\pm 10$	mA
$I_{DIAG}$	Diag pin current	$\pm 10$	mA
$V_{ESD}$	Electrostatic discharge (R = 1.5K $\Omega$ ; C = 100pF)	2000	V
$E_{AS}$	Single pulse avalanche energy per channel not simultaneously <a href="#">Figure 4.</a>	400	mJ
$P_{tot}$	Power dissipation at $T_c = 25^\circ\text{C}$	Internally limited	w
$T_J$	Junction operating temperature	Internally limited	$^\circ\text{C}$
$T_{STG}$	Storage temperature	-55 to 150	$^\circ\text{C}$

**Table 2. Thermal data**

Symbol	Parameter	Max Value	Unit
$R_{thJC}$	Thermal resistance junction-case <sup>(1)</sup>	Max 3	$^\circ\text{C}/\text{W}$
$R_{thJA}$	Thermal resistance junction-ambient <sup>(2)</sup>	Max 50	$^\circ\text{C}/\text{W}$

1. Per channel
2. When mounted using minimum recommended pad size on FR-4 board

## 2 Pin connections

Figure 2. Connection diagram (top view)

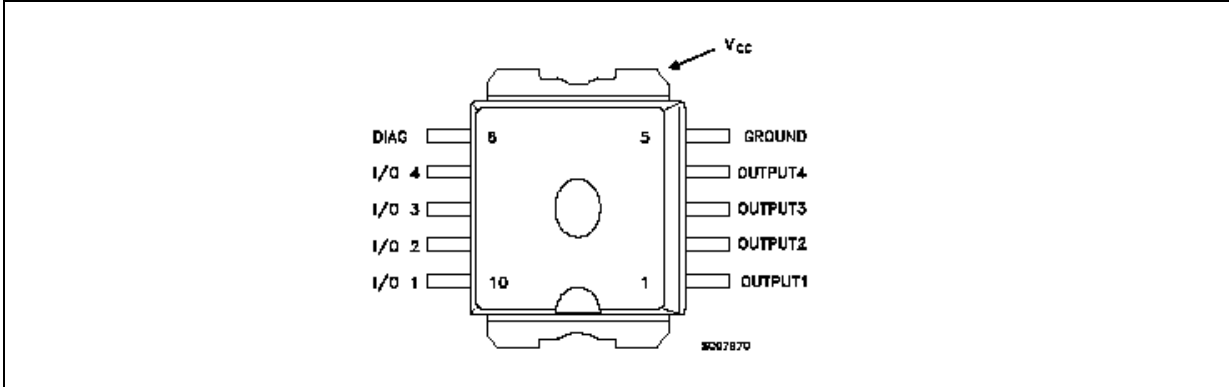
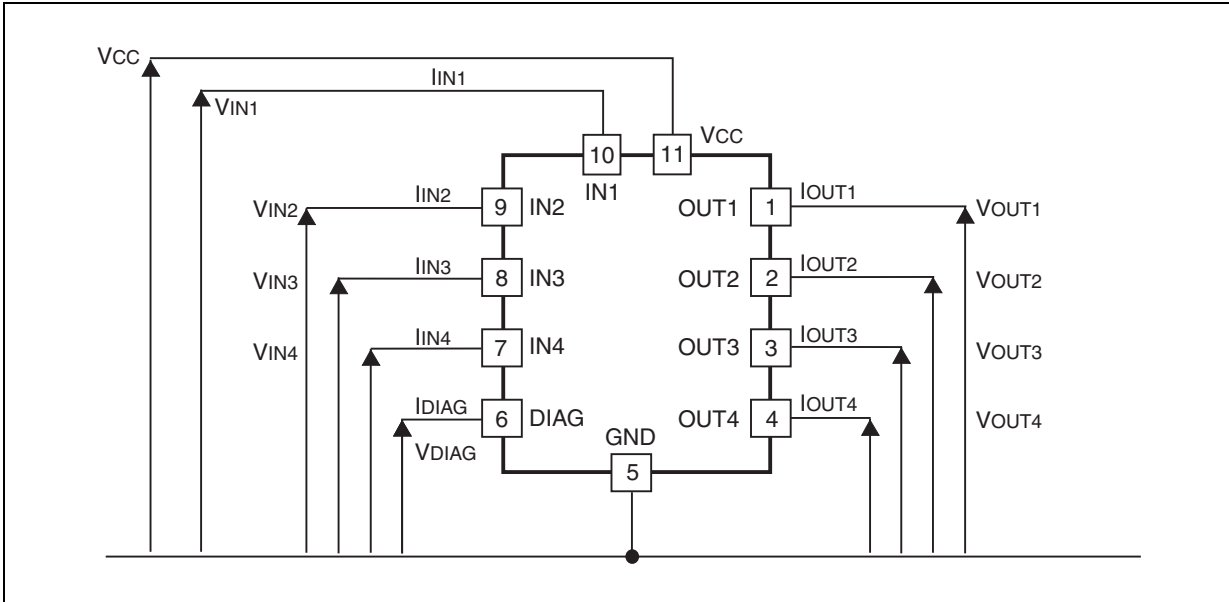


Figure 3. Current and voltage conventions



### 3 Electrical characteristics

10V < V<sub>CC</sub> < 36V; -40°C < T<sub>J</sub> < 125°C; unless otherwise specified

**Table 3. Power section**

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
V <sub>CC</sub>	Supply voltage		10		36	V
R <sub>ON</sub>	On state resistance	I <sub>OUT</sub> = 0.5A; T <sub>J</sub> = 25°C I <sub>OUT</sub> = 0.5A; T <sub>J</sub> = 85°C I <sub>OUT</sub> = 0.5A; T <sub>J</sub> = 125°C			0.2 0.32 0.4	Ω Ω Ω
I <sub>S</sub>	Supply current	All channels OFF On state; V <sub>IN</sub> = 30V; I <sub>OUT</sub> = 0V (T <sub>J</sub> = 125°C)			1 6	mA mA
V <sub>OL</sub>	Low state output voltage	V <sub>IN</sub> = V <sub>IL</sub> ; R <sub>LOAD</sub> ≥ 10MΩ			1.5	V
V <sub>demag</sub>	Output voltage at turn-off	I <sub>OUT</sub> = 0.5A; L <sub>LOAD</sub> ≥ 1mH	V <sub>CC</sub> -65	V <sub>CC</sub> -55	V <sub>CC</sub> -45	V
I <sub>LGND</sub>	Output current at turn-off	V <sub>CC</sub> = V <sub>INn</sub> = V <sub>GND</sub> = V <sub>STAT</sub> = 18 to 30V T <sub>amb</sub> = - 25°C to 85°C <a href="#">Figure 6.</a>			2	mA

**Table 4. Switching ( V<sub>CC</sub> = 24V)**

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
t <sub>d(ON)</sub>	Turn-on delay time of Output current	I <sub>OUT</sub> = 0.5A, resistive load input rise time < 0.1μs, T <sub>J</sub> = 25°C		52	100	μs
t <sub>r</sub>	Rise time of output current	I <sub>OUT</sub> = 0.5A, resistive load input rise time < 0.1μs, T <sub>J</sub> = 25°C		94	250	μs
t <sub>d(OFF)</sub>	Turn-off delay time of output current	I <sub>OUT</sub> = 0.5A, resistive load input rise time < 0.1μs, T <sub>J</sub> = 25°C		34	50	μs
t <sub>f</sub>	Fall time of output current	I <sub>OUT</sub> = 0.5A, resistive load input rise time < 0.1μs, T <sub>J</sub> = 25°C		8	20	μs

**Table 5. Logical input**

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
V <sub>IL</sub>	I/O Input low level voltage				2	V
V <sub>IH</sub>	I/O Input high level voltage <sup>(1)</sup>		3.5			V
V <sub>I(HYST)</sub>	I/O Input hysteresis voltage			0.5		V
I <sub>IN</sub>	I/O Input current	V <sub>IN</sub> = 30V			25	μA
V <sub>ICL</sub>	I/O Input clamp voltage <sup>(1)</sup>	I <sub>IN</sub> = 1mA I <sub>IN</sub> = -1mA	32	36 -0.7		V V

1. The input voltage is internally clamped at 32V minimum, it is possible to connect the input pins to an higher voltage via an external resistor calculate to not exceed 10mA

**Table 6. Protection and diagnostic**

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
$V_{DIAG}^{(1)}$	Status voltage output low	$I_{DIAG} = 5\text{mA}$ ( Fault condition )			1	V
$V_{SCL}^{(1)}$	Status clamp voltage	$I_{DIAG} = 1\text{mA}$	32	36		V
		$I_{DIAG} = 1\text{mA}$		-0.7		V
$V_{USD}$	Undervoltage shut down		5		8	V
$I_{LIM}$	DC Short circuit current	$V_{CC} = 24\text{V}; R_{LOAD} < 10\text{m}\Omega$	0.7		2	A
$I_{OVPK}$	Peak short circuit current	$V_{CC} = 24\text{V}; V_{IN} = 30; R_{LOAD} < 10\text{m}\Omega$			4	A
$I_{DIAGH}$	Leakage ondiag pin in high state	$V_{DIAG} = 24\text{V}$			25	$\mu\text{A}$
$I_{LOAD}$	Output leakage current	$V_{CC} = 10 \text{ to } 36\text{V}; V_{IN} = V_{IL}$			50	$\mu\text{A}$
$t_{SC}$	Delay time of current limiter				100	$\mu\text{s}$
$T_{TSD}$	Thermal shut down temperature		150	170		$^{\circ}\text{C}$
$T_R$	Thermal reset temperature		135	155		$^{\circ}\text{C}$

1. Status determination > 100 $\mu\text{s}$  after the switching edge.

**Note:** If INPUT pin is floating the corresponding channel will automatically switch OFF. If GND pin is disconnected, the channel will switch OFF provided  $V_{CC}$  not exceed 36V.

## 4 Test circuits

Figure 4. Avalance energy test circuit

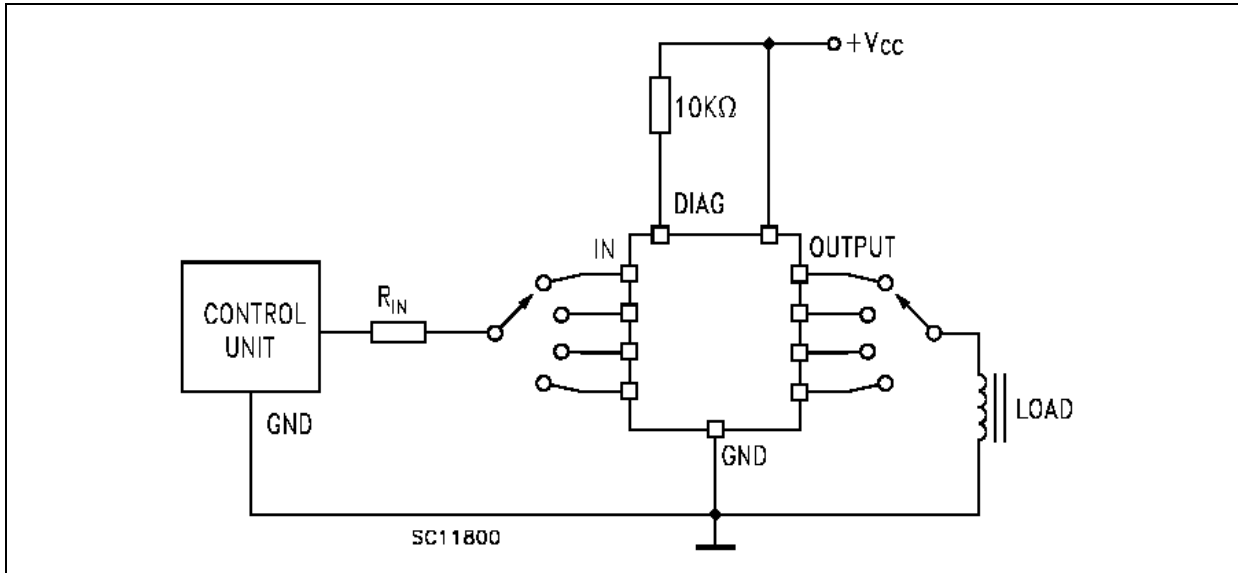
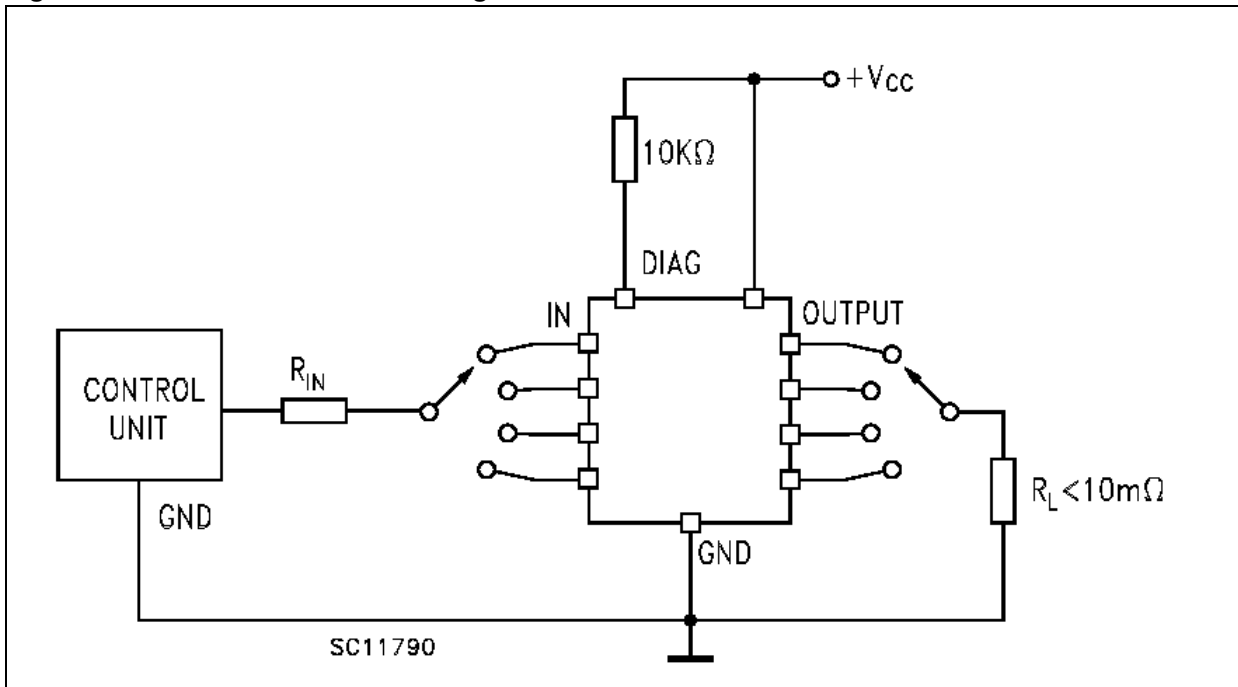
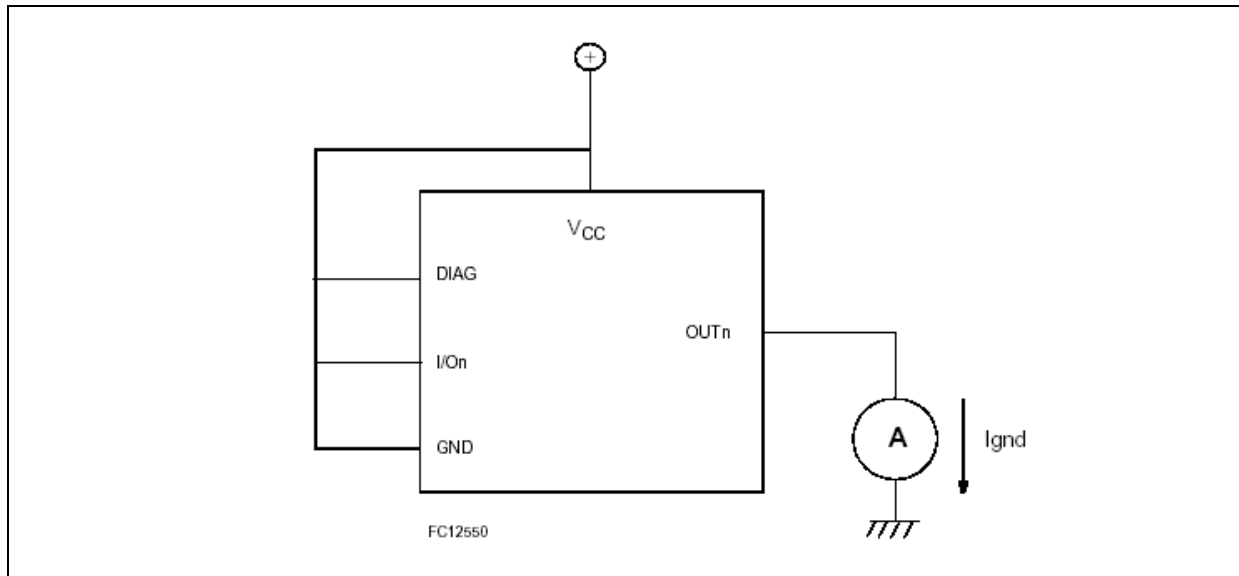


Figure 5. Peak short circuit test diagram



**Figure 6.**  $I_{LGND}$  test configuration





## 5 Switching time waveforms and truth table

Figure 7. Switching waveforms

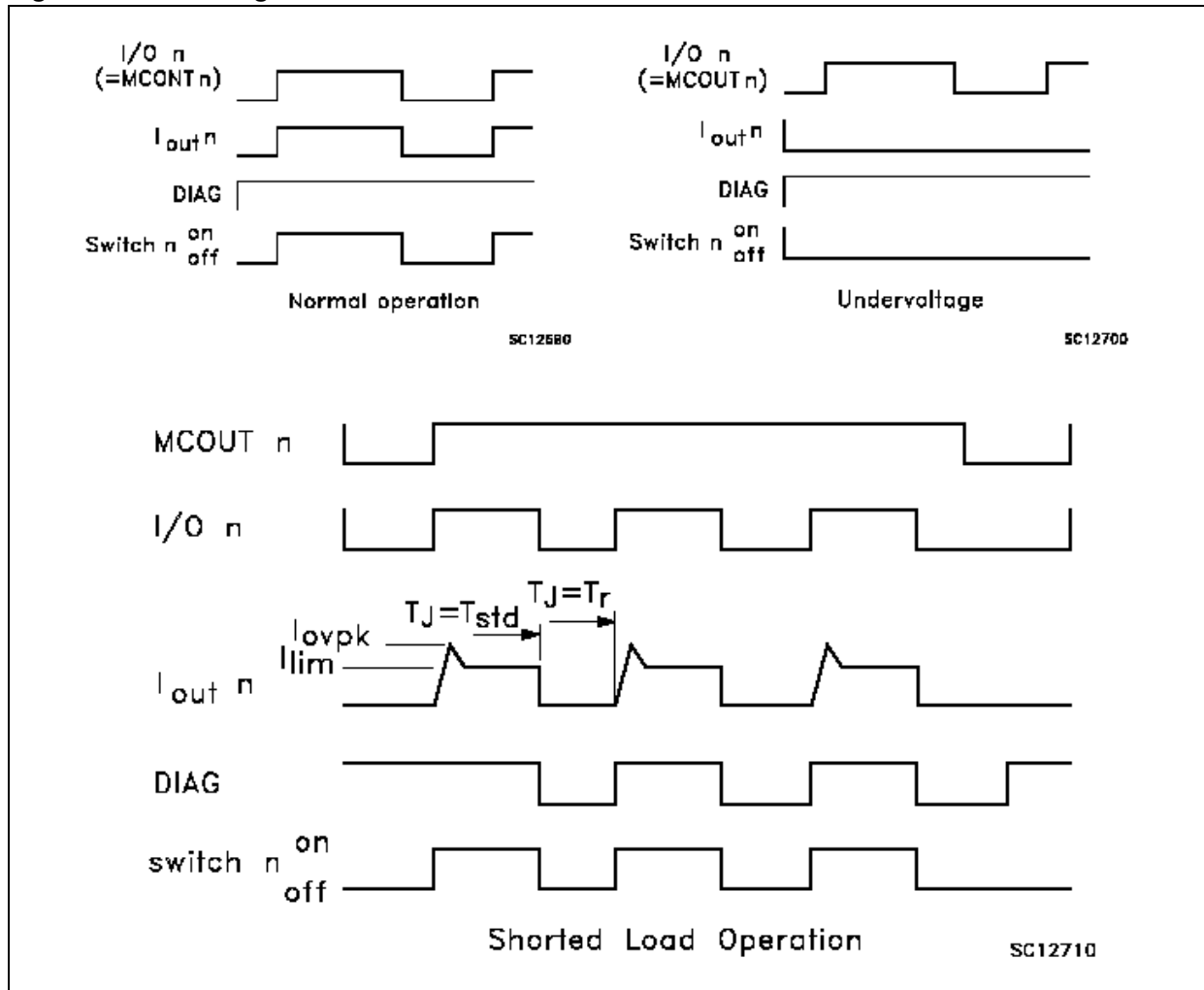
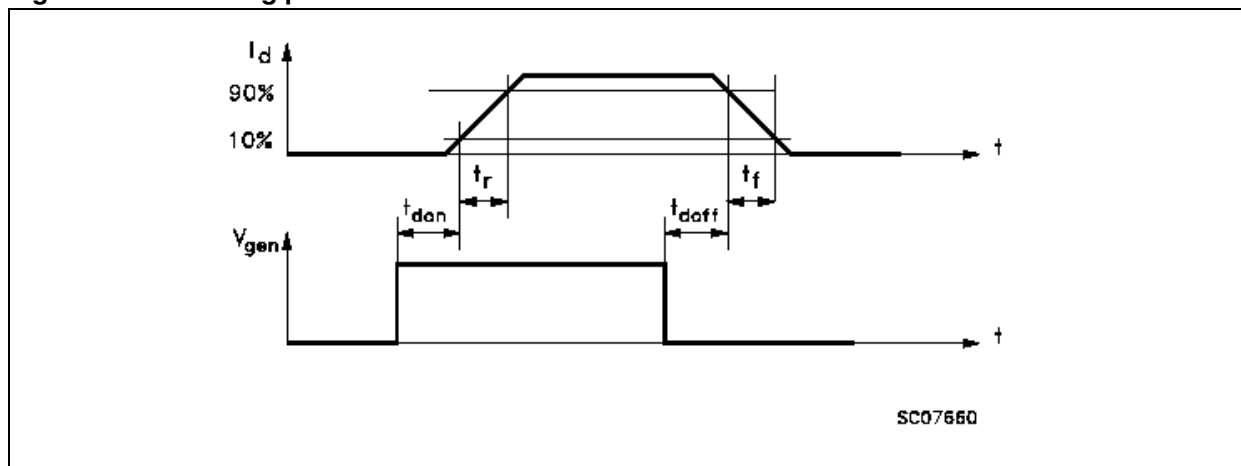


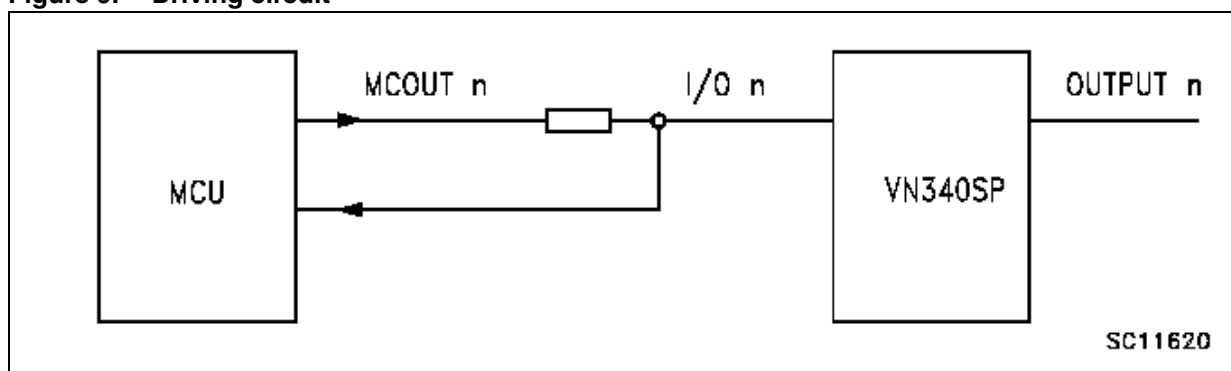
Figure 8. Switching parameter test conditions



**Table 7. Truth table**

	MCOUTn	I/O n	OUTPUTn	Diagnostic
Normal operation	L	L	L	H
	H	H	H	H
Overtemperature	L	L	L	H
	H	L	L	L
Undervoltage	L	L	L	H
	H	H	L	H
Shorted load ( Current limitation )	L	L	L	H
	H	H	H	H

**Figure 9. Driving circuit**



## 6 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect . The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: [www.st.com](http://www.st.com)

**Table 8. PowerSO-10 Mechanical data**

Dim	Mm			Inch		
	Min	Typ	Max	Min	Typ	Max
A	3.35		3.65	0.132		0.144
A1	0.00		0.10	0.000		0.004
B	0.40		0.60	0.016		0.024
c	0.23		0.32	0.009		0.012
D	9.40		9.60	0.370		0.378
D1	7.40		7.60	0.291		0.300
E	9.30		9.50	0.366		0.374
E1	7.20		7.40	0.283		0.291
E2	7.20		7.60	0.283		0.300
E3	6.10		6.35	0.240		0.250
E4	5.90		6.10	0.232		0.240
e		1.27			0.050	
F	1.25		1.35	0.049		0.053
H	13.80		14.40	0.543		0.567
h		0.50			0.002	
L	1.20		1.80	0.047		0.071
q		1.70			0.067	
a	0°		8°			

**Figure 10. Package dimension**

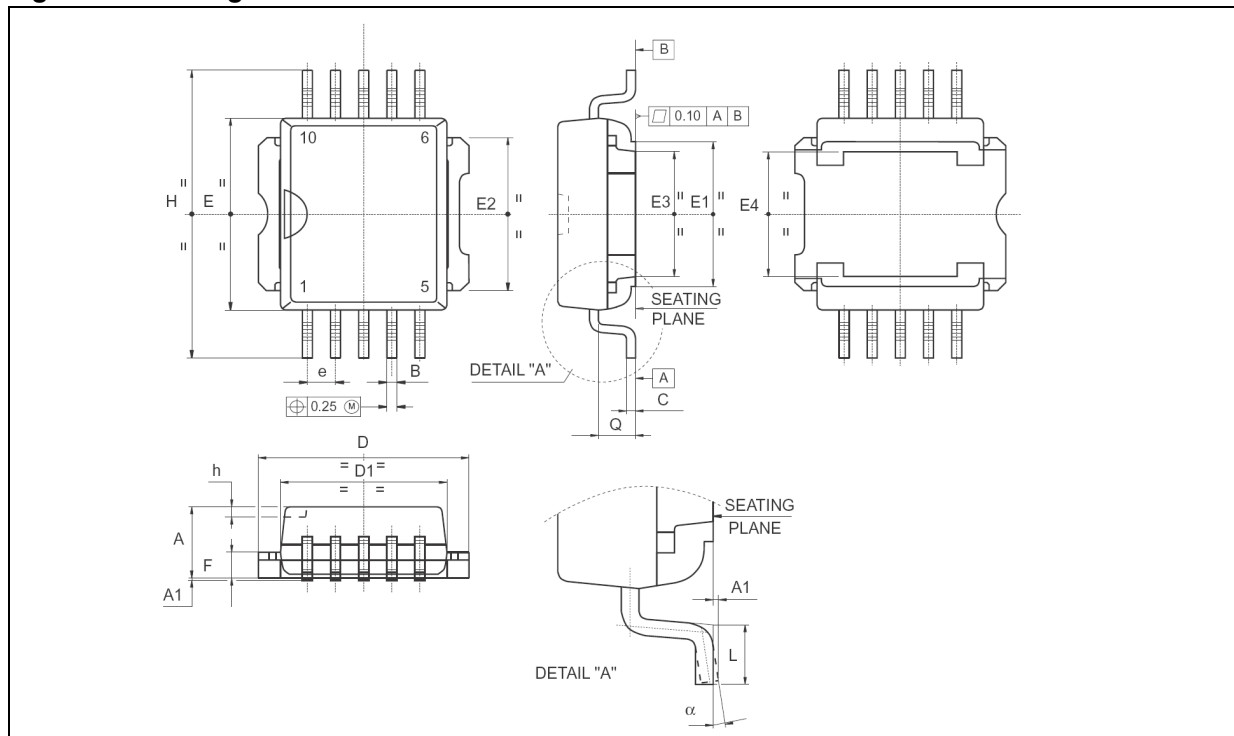


Figure 11. PowerSO-10™ Suggested Pad and Tube Shipment (No Suffix)

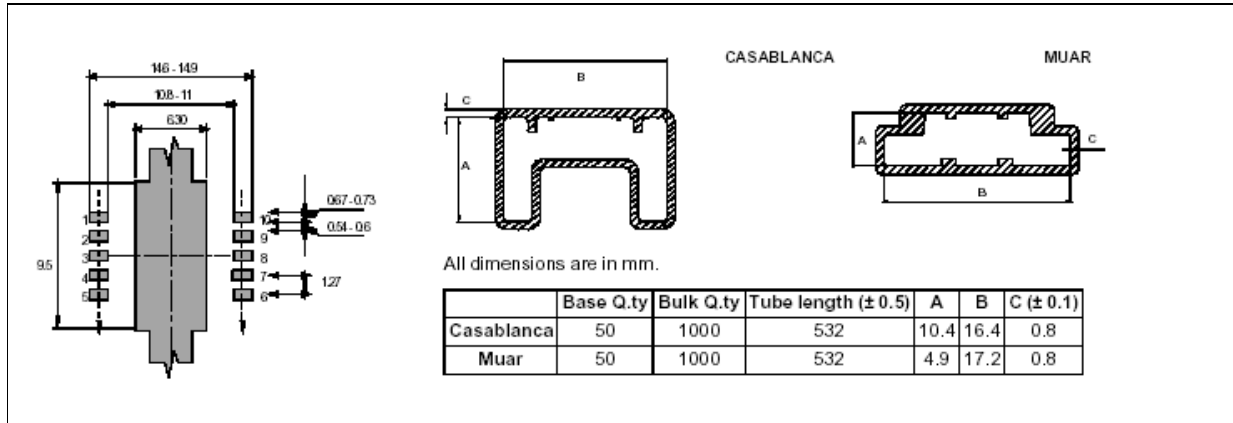
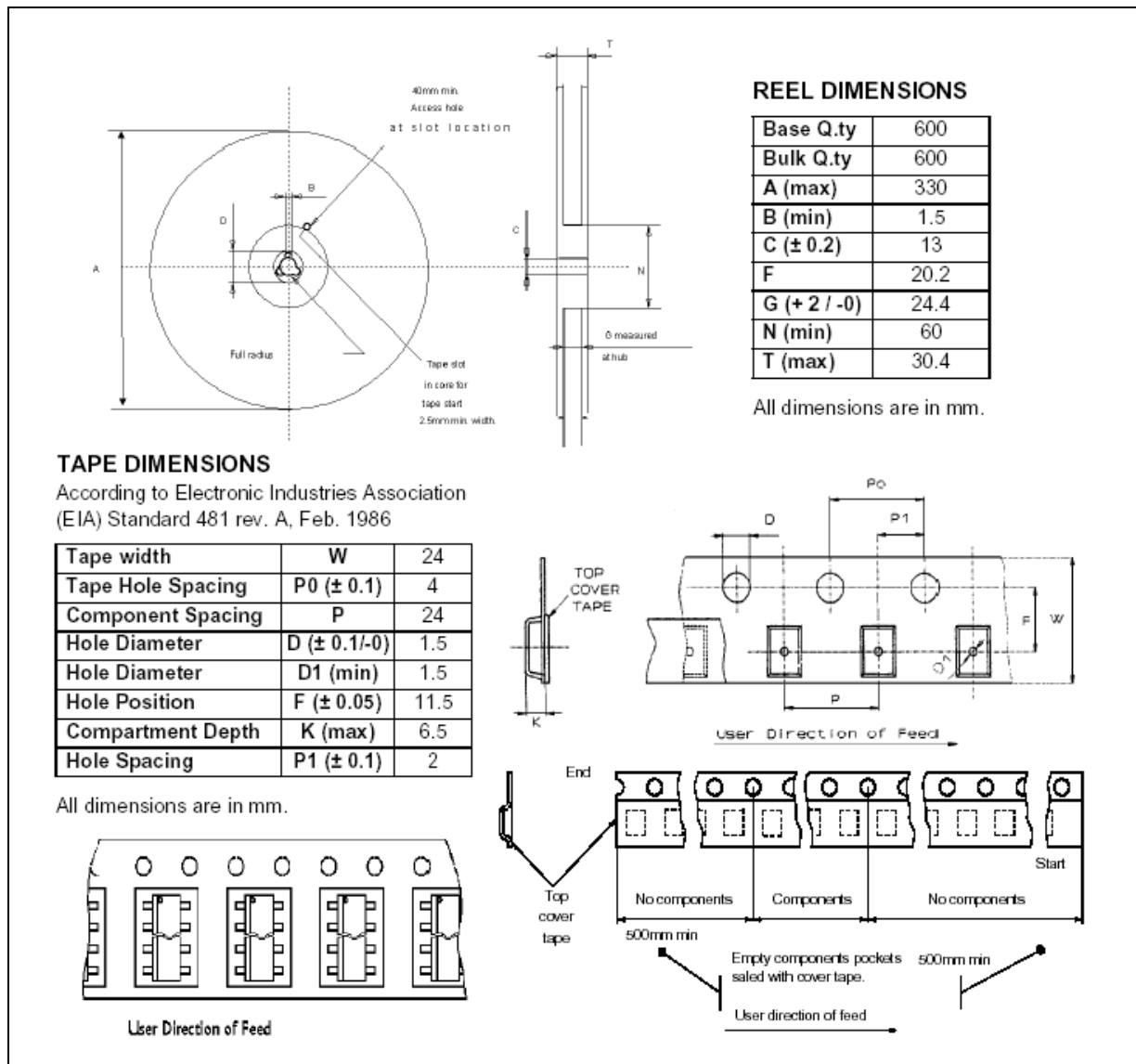


Figure 12. Tape and Reel Shipment (Suffix “TR“)



## 7 Order code

**Table 9. Order code**

Part number	Package	Packaging
VN340SP-E	PowerSO-10 <sup>TM</sup>	Tube
VN340SPTR-E	PowerSO-10 <sup>TM</sup>	Tape and reel

## 8 Revision history

**Table 10. Revision history**

Date	Revision	Changes
5-Sep-2005	1	Initial release
27-Jun-2006	2	Mechanical data updated
18-Sep-2006	3	Mechanical data updated, Added powerSO-10 Tape and reel information
31-Oct-2006	4	Typo in Electrical characteristics temperature conditions updated <a href="#">on page 5</a>
05-Mar-2007	5	Document reformatted, typo in <a href="#">Note 1 on page 6</a>

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