iC-MB3

BiSS INTERFACE MASTER, 1-Chan./3-Slaves

target specification

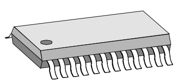
FEATURES

- Bidirectional *BiSS* sensor communication with up to 3 slaves
- Supports SSI protocol for unidirectional communication
- Synchronous sensor data acquisition with cyclic transfer at data rates of up to 10 Mbit/s
- Command and slave register operations during cyclic data transfers
- Data lengths of up to 64 bits for sensor data and multicycle data, independently scalable for each slave
- Automatic compensation of line delays, measurement and conversion times
- Data verification by CRC polynomials of up to 8 bits, adjustable per slave and data area
- Separate memory banks enable free controller access during *BiSS* sensor data transfers
- 32 bytes of intermediate memory to ease bidirectional slave register communications
- Parallel controller interface with an 8-bit data/address bus services Intel and Motorola devices
- Serial controller communication by SPI™-compatible mode
- Single 3 to 5V supply, industrial temperature range

APPLICATIONS

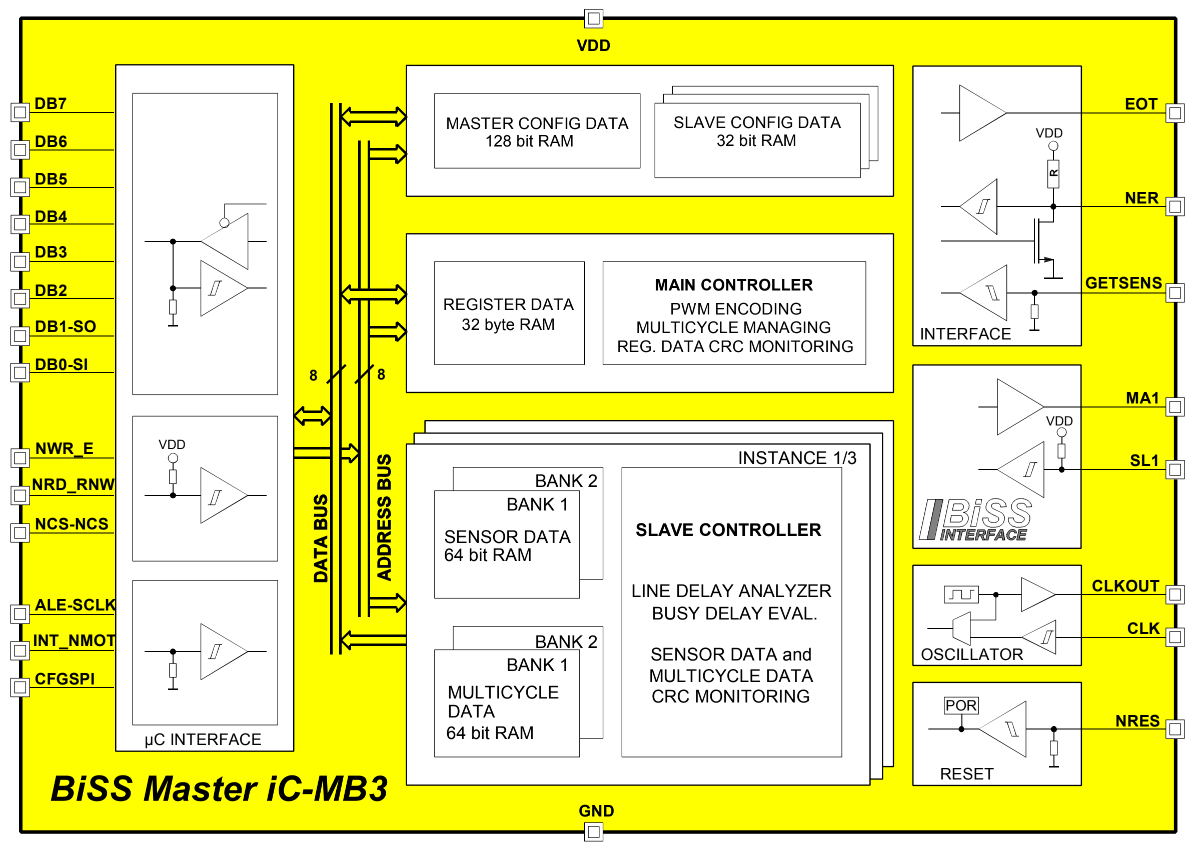
- Bidirectional device communication in multisensor systems
- Position measurement with linear or angular encoders
- Drive systems (motor feedback)

PACKAGES



TSSOP24

BLOCK DIAGRAM



SPI is a trademark of MOTOROLA, Inc.

DESCRIPTION

iC-MB3 is a single-chip *BiSS/SSI* interface controller featuring an 8-bit bus interface to industrial standard microcontrollers. An additional SPI interface mode also enables serial communication between iC-MB3 and the connected microcontroller.

One to three *BiSS* devices can be attached to the sensor side of the device. These are connected up to clock line MA1 and data return line SL1 using RS422 transceivers (Figure 1). The *BiSS* devices can be connected directly in noise-free environments.

A maximum of three *BiSS* slaves is supported, each with their own independently scalable data sections encompassing:

1) Sensor data from 0 to 64 bits
   (for measurement data, alarms and warnings)
2) Multicycle data from 0 to 64 bits
   (for additional measurement data)
3) Register data with 128 bytes per slave ID
   (e.g. for device parameters).

For both sensor and multicycle data iC-MB3 provides dual RAM memory banks for each slave, enabling flexible access to the microcontroller while new sensor data is being read in. A 32-byte intermediate memory supports register transfers.

Sensor data acquisition is started by a microcontroller command or via pin GETSENS. Alternatively, iC-MB3 can also read in new sensor data automatically; the cycle time in this instance can be set as required.

The end of sensor data acquisition and readin is signaled at pin EOT by a high; if faults occur during transmission pin NER signals a low. Errors in communication can be verified by the microcontroller via a status register; a system error message can also enter this register if bidirectional message pin NER is kept low by external intervention.

iC-MB3 generates a clock signal for sensor communication using an internal 20 MHz oscillator. The clock can also be supplied externally.

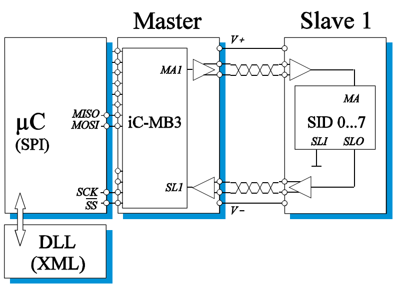


Figure 1: Point-to-point connection of iC-MB3 and one bus subscriber. This can use 1 to 8 slave IDs (SID).

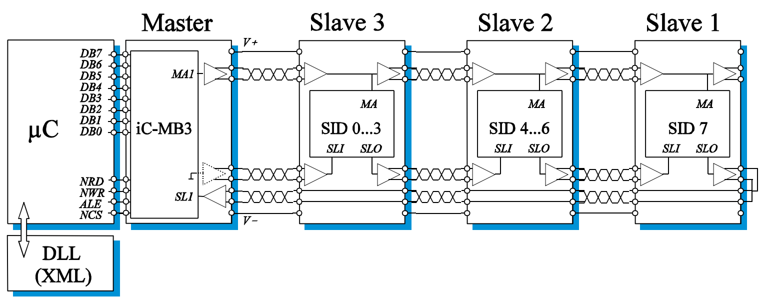
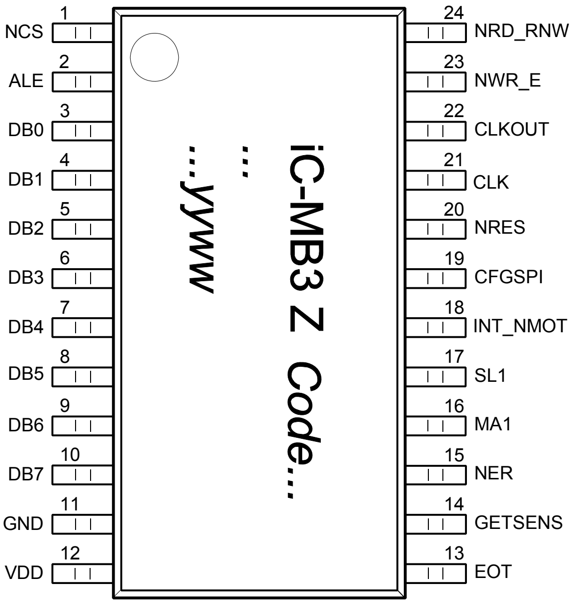


Figure 2: Example network of iC-MB3 and three subscribers. All 8 possible slave IDs (SIDs) are used distributed.

PACKAGES TSSOP24 to JEDEC Standard

PIN CONFIGURATION
TSSOP24 4.4 mm, lead pitch 0.65 mm
(top view)



PIN FUNCTIONS

No.	Name	Function
1	NCS	Chip Select Input, low active
2	ALE-SCLK	Address Latch Enable Input
3	DB0	Data Bus
4	DB1	Data Bus
5	DB2	Data Bus
6	DB3	Data Bus
7	DB4	Data Bus
8	DB5	Data Bus
9	DB6	Data Bus
10	DB7	Data Bus
11	GND	Ground
12	VDD	+3.3 ... +5V Supply Voltage
13	EOT	End-Of-Transmission Output
14	GETSENS	Sensor Data Request Input
15	NER	Error Message Input/Output, low active
16	MA1	*BiSS* Clock/Data Line Output
17	SL1	*BiSS* Data Line Input
18	INT_NMOT	Mode Select (Intel = 1, Motorola = 0)*
19	CFGSPI	Serial/Parallel Mode Select Input (serial SPI = 1, parallel = 0)
20	NRES	Reset Input, low active
21	CLK	External Clock Input
22	CLKOUT**	Clock Output
23	NWR_E	Write Input, low active (Intel) Enable Input, high active (Motorola)
24	NRD_RNW	Read Input, low active (Intel) Read/Not-Write Select Input (Motorola)

Serial SPI Communication Mode (CFGSPI = 1):

No.	Name	Function
1	NCS	Chip Select Input, low active
2	SCLK	SPI Clock Input
3	SI	SPI Serial Data Input
4	SO	SPI Serial Data Output

* only when CLKENI = 1 else no signal
** on SPI no effect

ABSOLUTE MAXIMUM RATINGS

Values beyond which damage may occur; device operation is not guaranteed.

Item	Symbol	Parameter	Conditions	Fig.	Min.	Max.	Unit
G001	VDD	Supply Voltage VDD			-0.3	6	V
G002	I(VDD)	Current in VDD			-20	30	mA
G003	V()	Voltage at all pins, excluding VDD and GND	V()≤ VDD + 0.3 V		-0.3	6	V
G004	I()	Current in all pins excluding VDD and GND			-10	10	mA
E001	Vesd()	ESD Susceptibility at all pins	MIL-STD-883, Method 3015, HBM 100 pF discharged through 1.5 kΩ			2	kV
TG1	Tj	Operating Junction Temperature			-40	150	°C
TG2	Ts	Storage Temperature Range			-40	150	°C

THERMAL DATA

Operating Conditions: VDD = 3 ... 5 V

Item	Symbol	Parameter	Conditions	Fig.	Min.	Typ.	Max.	Unit
T1	Ta	Operating Ambient Temperature Range (extended range to -25 °C is available on request)			-25		85	°C

All voltages are referenced to ground unless otherwise noted.
All currents into the device pins are positive; all currents out of the device pins are negative.

ELECTRICAL CHARACTERISTICS

Operating Conditions: VDD = 3 ... 5.5 V, Tj = -25 ... +125 °C, unless otherwise noted

Item	Symbol	Parameter	Conditions	Tj °C	Fig.	Min.	Typ.	Max.	Unit
Total Device									
001	VDD	Permissible Supply Voltage				3		5.5	V
002	I(VDD)	Supply Current in VDD	outputs not loaded, f(CLK) = 20 MHz					20	mA
003	Vc()hi	Clamp Voltage hi at all pins excluding VDD, GND	Vc()hi = V() - VDD, I() = 1 mA; outputs tristate			0.3		1.6	V
004	Vc()lo	Clamp Voltage lo at all pins excluding VDD, GND	I() = -1mA; outputs tristate			-1.6		-0.3	V
Control Interface: EOT, NER, GETSENS									
201	Vs()hi	Saturation Voltage hi at EOT	Vs()hi = VDD - V(); I() = -4 mA					400	mV
202	Vs()lo	Saturation Voltage lo at EOT, NER	I() = 4 mA					420	mV
203	Vt()hi	Threshold Voltage hi at NER, GETSENS						2	V
204	Vt()lo	Threshold Voltage lo at NER, GETSENS				0.8			V
205	Vt()hys	Threshold Voltage Hysteresis at NER, GETSENS				300	500		mV
206	Ipu()	Pull-Up Current at NER vs. VDD	V() = 0 ... VDD - 1.5 V			-600	-300	-60	µA
207	Ipd()	Pull-Down Current at GETSENS vs. GND	V() = 1.5 V ... VDD			4	35	70	µA
***BiSS Interface*: MA1, SL1**									
301	Vs(MA1)hi	Saturation Voltage hi	Vs()hi = VDD - V(); I() = -4 mA					400	mV
302	Vs(MA1)lo	Saturation Voltage lo	I() = 4 mA					420	mV
303	Vt(SL1)hi	Threshold Voltage hi						2	V
304	Vt(SL1)lo	Threshold Voltage lo				0.8			V
305	Vt(SL1)hys	Threshold Voltage Hysteresis				300	500		mV
306	Ipu(SL1)	Pull-Up Strom vs. VDD	V() = 0 ... VDD - 1.5 V			-70	-35	-5	µA
µC Interface: bidirectional data bus DB7 ... 0, Inputs NWR_E, NRD_RNW, NCS, ALE, INT_NMOT, CFGSPI									
401	Vs()hi	Saturation Voltage hi at DB7...0	Vs()hi = VDD - V(); I() = -4 mA					400	mV
402	Vs()lo	Saturation Voltage lo at DB7...0	I() = 4 mA					420	mV
403	Vt()hi	Threshold Voltage hi						2	V
404	Vt()lo	Threshold Voltage lo				0.8			V
405	Vt()hys	Threshold Voltage Hysteresis				300	500		mV
406	Ipd()	Pull-Down Current at DB7...0, ALE, CFGSPI, INT_NMOT to GND	V() = 1.5 V ... VDD			4	35	70	µA
407	Ipu()	Pull-Up Current at NRD_RNW, NWR_E, NCS vs.VDD	V() = 0 ... VDD-1.5 V			-70	-35	-4	µA

ELECTRICAL CHARACTERISTICS

Operating Conditions: VDD = 3 ... 5.5 V, Tj = -25 ... +125 °C, unless otherwise noted

Item	Symbol	Parameter	Conditions	Tj °C	Fig.	Min.	Typ.	Max.	Unit
Oscillator: CLK, CLKOUT									
501	f(CLK)	Permissible Clock Rate at CLK					20	25	MHz
502	f(CLKOUT)	Oscillator Clock Frequency	VDD = 5 V, CLKENI = 1				20		MHz
503	Vt(CLK)hi	Threshold Voltage hi						2	V
504	Vt(CLK)lo	Threshold Voltage lo				0.8			V
505	Vt(CLK)hys	Threshold Voltage Hysteresis				300	500		mV
506	Ipd()	Pull-Down Current at CLK	V() = 1.5 V ... VDD			4	35	70	µA
507	Vs()hi	Saturation Voltage hi at CLKOUT	Vs()hi = VDD- V(); I()= -4 mA					400	mV
508	Vs()lo	Saturation Voltage lo at CLKOUT	I()= 4 mA					420	mV
509	Isc()hi	Short-Circuit Current hi at CLKOUT	V() = 0			-30	-12	-4	mA
510	Isc()lo	Short-Circuit Current lo at CLKOUT	V() = VDD			5	23	50	mA
Reset: NRES									
601	VDDoff	Undervoltage Reset	VDD decreasing				1.6		V
602	VDDon	Undervoltage Release	VDD increasing				1.75		V
603	VDDhys	Undervoltage Hysteresis	VDDhys = VDDon - VDDoff				100		mV
604	Vt()hi	Threshold Voltage hi						2	V
605	Vt()lo	Threshold Voltage lo				0.8			V
606	Vt()hys	Threshold Voltage Hysteresis				300	500		mV
607	Ipd()	Pull-Down Current	V() = 1.5 V ... VDD			4	35	70	µA
608	td()res	Required Reset Pulse Duration at NRES				250			ns

OPERATING REQUIREMENTS: µC Interface, INTEL mode

Operating conditions: CFGSPI = 0, INT_NMOT = 1
VDD = 3 ... 5.5V, Ta = -25 ... 85 °C; input levels lo = 0 ... 0.45 V, hi = 2.4 V ... VDD

Item	Symbol	Parameter	Conditions	Fig.	Min.	Max.	Unit
I01	t_{sAA}	Setup Time: Address stable before ALE hi→lo		3/4	15		ns
I02	t_{Ah}	Signal Duration: ALE at high level		3/4	10		ns
I03	t_{sCA}	Setup Time: NCS hi→lo until ALE hi→lo		3/4	10		ns
I04	t_{hAA}	Hold Time: Address stable after ALE hi→lo		3/4	15		ns
I05	t_{sAW}	Setup Time: ALE hi→lo until NWR_E hi→lo		3	0		ns
I06	t_{WI}	Signal Duration: NWR_E at low level		3	10		ns
I07	t_{sDW}	Setup Time: Data stable before NWR_E lo→hi		3	15		ns
I08	t_{hWD}	Hold Time: Data stable after NWR_E lo→hi		3	0		ns
I09	t_{hWC}	Hold Time: NCS lo after NWR_E lo→hi		3	0		ns
I10	t_{hWA} t_{hRA}	Hold Time: ALE lo after NWR_E lo→hi	NCS = lo	3/4	15		ns
I11	t_{sAR}	Setup Time: ALE hi→lo until NRD_RNW hi→lo		4	0		ns
I12	t_{RI}	Signal Duration: NRD_RNW at low level		4	70		ns
I13	t_{pRD1}	Propagation Delay: Data stable after NRD_RNW hi→lo		4	0	25	ns
I14	t_{pRD2}	Propagation Delay: Data Bus high impedance after NRD_RNW lo→hi		4	0	25	ns

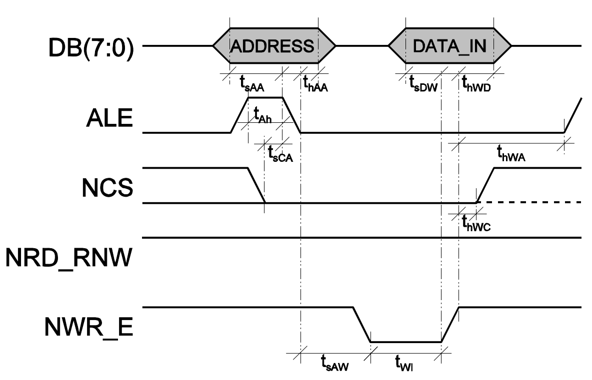


Figure 3: Write cycle (Intel Mode)

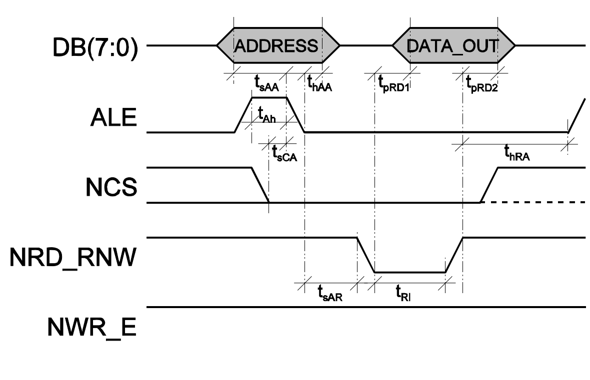


Figure 4: Read cycle (Intel Mode)

OPERATING REQUIREMENTS: µC Interface, MOTOROLA mode

Operating conditions: CFGSPI = 0, INT_NMOT = 0
VDD = 3 ... 5.5V, Ta = -25 ... 85 °C; input levels lo = 0 ... 0.45 V, hi = 2.4 V ... VDD

Item	Symbol	Parameter	Conditions	Fig.	Min.	Max.	Unit
I20	tsAA	Setup Time: Address stable before ALE hi→lo		5/6	15		ns
I21	tAh	Signal Duration: ALE at high level		5/6	10		ns
I22	tsCA	Setup Time: NCS hi→lo until ALE hi→lo		5/6	10		ns
I23	thAA	Hold Time: Address stable after ALE hi→lo		5/6	15		ns
I24	tsAE	Setup Time: ALE hi→lo until NWR_E lo→hi		5/6	0		ns
I25	tsRE	Setup Time: NRD_RNW lo→hi until NWR_E lo→hi		5/6	0		ns
I26	tEh	Signal Duration: NWR_E at high level		5/6	10		ns
I27	tsDE	Setup Time: Data stable before NWR_E hi→lo		5	15		ns
I28	thED	Hold Time: Data stable before NWR_E hi→lo		5	0		ns
I29	thEC	Hold Time: NCS lo after NWR_E hi→lo		5/6	0		ns
I30	thER	Hold Time: NRD_RNW lo after NWR_E hi→lo		5/6	0		ns
I31	tpED1	Propagation Delay: Data stable after NWR_E lo→hi		6	0	25	ns
I32	tpED2	Propagation Delay: Data bus high impedance after NWR_E hi→lo		6	0	25	ns
I33	thEA	Hold Time: NWR_E hi→lo before ALE lo→hi	NCS = lo	5/6	0		ns

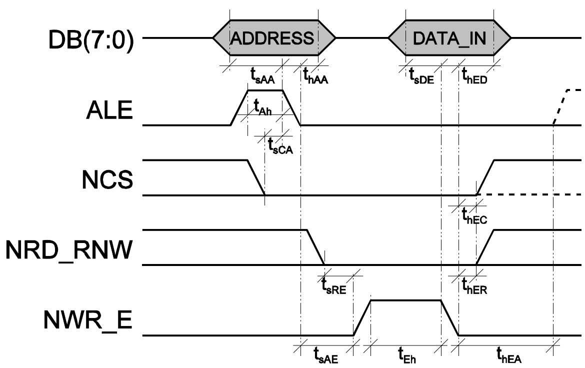


Figure 5: Write cycle (Motorola Mode)

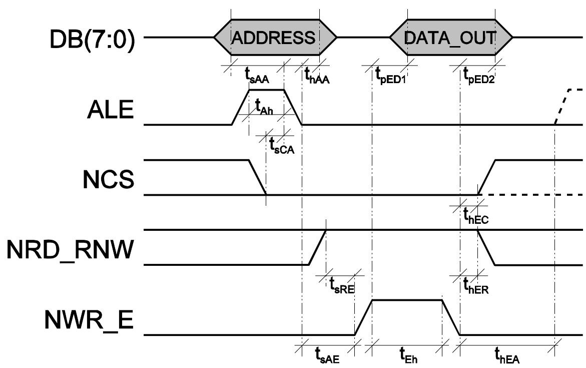


Figure 6: Read cycle (Motorola Mode)

OPERATING REQUIREMENTS: µC Interface, SPI mode

Operating conditions: CFGSPI = 1
VDD = 3 ... 5.5V, Ta = -25 ... 85 °C; input levels lo = 0 ... 0.45 V, hi = 2.4 V ... VDD

Item	Symbol	Parameter	Conditions	Fig.	Min.	Max.	Unit
I40	tsCCL	Setup Time: NCS hi→lo until SCLK/ALE lo→hi		0.29	10		ns
I41	tsDCL	Setup Time: SI/DB0 stable before SCLK/ALE lo→hi		0.29	15		ns
I42	thDCL	Hold Time: SI/DB0 stable after SCLK/ALE lo→hi		0.29	0		ns
I43	tCLh	Signal Duration SCLK/ALE hi		7a/b	10		ns
I44	tCLl	Signal Duration SCLK/ALE lo		7a/b	10		ns
I45	thCLC	Hold Time: NCS lo after SCLK/ALE lo→hi		7a/b	0		ns
I46	tCSh	Signal Duration NCS hi		7a/b	0		ns
I47	tpCLD	Propagation Delay: SO/DB1 stable after SCLK/ALE hi→lo		7b	0	25	ns
I48	tpCSD	Propagation Delay: SO/DB1 high impedance after NCS lo→hi		7b	0	25	ns

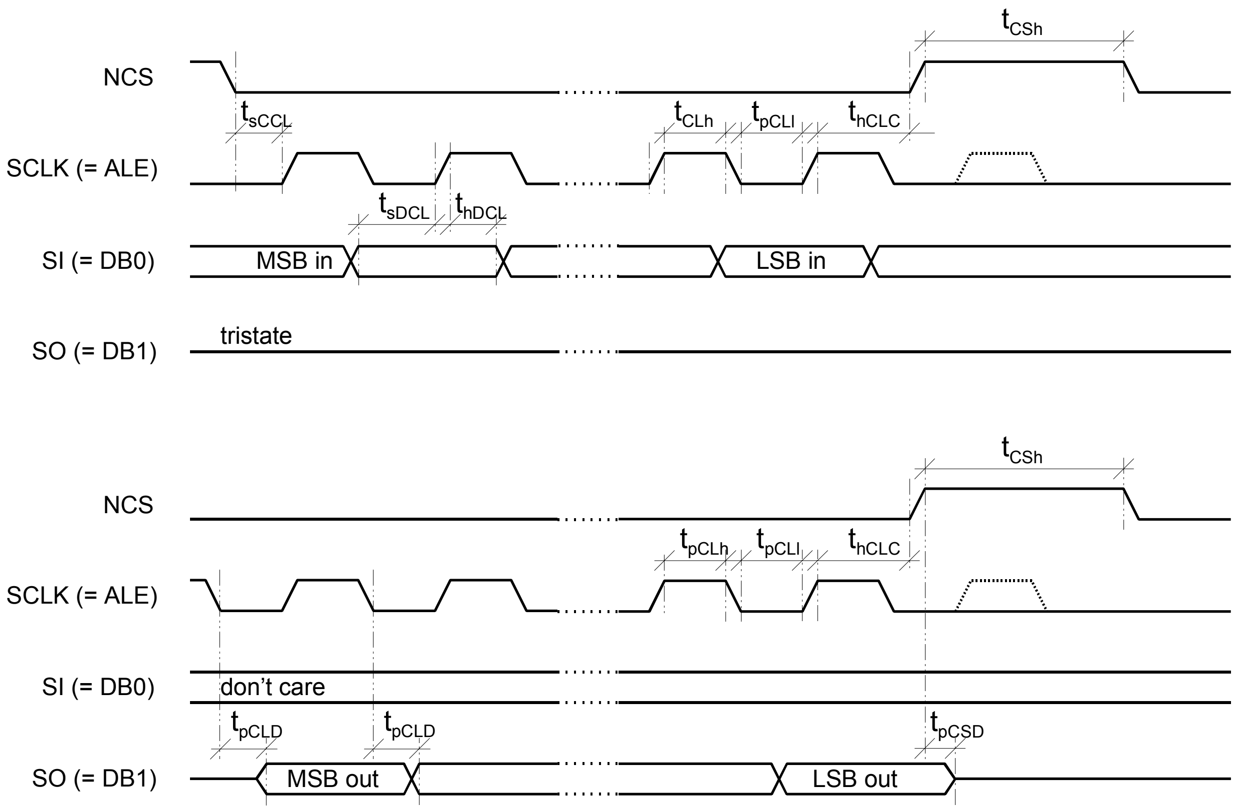


Figure 7: µC interface in SPI mode with write cycle (top) and read cycles (bottom).

OPERATING REQUIREMENTS: *BiSS Interface*

Operating conditions: Register bit SELSSI = 0
VDD = 3 ... 5.5 V, Ta = -25 ... 85 °C; input levels lo = 0 ... 0.45 V, hi = 2.4 V ... VDD

Item	Symbol	Parameter	Conditions	Fig.	Min.	Max.	Unit
Sensor Mode							
I60	TMAS	Clock Period	FreqSens via FREQ(4:0) selected in accordance with table on page 17	8	2	320	1/f(CLK)
I61	tMASl	Clock Signal Lo Level Duration		8	50		% TMAS
I62	tMASh	Clock Signal Hi Level Duration		8	50		% TMAS
I63	tpLine	Permissible Line Delay		8	0	indefinite	
I64	ΔtpL	Permissible Propagation Delay of Subsequent Clock Cycles vs. 1st Clock Cycle	ΔtpL = max(|tpLine - tpLx|); x= 1 ... n	8		25	% TMAS
I65	Ttos	Permissible Timeout (Slave)		8	55		% TMAS
Register Mode*							
I65	TMAR	Clock Period	FreqReg via FREQ(7:5) selected in accordance with table on page 17	9	2	256	TMAS
I66	tMA0h	"Logic 0" Hi Level Duration		9	25		% TMAR
I67	tMA1h	"Logic 1" Hi Level Duration		9	75		% TMAR
I68	tMAth	Clock Signal Hi Level Duration	register data readout	9	50		% TMAR
I69	tsSL	Setup Time: SL1 stable before MA1 lo→hi		9	30		ns
I70	thSL	Hold Time: SL1 stable before MA1 lo→hi		9	20		ns
I71	Ttor	Permissible Timeout (Slave)		9	80		% TMAR

*) For clocking to occur in register mode the slaves must have signaled that they are ready for register mode communication (see page 17).

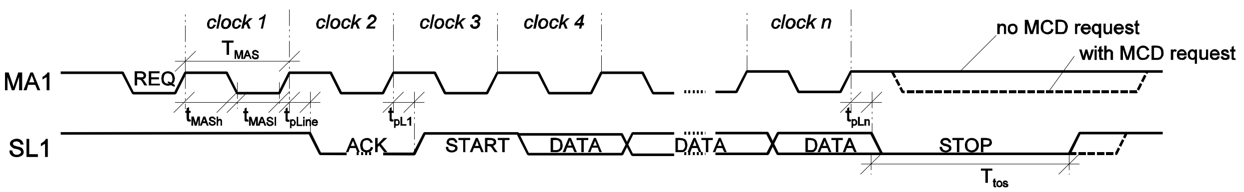


Figure 8: Timing diagram of sensor mode

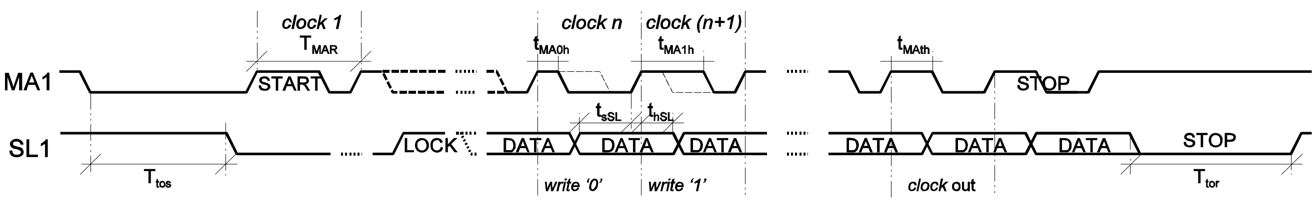


Figure 9: Timing diagram of register mode

Evaluating SL1 Signals

In *BiSS* mode delay times of longer than one clock cycle are permissible, with the result that line delays during communication are negligible. Evaluation of the sensor response is delayed until the first falling edge at SL1 while at MA1 the clock signal continues to be output.

Within one MA1 clock cycle four equally distributed sampling instances are available. Following the falling edge at SL1, the slave's acknowledge signal, the SL1 level is evaluated two sampling instances on, close to the center of the transmitted bit.

OPERATING REQUIREMENTS: *BiSS Interface* (SSI mode)

Operating conditions: Register bit SELSSI = 1;
VDD = 3 ... 5.5 V, Ta = -25 ... 85 °C; input levels lo = 0 ... 0.45 V, hi = 2.4 V ... VDD

Item	Symbol	Parameter	Conditions	Fig.	Min.	Max.	Unit
I80	TMAS	Clock Period	FreqSens über FREQ(4:0) selected in accordance with table on page 17	10	2	320	1/f(CLK)
I81	tMASh	Clock Signal Hi Level Duration		10	50		%TMAS
I82	tMASl	Clock Signal Lo Level Duration		10	50		%TMAS
I83	tsDC	Setup Time: SL1 stable before MA1 lo→hi		10	30		ns
I83	thDC	Hold Time: SL1 stable before MA1 lo→hi		10	10		ns

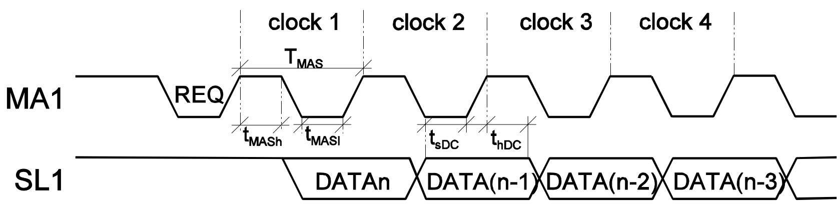


Figure 10: Timing diagram of SSI mode.

Evaluating SL1 Signals
In *BiSS* interface SSI mode SL1 values are sampled with the rising edge at MA1. An overall delay of the sensor response to the clock at MA1, caused by process times in the sensor or transmission times, is permissible up to the length of one clock cycle.

DESCRIPTION OF FUNCTIONS

iC-MB3 must be configured in accordance with the sensors connected to it; to this end a special area of memory has been included in the device. The other memory banks are used for the interim storage of incoming slave data or of slave data yet to be transmitted.

iC-MB3's second main component is its logic blocks which enable communication with the controller and generate the *BiSS* interface protocol on the slave side of the chip.

Microcontroller Interface

Via pins CFGSPI and INT_NMOT iC-MB3 can be configured for operation with an SPI-competent microcontroller, an Intel 8051 controller or a 68HC11 Motorola controller.

Here, 8-bit multiplex mode is used, in which the bidirectional data bus alternately transmits addresses and data in blocks of 8 bits (see Figures 3 to 6).

Communication Modes

CFGSPI	INT_NMOT	Mode
0	0	Motorola 68HC11
0	1	Intel 8051
1	-	SPI (polarity= 0, phase= 0)

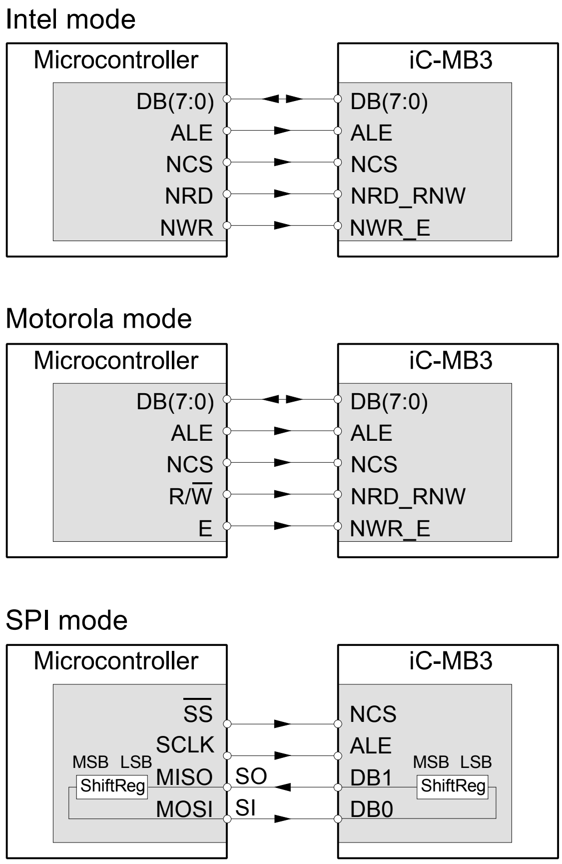


Figure 11: Wiring diagram for the microcontroller and iC- MB3.

When operated in conjunction with an SPI controller pin ALE is used as a clock input (SCK) and pin NCS as an enable input (NCS), with DB0 as the data input (SI) and DB1 as the data output (SO). Data is transmitted serially in successive blocks of 8 bits (command, address and data).

Four commands are available. These are WriteData (0000 0010b), ReadData (0000 0011b), ReadStatus (0000 0101b) and WriteInstruction (0000 0111b). The first two commands can be used to write data to or read data from iC-MB3's registers. The latter two commands are truncated write and read commands where the start address is fixed (namely that of the command register to address 244 and that of the status register to address 240). This means that it is not necessary to give an address, with the data directly adhering to the command.

With all commands it is possible to transmit several bytes of data consecutively if the NCS signal is not reset and ALE/SCK continues to be clocked. The address transmitted (240 for ReadStatus and 244 for WriteInstruction) is then the start address which is internally increased by 1 following each transmitted byte.

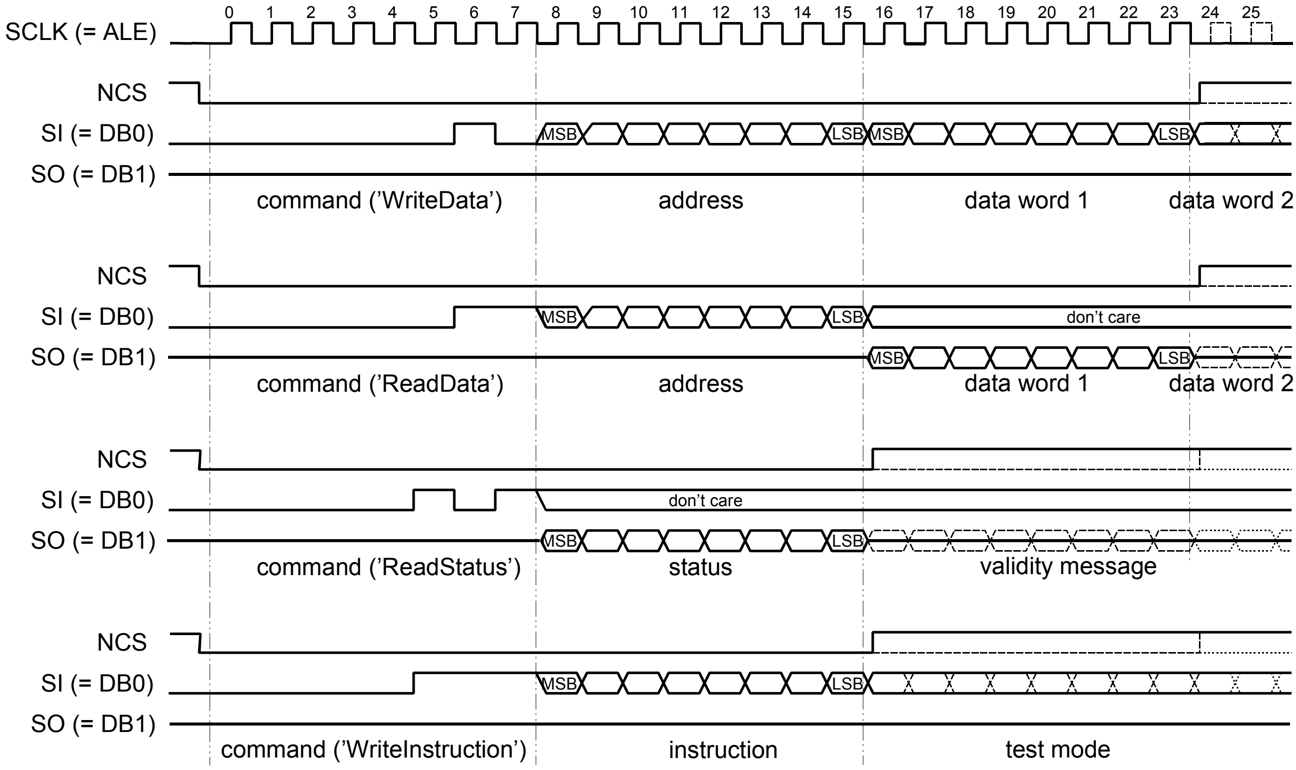


Figure 12: SPI transmission protocol (polarity 0, phase 0)

BiSS(SSI) Interface Configurations

Device Registers					
Address[1)]	Description				Dir.[2)]
00 ... 63	Sensor Data - 64 bits per Slave				in/out
	Slave 1 Addresses 07...00; lowest byte in Adr. 00	**Slave 2** Addresses 15...08; lowest byte in Adr. 08	**Slave 3** Addresses 23...16; lowest byte in Adr. 16	*Adr. 63...24 reserved for slaves 4...8*	
64 ... 127	Multicycle Data (MCD) - 64 bits per Slave				in/out
	Slave 1 Addresses 71...64; lowest byte in Adr. 64	**Slave 2** Addresses 79...72; lowest byte in Adr. 72	**Slave 3** Addresses 87...80; lowest byte in Adr. 80	*Adr. 127...88 reserved for slaves 4...8*	
128 ... 191	159 ... 128: Register Data (32 bytes) *191 ... 160: reserved for additional register data*				bidir
192 ... 223	Slave Configuration Data - 32 bits per Slave				in
	Slave 1 Addresses 195...192	**Slave 2** Addresses 199...196	**Slave 3** Addresses 203...200	*Adr. 223...204 reserved for slaves 4...8*	
224 ... 229	Configuration of Register Communication				in
230 ... 239	Configuration of Master				in
240 ... 255	Status information and command register				in/out

1) All addresses are decimals unless otherwise stated.
2) Direction
- in: Can only be written to by the µC
- out: Can be read out only by the µC
- in/out: Sections can be written to by the µC in part and only be read out in part
- bidir: Can be written to and read out by the µC

☐ Reserved address range for other master devices.

<table>
<tr><th colspan="11">Sensor Data, Multicycle Data and Slave Configuration</th></tr>
<tr><td colspan="3">Address</td><td colspan="8" rowspan="2">Description</td></tr>
<tr><td>SL1</td><td>SL2</td><td>SL3</td></tr>
<tr><td>07
...
00</td><td>15
...
08</td><td>23
...
16</td><td colspan="8">Sensor Data - SDATA(63...0)</td></tr>
<tr><td>71
...
64</td><td>79
...
72</td><td>87
...
80</td><td colspan="8">Multicycle Data - MCData(63...0)</td></tr>
<tr><td></td><td></td><td></td><td>Configuration</td><td>Bit 7</td><td>Bit 6</td><td>Bit 5</td><td>Bit 4</td><td>Bit 3</td><td>Bit 2</td><td>Bit 1</td><td>Bit 0</td></tr>
<tr><td>192</td><td>196</td><td>200</td><td>Sensor Data</td><td>ACTnSENS</td><td>ENSENS</td><td colspan="6">SDLEN(5:0)</td></tr>
<tr><td>193</td><td>197</td><td>201</td><td>Sensor CRC</td><td>INVCRCS</td><td colspan="7">SENSCRCPOLY(7:1)</td></tr>
<tr><td>194</td><td>198</td><td>202</td><td>Multicycle Data</td><td>GRAY</td><td>ENMCD</td><td colspan="6">MCDLEN(5:0)</td></tr>
<tr><td>195</td><td>199</td><td>203</td><td>MCD CRC</td><td>INVCRCM</td><td colspan="7">MCDCRCPOLY(7:1)</td></tr>
</table>

Key to the configuration bits:

- ACTnSENS — Access to slave data: Read (0), Write (1)
- ENSENS: — Adaptation to slave sensor data: available (1), not available (0)
- SDLEN: — Bit length of sensor data [1)]
- INVCRCS: — Transmission of CRC bits for sensor data: inverted (1), not inverted (0)
- SENSCRCPOLY: — CRC polynomial for verification of sensor data [2)]

- GRAY — Gray/binary data conversion of sensor and multicycle data: active (1, required with SSI encoders), not active (0)

- ENMCD: — Adaptation to slave multicycle data: available (1), not available (0)
- MCDLEN: — Bit length of multicycle data [1)]
- INVCRCM: — Transmission of CRC bits for multicycle data: inverted (1), not inverted (0)
- MCDCRCPOLY: — CRC polynomial for verification of multicycle data [2)]

1) The length of the data should be given minus 1, i.e. for 64 data bits enter 63.

2) If 0000 0000b is entered as the CRC polynomial, no cyclic redundancy check is carried out. As the last bit of a CRC polynomial is always 1 this is not entered in the polynomial register but added in the master. A CRC polynomial of up to 8 bits is thus possible. Should the full polynomial length not be required, the polynomial (minus its final 1) must be justified right and the spaces before it filled with zeros. For example, CRC polynomial 10 0011b is stored as 001 0001b.

Configuration Register Communication

Address	Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
224	Not used	-	-	-	-	-	-	-	-
225	Not used	-	-	-	-	-	-	-	-
226	Start Address	WNR	REGADR(6:0)						
227	Count Of Bytes	-	-	REGNUM(5)	REGNUM(4:0)				
228	Channel Select	CHSEL(8:1)							
229	SlaveID	-	REGVERS	SLAVEID(2:0)			-	-	-

Configuration Master

Address	Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
230	Frequency Division	FREQ(7:0)							
231	Not used	-	-	-	-	-	-	-	-
232	Frequency Division AutoGetsens	FREQAGS(7:0)							
233	Not used	-	-	-	-	-	-	-	-
Device ID									
234	Revision	0	0	0	0	0	0	0	1
235	Type	1000 0011b							
Configuration Channel									
236	Slave Location	SLAVELOC(8:1)							
237	Mode of Operation	SELSSI4	BiSSMOD4	SELSSI3	BiSSMOD3	SELSSI2	BiSSMOD2	SELSSI1	BiSSMOD1
238	Mode of Operation	SELSSI8	BiSSMOD8	SELSSI7	BiSSMOD7	SELSSI6	BiSSMOD6	SELSSI5	BiSSMOD5
239	Not used	-	-	-	-	-	-	-	-

Key to the configuration bits:
- SELSSI: Type of protocol: *BiSS* (0), SSI (1)
- BiSSMOD: *BiSS* protocol model: BiSS model A or B (0), BiSS-A/S (1)

Status Information and Command Register

Address	Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
240	Status Information	nERR	nWDERR	nMCDERR	nSENSERR	nREGERR	REGEND	MCDEND	EOT
241	Validity Messages 1,2)	SVALID4	MVALID4	SVALID3	MVALID3	SVALID2	MVALID2	SVALID1	MVALID1
242	Validity Messages 1,2)	SVALID8	MVALID8	SVALID7	MVALID7	SVALID6	MVALID6	SVALID5	MVALID5
243	Register Messages	MCD-TIMEOUT	REG 2, 4)	REG-BYTES(5)	REGBYTES(4:0)				
244	Command Register	BREAK	UCREAD-SENS	SWRAM-BANK	INIT	REGCMD	GETSENS0	GETSENS1	AGS
245	Control Flages	MAv0	MAf0	MAvS	MAfS	reserved	IDDQ 3)	IFTEST 3)	CLKENI
246	Not used	-	-	-	-	-	-	-	-
247	Not used	-	-	-	-	-	-	-	-
248	Channel Status	REG4	SL4	REG3	SL3	REG2	SL2	REG1	SL1
249	Channel Status	REG8	SL8	REG7	SL7	REG6	SL6	REG5	SL5
250	MCD bits 2)	MCD8	MCD7	MCD6	MCD5	MCD4	MCD3 2)	MCD2 2)	MCD1 2)
251...255	Not used	-	-	-	-	-	-	-	-

(shaded) Reserved addresses for master devices featuring a higher slave or channel count, or more memory for register data.
1) Any attempt to write to this register sets register values to 0.
2) Two memory banks available.
3) iC-Haus device test only, set to 0.
4) For iC-MB3 the register bit REG is equal to REG1.

Configuration - Master

Master Clock

The master clock, either generated by the basic clock of the internal 20 MHz oscillator (CLKENI = 1) or by an external clock oscillator (CLKENI = 0) which supplies pin CLK, is set with the aid of the frequency division register (address 230).

The clock frequency for both *BiSS* sensor and SSI modes is set via FREQ(4:0) in accordance with the table on the top right. With an external clock pulse of f_{CLK} = 20 MHz clock frequencies ranging from 62.5 kHz to 10 MHz can thus be selected for sensor data transmission.

Both *BiSS* and SSI devices recognize an idle bus at the end of a transmission cycle via a monoflop timeout elapsing (timeoutSENS, see *BiSS* protocol). The choice of possible clock frequency is thus limited as the duration of both the high and low level may not exceed the shortest timeout of all of the connected subscribers (slaves).

BiSS devices switch to register mode on recognizing that the bus is idle after a high-low transition at the clock input and signal this state back to the master on the data line.

The clock frequency in *BiSS* register mode is set via FREQ(7:5) and can lie within a range of ca. 244 Hz to 5 MHz. Here selection is also limited as with the above; a different monoflop timeout now recognizes the idle bus at the end of the cycle (timeoutREG, see *BiSS* protocol).

Additionally, *BiSS* devices generally only permit a lower clock frequency (such as 250 kHz maximum, for example) because the clock form has to be evaluated as a PWM signal.

Master Clock for *BiSS* Sensor Mode and SSI (FreqSens)

FREQ(3:0)	FREQ(4) = 0	FREQ(4) = 1
0	$f_{CLK}/2$	*not permitted*
1	$f_{CLK}/4$	$f_{CLK}/40$
2	$f_{CLK}/6$	$f_{CLK}/60$
3	$f_{CLK}/8$	$f_{CLK}/80$
4	$f_{CLK}/10$	$f_{CLK}/100$
5	$f_{CLK}/12$	$f_{CLK}/120$
6	$f_{CLK}14$	$f_{CLK}140$
7	$f_{CLK}/16$	$f_{CLK}/160$
8	$f_{CLK}/18$	$f_{CLK}/180$
9	$f_{CLK}/20$	$f_{CLK}/200$
10	$f_{CLK}/22$	$f_{CLK}/220$
11	$f_{CLK}/24$	$f_{CLK}/240$
12	$f_{CLK}/26$	$f_{CLK}/260$
13	$f_{CLK}/28$	$f_{CLK}/280$
14	$f_{CLK}/30$	$f_{CLK}/300$
15	$f_{CLK}/32$	$f_{CLK}/320$

A combination of FREQ(4) = 1 and FREQ(3:0) = 0 is not permitted; for a clock frequency of $f_{CLK}/20$ FREQ(4) = 0 and FREQ(3:0) = 9 must be set.

Master Clock for *BiSS* Register Mode (FreqReg)

FREQ(7:5)	FreqReg
0	FreqSens/2
1	FreqSens/4
2	FreqSens/8
3	FreqSens/16
4	FreqSens/32
5	FreqSens/64
6	FreqSens/128
7	FreqSens/256

Automatic request for sensor data

The frequency with which new requests for sensor data are sent to the slaves is set using FREQAGS according to the table on the right. With an external clock of 20 MHz sensor data request cycles ranging from 1 µs to 4 ms are possible.

FREQAGS must be set in such a way that the distance between two requests for data is greater than a complete cycle; this consists of the transmission of a request, an acknowledge signal (including any line delays), a start bit (including process times), a register bit (optional), the sensor, CRC and MCD bits of each slave and the longest sensor timeout of all the slaves.

Automatic Sensor Data Request (FreqAGS)

FREQAGS(6:0)	FREQAGS(7)= 0	FREQAGS(7)= 1
0	$f_{CLK}/20$	$f_{CLK}/625$
1	$f_{CLK}/40$	$f_{CLK}/1250$
2	$f_{CLK}/60$	$f_{CLK}/1875$
...	...	...
125	$f_{CLK}/2520$	$f_{CLK}/78750$
126	$f_{CLK}/2540$	$f_{CLK}/79375$
127	$f_{CLK}/2560$	$f_{CLK}/80000$

DATA STORAGE - Sensor and Multicycle Data

So that new sensor data can be read in during controller accesses iC-MB3 has dual memory banks for sensor and multicycle data. While sensor data is being read into the first RAM, from the second RAM section the controller can read out the sensor data last read in. The relevant sensor data memory banks are swapped over at the end of the readin procedure; this can be prevented by the controller entering the command register bit UCREADSENS. The MCD memory banks are swapped once a complete MCD cycle has been transmitted if at the same time bit MCDEND changes to a 1 in the status register. In parallel with this the validity message register (address 241) and the bits REG and MCD (addresses 248 to 250) are also swapped.

Arrangement of sensor and multicycle data in the RAM

The sensor or multicycle data memory bank for each slave has 8 bytes of memory which can be interpreted as 64 bits of memory in the array xxxxx111b to xxxxx000b. The sensor or multicycle data is written to memory area [SDLEN - 1:0] or [MCDLEN - 1:0], with SDLEN and MCDLEN marking the length of the relevant data. Should there be room in the available memory for the CRC bits, these are then also stored with the above data at positions [63:63 - (CRCLEN-1)].

Example Slave 2: 20 bits of sensor data, 6 bits of CRC => total length of 26 bits
13 bit of multicycle data, 5 bits of CRC => total length of 18 bits

Adr. 07 ... 00: Sensor data Slave 1
Adr. 15 ... 08: Sensor data Slave 2 -
Adr. 15: SensCRC(5:0), *not defined*, *not defined*
Adr. 14: *- not defined -*
Adr. 13: *- not defined -*
Adr. 12: *- not defined -*
Adr. 11: *- not defined -*
Adr. 10: *not defined*, *not defined*, *not defined*, *not defined*, SensData(19:16)
Adr. 9: SensData(15:8)
Adr. 8: SensData(7:0)
Adr. 23 ... 16: Sensor data Slave 3
...
Adr. 71 ... 64: Multicycle data Slave 1
Adr. 79 ... 72: Multicycle data Slave 2 -
Adr. 79: MCDCRC(4:0), *not defined*, *not defined*, *not defined*
Adr. 78: *- not defined -*
Adr. 77: *- not defined -*
Adr. 76: *- not defined -*
Adr. 75: *- not defined -*
Adr. 74: *- not defined -*
Adr. 73: *not defined*, *not defined*, *not defined*, MCD(12:8)
Adr. 72: MCD(7:0)
Adr. 87 ... 80: Multicycle data Slave 3
...

DATA STORAGE - register data

For the interim storage of register information read out from or to be written to the slaves iC-MB3 has an individual storage area (addresses 128 to 159) which can temporarily store up to 32 bytes of data. With just one single command this is then transmitted to a slave selected using SLAVEID(2:0) or requested from it as register data. The transmission of register data takes longer than that of sensor data so that the content of the sensor data and MCD RAM is then often obsolete.

STATUS INFORMATION and COMMAND REGISTER

Address 240: Status Messages			
Bit	Designation	Function	Remarks
7	nERR	An error has occurred (low active), equivalent to the pin level at NER (see "Error messaging" on page 22)	
6	nWDERR	Watchdog error (low active) on - transmissions triggered by an automatic sensor data request - transmissions of register data	1
5	nMCDERR	CRC error in the multicycle data (low active)	2
4	nSENSERR	CRC error in the sensor data (low active)	2
3	nREGERR	CRC error during the transmission of register data (low active)	3
2	REGEND	End of register data transmission	
1	MCDEND	End of multicycle data transmission (cycle completed)	
0	EOT	End of transmission: signals the end of sensor or register data transmission before timed out	

1. A watchdog error is triggered during the automatic transmission of sensor data if no new cycle could be initiated; bit AGS in the command register is reset and the automatic request for sensor data aborted. During the transmission of register data a watchdog error is triggered if the slave shows no response, i.e. if it does not answer the first falling master edge with a low or fails to generate a start bit.
2. If a sensor data or MCD error is signaled the faulty sensor can be verified by reading out address 241 (validity message).
3. If a register data error is generated the number of bytes transmitted correctly before the error occurred can be determined by reading out the register message REGBYTES (address 243, bits 5...0). In the event of error the transmission of data is terminated.

Address 241: Validity Messages			
Bit	Designation	Function	Remarks
7	MVALID4	Not used	1
6	SVALID4	Not used	1
5	MVALID3	Readout multicycle data from slave 3 valid	1
4	SVALID3	Readout sensor data from slave 3 valid	1
3	MVALID2	Readout multicycle data from slave 2 valid	1
2	SVALID2	Readout sensor data from slave 2 valid	1
1	MVALID1	Readout multicycle data from slave 1 valid	1
0	SVALID1	Readout sensor data from slave 1 valid	1

1. Any attempt to write to this register resets the validity messages.

Address 243: Register Messages			
Bit	Designation	Function	Remarks
7	MCDTIMEOUT	MCD timeout elapsed (1), not elapsed (0)	1
6	REG	Current register data bit at the slave operating on *BiSS* model C	2
5	REGBYTES(5)	Not used	
4...0	REGBYTES(4:0)	Number of register bytes transmitted correctly if an error occurs	3

1. A new request for multicycle data can only be made once the MCD timeout has elapsed; if a new MCD request is issued before this time the slaves operating on *BiSS* protocol model C will treat this as a register data transmission (see "Register communication in sensor mode").
2. During the data transmission in *BiSS* protocol model C format, where register data is transmitted together with sensor and multicycle data, the current register data bit in bit REG can be read out. Similar to the sensor data this bit also has a second storage section which allows the readout of bits transmitted during the last cycle while a new cycle is running. A swap occurs in parallel with that of the sensor data banks.
3. If no errors occur during transmission these bits are set to 0. Otherwise the number of register bytes successfully transmitted without error is displayed.

Address 244: Command Register			
Bit	Designation	Function	Remarks
7	BREAK	The current action is aborted (e.g. the clock at MA1 is stopped)	
6	UCREADSENS	RAM bank swapping is blocked	
5	SWRAMBANK	All RAM banks and the validity message register are forcibly swapped	
4	INIT	The sensor is initialized	
3	REGCMD	Executes transmissions of register data	
2	GETSENS0	Single request for sensor data with a high cycle termination (no refreshing of multicycle data)	
1	GETSENS1	Single request for sensor data with a low cycle termination (request to update multicycle data)	
0	AGS	Start of automatic sensor data requests (AutoGetSens)	

All bits with the exception of AGS, UCREADSENS and SWRAMBANK are independently deleted by the master once the command has been carried out.

All current actions can be aborted using the BREAK command so that a defined state can be resumed if one of the sensors proves faulty, for example.

During the readout of more than one sensor data register by the controller it is possible that the RAM banks in the master could be swapped over once a sensor data transmission is complete. So that the controller only reads related values bit UCREADSENS should be set at the start of the readout and returned at the end; this suppresses the RAM swap. With the start of a new sensor data cycle previous values are then overwritten by the new sensor data.

Each setting or deletion of bit SWRAMBANK forces the sensor data and MCD RAM banks to be swapped over. Data just input, for example, can then be read out if a cycle has ended during UCREADSENS = 1 (this is indicated by EOT in the status register switching to 1 during the suppression of the RAM swap).

The sensor chain can be initiated using the command INIT. A set REG bit starts the transmission of register data between iC-MB3 and a sensor.

The transmission of sensor data can be triggered via bits GETSENS0 and GETSENS1. In both instances a new transmission process is initiated; the difference between the two commands lies in how the transmission cycle is ended. With GETSENS0 the cycle finishes with a high; GETSENS1 ends on a low which also files a request for multicycle data. In this case the previous MCD cycle must have ended (MCDEND = 1) and the multicycle data timeout must have elapsed (MCDTIMEOUT = 1).

When initializing the sensor data transmission via GETSENS0 = 1 and GETSENS1 = 1, the cycle finishes with a level determined by the REG bit entered (Address 243, bit 6), i.e. for REG = 0 with a high or for REG = 1 with a low. By this function register data can be transmitted to slaves operating on the *BiSS* protocol model C principle in parallel to the transmission of sensor data (see "Transmission of register data in sensor mode").

To enable the synchronized data conversion of several slaves at once, all of which have differing wake-up times (power save mode), a sensor data cycle which initially wakes all of the slaves can be started by explicitly setting the GETSENS1 bit. Once the slaves have confirmed their state of readiness by sending an MCD start bit, setting GETSENS1 a second time (following the end of the MCD timeout) forces the synchronous storage of multicycle data in all slaves (see general notes on the *BiSS* protocol).

If an AGS bit has been set sensor data is read in cyclically according to the cycle frequency set in register 232 (FREQAGS) without any further commands being issued by the controller. As soon as all of the slaves connected have finished transmitting multicycle data (MCDEND = 1, MCDTIMEOUT = 1) a new request for multicycle data is started automatically.

Registers start address (REGADR, address 226), number of bytes (REGNUM, address 227) and slave ID (SLAVEID, address 229) stipulate from which slave register address onwards how many bytes are to be written to or read out from which specific slave. A byte count of 0 entered for REGNUM signals the transmission of a single register value; a 31 indicates the transmission of 32 register values. In the register REGBYTES (address 243) a 0 is entered if communication has proved error free. In the event of error the number of registers correctly read or written is displayed.

iC-MB3 does not support autonomous register communication as with *BiSS* model C, thus it is imperative that address 229's bit REGVERS remain set to 0.

Initialization
To initialize the bus subscribers and to allow them to find their position in the queue (and particularly so that the first slave recognizes its position as such) the master line must be set to 0 after a 1 period (longer than the longest sensor timeout). The slaves themselves signal that initialization has been successful with a 0 on line SL1.

During initialization internal counters and error flags in the master are deleted or set as appropriate. Should a slave prove faulty and not switch to 0 initialization must be aborted by a BREAK command.

Initialization ends when the MCD timeout flag is set (address 243); a request for multicycle data can thus be made in the next sensor data cycle.

Communication in sensor mode
The transmission of sensor data begins when at pin MA1 the master outputs the clock signal with the clock frequency selected by FREQ. The line delay, i.e. the transmission propagation until an acknowledgement is generated at SL1, is determined from the second falling edge onwards.

While the clock continues to be output at MA1 the master waits for the slaves' start bit (1) signaling the start of data transmission. Following this the actual clocking out of sensor data begins, i.e. the sensors place a new bit on the SL1 line with each rising edge on the MA1 line.

The sensor data being input into the master and the ensuing sets of CRC data are written to the appropriate sensor data RAM. At the same time the new CRC value is calculated in accordance with InvSensCRC and using the CRC polynomial stored in the configuration RAM. Should, after entry of the last CRC bit, the system ascertain that transmission was faulty the relevant validity message in address 241 is deleted and error message nSENSERR set in the status register at address 240. At the same time the sensor data RAM banks are swapped.

If the sensor is MCD competent the MCD bit following the sensor data CRC is stored in the appropriate position in the relevant RAM bank. If a CRC code is to be calculated this is done simultaneously – in accordance with InvMCDCRC and using the CRC polynomial stored in the configuration RAM – and also saved to the RAM. With the last multicycle data CRC bit read in the transmission is checked for errors; if any are determined the relevant validity message bit is deleted.

At the end of the sensor data cycle, when the last bit of the longest multicycle data from all the connected sensors has been read in, the terminated MCD transmission is signaled by flag MCDEND and the MCD RAM banks are swapped over. The controller can now read out the current MCD values.

Each sensor data cycle ending with a request for multicycle data resets the MCD timeout counter. Each cycle without an MCD request raises the counter by 1 until after 14 consecutive cycles the MCDTIMEOUT bit is set. This makes it possible to differentiate between an MCD request and a register bit sent by a slave operating on *BiSS* protocol model C (see "Register communication in sensor mode").

Communication in register mode
Once the slaves have signaled their readiness for register communication (SL1 = 0) the addressing sequence is compiled, consisting of a start bit (1), the slave ID, the register address, the write/read flag, the inverted CRC calculated from this and a stop bit (0). This sequence is then transmitted bit by bit.

At the same time the ID distribution among the slaves is checked; should none of the slaves react (should SL1 not signal a 1 after 9 clock pulses) communication is aborted and a register error message generated (nREGERR = 0). The same happens if the slave response is not 0 after the 17^{th} rising edge at MA1.

If a register value is to be transmitted to a slave transmission of the new register value begins after 17 clock pulses (i.e. following the transmission of the start bit, slave ID, register address, WNR, CRC and stop bit). This new register value consists of a start bit (1), the new contents of the register, the inverted CRC code and a stop bit (0). At the same time the slave response (SL1) is checked. If the slave does not send a start bit for any reason (if the register addressed does not exist, for example, or access to a write protected register is attempted) communication is aborted after 4,096 MA1 clock pulses and the message nWDERR generated; a register error (nREGERR = 0) is signaled if the CRC proves faulty.

If transmission has proved free of error further register values are then compiled as needed and transmitted until communication with the register has ended. If no errors have occurred during communication register 243 then has a value of 0; in the event of error this value is the number of bytes transmitted correctly.

When reading out a register value from a slave, following a correct addressing sequence (see above) the system waits while the clock pulse continues to be output at MA1 until the addressed slave sends a start bit. During this waiting period a slave can read out a connected EEPROM, for example, and then transmit this value to the master. Once the slave's start bit has been entered into the master the actual data bits are stored and the CRC carried out on the fly. This cyclic redundancy check operates with the fixed polynomial 10011b and with inverted CRC bits. Should a CRC error occur during transmission this is signaled by a register error; the number of register values transmitted without error is stored in register 243 and further communication aborted.

If no errors occur during the transmission of data the next register values can be transmitted from the slave to the master by continued clock pulses at MA1. Register 243 contains a 0 if transmission has proved error free.

At the end of communication in register mode the MCD timeout flag is set (address 243); a request for multicycle data can then be issued during the following sensor data cycle.

Error messaging

In sensor mode the validity of data is stored separately for each slave in the validity message register (address 241). In the event of error the appropriate validity message is deleted and nSENSERR or nMCDERR set to 0 in the status register. The error is signaled at pin NER.

In register mode a register error (nREGERR = 0) or a slave start signal missed for at least 4,096 MA1 clock pulses results in an error message at NER. As following initialization no valid sensor data yet exists all the bits in the validity message (address 241) are deleted; no display is generated at pin NER, however.

A watchdog error is triggered if during the automatic sensor data requests no new readout cycle was able to be initiated. In this instance bit AGS is reset in the command register and the cyclic sensor data requests aborted.

A watchdog error is also triggered if a slave response is lacking during the transmission of register data. This has two possible causes; either a slave does not respond to the first falling edge with a low or the slave fails to generate a start bit.

It is possible to connect other components to pin NER which can also generate an error message; this can then be read out via bit nERR in the status register at address 240.

Register communication in sensor mode
In the *BiSS* protocol (BiSS-A/S only) it is possible to send register data to or receive register data from a slave during a cyclic sensor data transmission.

In conjunction with *BiSS* master iC-MB3 the controller must arrange the ones and zeros necessary for the communication of register data overlaying the communication of sensor data by issuing or not issuing requests for multicycle data.

Register data is transmitted from the sensor to the *BiSS* master in a similar way to multicycle data, namely via a single bit transmitted in addition to the sensor data which is placed before the latter. The first bit received is treated as the register data bit if bit BiSSMOD in the MCD configuration register of the relevant slave (addresses 194, 198 or 202) has been set to 1.

The following GETSENSx commands are necessary for the transmission of register data and for requests for multicycle data (depending on MCDTIMEOUT settings):

GETSENS Functions

BiSSMOD	GETSENS Command	MCDTIMEOUT	Function
0 (model B)	GETSENS0	irrelevant	Start transmission of sensor data
	GETSENS1	0	Start transmission of sensor data; *not prudent here*, as in doing so the MCDTIMEOUT counter is reset
		1	Start transmission of sensor data, new request for multicycle data
1 (BiSS-A/S)	GETSENS0	0	Start transmission of sensor data, transmission of 0
		1	Start transmission of sensor data
	GETSENS1	0	Start transmission of sensor data, transmission of 1
		1	Start transmission of sensor data, new request for multicycle data

APPLICATION HINTS

Example system: iC-MB3 with two interpolators iC-NQ

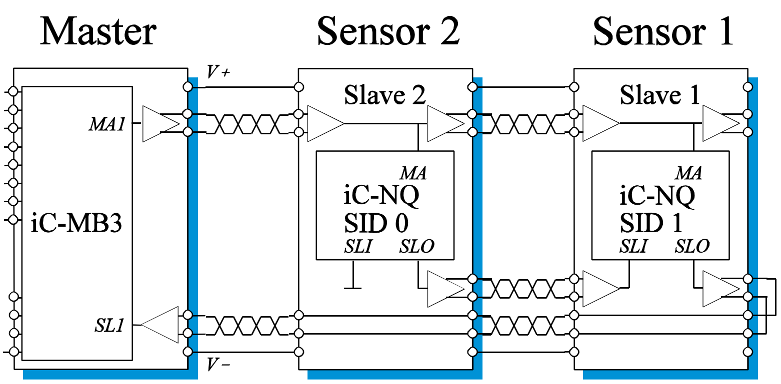


Figure 13: Example configuration

Sensor1:

```
<Manufacturer Code="6943">          -- iC-Haus GmbH
  <Device Code="4E5159300300">      -- iC-NQ RES=8192
    <Sens>
      <Length>15</Length>           -- 13 bit Sensordaten + Error1+ Error2
      <CrcPoly>0x25</CrcPoly>       -- Polynom '01001011'b
      <InvCrc>1</InvCrc>            -- CRC-Bits invertiert
    </Sens>
    <Mcd>
      <Length>24</Length>           -- 24 bit Periodenzähler (MCD)
      <CrcPoly>0x25</CrcPoly>       -- Polynom '01001011'b
      <InvCrc>1</InvCrc>            -- CRC-Bits invertiert
    </Mcd>
    <Reg>
      <IdUsed>1</IdUsed>            -- maximal 128 Register => eine Slave-ID
    </Reg>
  </Device>
</Manufacturer>
```

Sensor2:

```
<Manufacturer Code="6943">          -- iC-Haus GmbH
  <Device Code="4E5159302600">      -- iC-NQ RES=1024, Periodenzähler
    <Sens>
      <Length>20</Length>           -- 10 bit Sensordaten+ Error1 + Error2
                                       + 8 bit Periodenzähler
      <CrcPoly>0x25</CrcPoly>       -- Polynom '01001011'b
      <InvCrc>1</InvCrc>            -- CRC-Bits invertiert
    </Sens>
    <Mcd>
      <Length>16</Length>           -- 24 bit Periodenzähler, davon 16 bit als MCD
      <CrcPoly>0x25</CrcPoly>       -- Polynom '01001011'b
      <InvCrc>1</InvCrc>            -- CRC-Bits invertiert
    </Mcd>
    <Reg>
      <IdUsed>1</IdUsed>            -- maximal 128 Register => eine Slave-ID
    </Reg>
  </Device>
</Manufacturer>
```

Figure 14: Example *BiSS* device description file in XML

Assumptions:

Sensor 1: iC-NQ with 8,192 steps of resolution, a CRC polynomial 10 0101b and an inverted output, 24 bit period counter with a CRC polynomial 10 0101b and an inverted output; $Timeout_{SENS}$: 2,62 µs

Sensor 2: iC-NQ with 1,024 steps of resolution, a CRC polynomial 10 0101b and an inverted output, 24 bit period counter (8 bits of which are sent with the sensor data and 16 as MCD) with a CRC polynomial 10 0101b and an inverted output; $Timeout_{SENS}$: 2,62 µs

iC-MB3 clock: 20 MHz (according to the electrical characteristics in the data sheet)

Setting the master clock for sensor mode: max. 10 MHz => FREQ(4:0) = 00000b (10 MHz)
Setting the master clock for register mode: max. 250 kHz => FREQ(7:5) = 101b (156 kHz)

Setting the cycle time for the automatic sensor data request:
without transmission delays and processing times =>

cycle time = (3+ (15+6+1) + (20+6+1)) clock pulses +$Timeout_{SENS}$
= 52*0,1µs + 2,62µs = 7,82µs ≈156 * t_{CLK}

AutoGetSens time > cycle time => FREQAGS ≥ 7

Example system: Required configurations of iC-MB3

Configuration Master									
Address	Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
230	Frequency Division	1010 0000b							
232	Frequency Division AutoGetsens	0000 0111b							

Slave Configuration: Slave 1									
Address	Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
192	Sensor data	0	1	00 1110b					
193	Sensor-CRC	1	001 0010b						
194	Multicycle Data	0	1	01 0111b					
195	MCD-CRC	1	001 0010b						

Slave Configuration: Slave 2									
Address	Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
196	Sensor data	0	1	01 0011b					
197	Sensor-CRC	1	001 0010b						
198	Multicycle Data	0	1	00 1110b					
199	MCD-CRC	1	001 0010b						

Slave Configuration: Slave 3									
Address	Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
200	Sensor data	0	0	irrelevant					
201	Sensor-CRC	irrelevant							
202	Multicycle Data	0	0	irrelevant					
203	MCD-CRC	irrelevant							

ORDERING INFORMATION

Type	Package	Order designation
iC-MB3	TSSOP24 4.4 mm	iC-MB3 TSSOP24
Demo Board SPI Demo Board PAR		iC-MB3 EVAL MB3D-S iC-MB3 EVAL MB3D-P
BiSS PC-LPT Adapter BiSS PC-USB Adapter		Please refer to descriptions available separately.

For technical support, information about prices and terms of delivery please contact:

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