

iC-DL

3-CHANNEL DIFFERENTIAL LINE DRIVER

target specification



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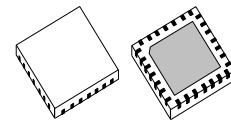
FEATURES

- ◆ 6 current-limited and short-circuit-proof push-pull drivers
- ◆ Differential 3-channel operation selectable
- ◆ Integrated impedance adaption for 30 to 140 Ω lines
- ◆ Wide power supply range from 4 to 40 V
- ◆ 200 mA output current (at $V_B = 24$ V)
- ◆ Low output saturation voltage (< 0.4 V at 30 mA)
- ◆ Compatible with TIA/EIA standard RS-422
- ◆ Tristate switching of outputs enables use in buses
- ◆ Short switching times and high slew rates
- ◆ Low static power dissipation
- ◆ Schmitt trigger inputs with pull-down resistors, TTL and CMOS compatible; voltage-proof up to 40 V
- ◆ Thermal shutdown with hysteresis
- ◆ Error message trigger input TNER
- ◆ Open-drain error output NER, active low with excessive chip temperature and undervoltage at VCC or VB
- ◆ Option: Extended temperature range from -40 to 125 $^{\circ}$ C

APPLICATIONS

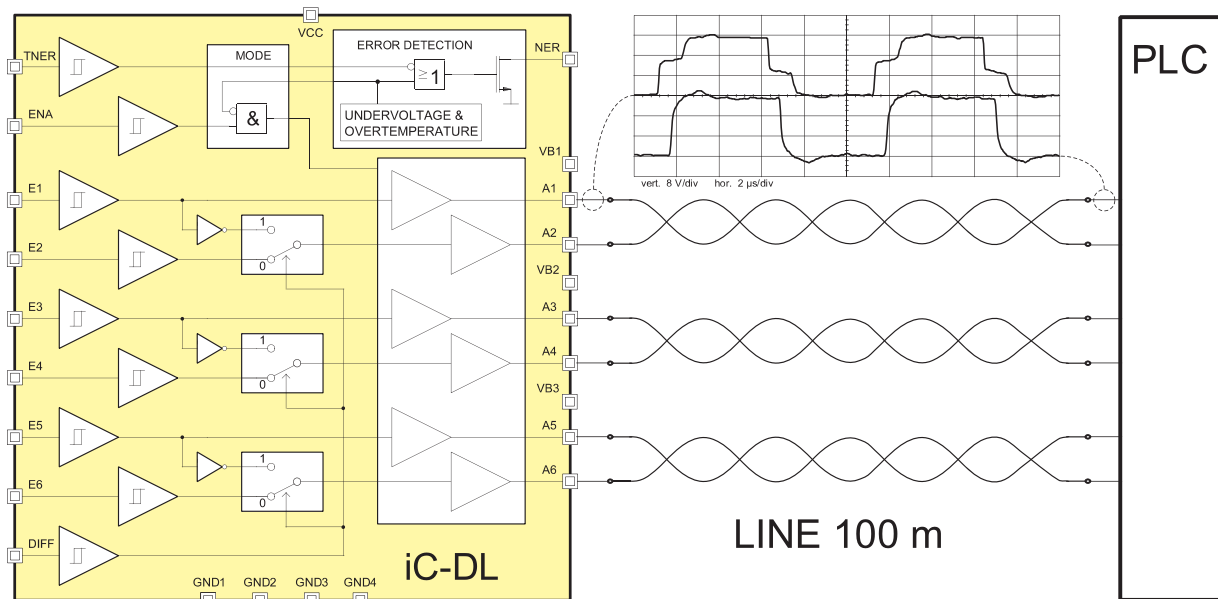
- ◆ Line drivers for 24 V control engineering
- ◆ Linear scales and encoders
- ◆ MR sensor systems

PACKAGES



QFN28 5 x 5 mm²

BLOCK DIAGRAM



iC-DL

3-CHANNEL DIFFERENTIAL LINE DRIVER

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DESCRIPTION

iC-DL is a fast line driver with six independent channels and integrated impedance adaptation for 30 to 140 Ω lines.

Channels are paired for differential 3-channel operation by a high signal at the DIFF input, providing differential output signals for the three inputs E1, E3 and E5. All inputs are compatible with CMOS and TTL levels.

The push-pull output stages have a driver power of typically 200 mA from 24V and are short-circuit-proof and current-limited, shutting down with excessive temperature. For bus applications the output stages can be switched to high impedance using input ENA.

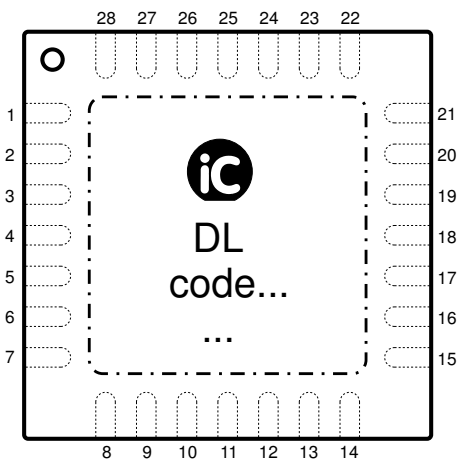
iC-DL monitors supply voltages VB and VCC and the chip temperature, switching all output stages to high impedance in the event of error and set NER active low. In addition, the device also monitors voltage differences at the pins VB1, VB2 and VB3 and generates an error signal if the absolute value exceeds 0.75 V.

The open-drain output NER allows the device to be wired-ORed to the relevant NER error outputs of other iC-DLs. Via input TNER the message outputs of other ICs can be extended to generate system error messages. NER switches to high impedance if supply voltage VCC ceases to be applied.

The device is protected against ESD.

PACKAGES QFN28 5 x 5 mm² JEDEC MO-220-VHHD-1

PIN CONFIGURATION QFN28 5 x 5 mm² (top view)



PIN FUNCTIONS

No. Name Function

1	E1	Input Channel 1
2	E2	Input Channel 2
3	E3	Input Channel 3
4	n.c.	
5	E4	Input Channel 4

PIN FUNCTIONS

No. Name Function

6	E5	Input Channel 5
7	E6	Input Channel 6
8	VCC	+5 V Supply
9	n.c.	
10	TNER	Error Input, low active
11	NER	Error Output, active low
12	A6	Output Channel 6
13	GND4	Ground
14	VB3	+4.5 ... 40 V Power Supply
15	A5	Output Channel 5
16	GND3	Ground
17	A4	Output Channel 4
18	VB2	+4.5 ... 40 V Power Supply
19	A3	Output Channel 3
20	GND2	Ground
21	A2	Output Channel 2
22	VB1	+4.5 ... 40 V Power Supply
23	GND1	Ground
24	A1	Output Channel 1
25	n.c.	
26	ENA	Enable Input, high active
27	n.c.	
28	DIFF	Differential Mode Input, high active

The pins VB1, VB2 and VB3 must be connected to the same driver supply voltage VB. The pins GND1, GND2, GND3 and GND4 must be connected to GND. To improve heat dissipation, the *thermal pad* at the bottom of the package should be joined to an extended copper area which must have GND potential.

ABSOLUTE MAXIMUM RATINGS

Beyond these values damage may occur; device operation is not guaranteed.

Item-No.	Symbol	Parameter	Conditions	Fig.	Limits		Unit
					Min.	Max.	
G001	VCC	Supply Voltage			0	7	V
G002	VBx	Driver Supply Voltage VB1, VB2, VB3			0	40	V
G003	V()	Voltage at E1...6, A1...6, DIFF, ENA, TNER			0	40	V
G004	I(Ax)	Driver Output Current (x=1...6)			-800	800	mA
G005	I(Ex)	Input Current Driver E1...E6, Diff, ENA, TNER			-4	4	mA
G006	V(NER)	Voltage at NER			0	50	V
G007	I(NER)	Current in NER			-4	25	mA
G008	V()	ESD Suceptibility at all pins	MIL-STD-883, Methode 3015, HBM 100 pF discharged through 1.5 kΩ			2	kV
G009	Tj	Operating Junction Temperature			-40	140	°C
G010	Ts	Storage Temperature Range			-40	150	°C

THERMAL DATA

Operating Conditions: VB = 4...40 V, VCC = 4...5.5 V

Item-No.	Symbol	Parameter	Conditions	Fig.	Limits			Unit
					Min.	Typ.	Max.	
T01	Ta	Operating Ambient Temperature Range (extended range to -40°C on request)			-25		125	°C
T02	Rthja	Thermal Resistance Chip to Ambient	surface mounted, <i>thermal pad</i> soldered to approx. 2 cm ² heat sink				40	K/W

All voltages are referenced to ground unless otherwise noted.

All currents into the device pins are positive; all currents out of the device pins are negative.

ELECTRICAL CHARACTERISTIC

Operating Conditions: $V_{B1...3} = 4...40\text{ V}$, $V_{CC} = 4...5.5\text{ V}$, $T_j = -40...140\text{ }^\circ\text{C}$, unless otherwise noted
 input level $I_o = 0...0.45\text{ V}$, $hi = 2.4\text{ V}...V_{CC}$, timing diagram see fig. 1

Item- No.	Symbol	Parameter	Conditions	Tj °C	Fig.				Unit	
						Min.	Typ.	Max.		
General										
001	VBx	Supply Voltage Range (Driver)				4		40		V
002	I(VBx)	Supply Current in VB1...3	A1...6 = lo					1.5		mA
003	I(VBx)	Supply Current in VB1...3	A1...6 = hi					3		mA
004	I(VBx)	Supply Current in VB1, Outputs A1...2 Tri-State	ENA = lo, $V(A1...2) = -0.3...(VB + 0.3\text{ V})$					1.2		mA
005	I(VBx)	Supply Current in VB2...3, Outputs A3...6 Tri-State	ENA = lo, $V(A2...6) = -0.3...(VB + 0.3\text{ V})$					1		mA
006	IO(Ax)	Output Leakage Current	ENA = lo, $V(Ax) = 0 \dots VB$			-20		20		µA
007	VCC	Supply Voltage Range (Logic)				4		5.5		V
008	I(VCC)	Supply Current in VCC	ENA = hi, Ax = lo				5	10		mA
009	I(VCC)	Supply Current in VCC	ENA = hi, Ax = hi				1.5	5		mA
010	Vc(lo)	Clamp Voltage low at pins VB1...3, A1...6, E1...6, DIFF, ENA TNER, NER, VCC	I() = -10 mA, all other pins open			-1.2		-0.4		V
011	Vc(hi)	Clamp Voltage high at Vcc	I() = 10 mA			5.6		7		V
012	Vc(hi)	Clamp Voltage high at pins VB1...3, A1...6, E1...6, DIFF, ENA TNER, NER, VCC	I() = 1 mA, all other pins open			45		64		V
013	I(VBx)	Supply Current in VB1...3	ENA = hi, $f(E1...6) = 1\text{ MHz}$				3	10		mA
Driver Outputs A1...6, Low-Side-action (x = 1...6)										
101	Vs(Ax)lo	Saturation Voltage low	I(Ax) = 10 mA, Ax = low					0.2		V
102	Vs(Ax)lo	Saturation Voltage low	I(Ax) = 30 mA, Ax = low					0.4		V
103	Isc(Ax)lo	Short circuit current low	$V(Ax) = 1.5\text{ V}$			40	60	90		mA
104	Isc(Ax)lo	Short circuit current low	$V(Ax) = VB$, Ax = low					800		mA
105	Rout(Ax)	Output resistance	$VB = 10...40\text{ V}$, $V(Ax) = 0.5 * VB$			40	75	100		Ω
106	SR(Ax)lo	Slew Rate low	$VB = 40\text{ V}$, $CI(Ax) = 100\text{ pF}$			200	600			V/µs
107	Vc(Ax)lo	Free Wheel Clamp Voltage low	I(Ax) = -100 mA			-1.3		-0.5		V
Driver Outputs A1...6, High-Side-action (x = 1...6)										
201	Vs(Ax)hi	Saturation Voltage high	$Vs(Ax)hi = VB - V(Ax)$, I(Ax) = -10 mA					0.2		V
202	Vs(Ax)hi	Saturation Voltage high	$Vs(Ax)hi = VB - V(Ax)$, I(Ax) = -30 mA, Ax = hi					0.4		V
203	Isc(Ax)hi	Short circuit current high	$V(Ax) = VB - 1.5\text{ V}$, Ax = hi			-90	-60	-40		mA
204	Isc(Ax)hi	Short circuit current high	$V(Ax) = 0\text{ V}$, Ax = hi			-800				mA
205	Rout(Ax)	Output resistance	$VB = 10...40\text{ V}$, $V(Ax) = 0.5 * VB$			40	75	100		Ω
206	SR(Ax)hi	Slew Rate high	$VB = 40\text{ V}$, $CI(Ax) = 100\text{ pF}$			200	400			V/µs
207	Vc(Ax)hi	Free Wheel Clamp Voltage high	I(Ax) = 100 mA, $VB = V_{CC} = GND$			0.5		1.3		V
Inputs E1...6, DIFF, ENA, TNER										
601	Vt(hi)	Threshold Voltage high						2		V
602	Vt(lo)	Threshold Voltage low				0.8				V
603	Vt(hys)	Input Hysteresis	$Vt(hys) = Vt(hi) - Vt(lo)$			200	400	800		mV
604	Ipd()	Pull-Down-Current	$V() = 0.8\text{ V}$			10		80		µA
605	Ipd()	Pull-Down-Current	$V() \leq 40\text{ V}$					160		µA
Supply Voltage Control VB										
701	VBon	Threshold Value at VB1 for Undervoltage Detection on (NER ⇒ low)	$ VB1 - VB2 \& VB2 - VB3 \& VB1 - VB3 < 0.75\text{ V}$					3.95		V
702	VBoff	Threshold Value at VB1 for Undervoltage Detection off (NER ⇒ high)	$ VB1 - VB2 \& VB2 - VB3 \& VB1 - VB3 < 0.75\text{ V}$			3				V

ELECTRICAL CHARACTERISTIC

Operating Conditions: $V_{B1...3} = 4...40V$, $V_{CC} = 4...5.5V$, $T_j = -40...140^\circ C$, unless otherwise noted
 input level $lo = 0...0.45V$, $hi = 2.4V...V_{CC}$, timing diagram see fig. 1

Item-No.	Symbol	Parameter	Conditions	Tj °C	Fig.				Unit	
						Min.	Typ.	Max.		
703	V_{Bhys}	Hysteresis	$V_{Bhys} = V_{Bon} - V_{Boff}$			150	250		mV	
Supply Voltage Difference Control VB1...3										
801	$\Delta V(V_{Bx})$	Threshold Condition for Supply Voltage Difference between V_{B1} , V_{B2} and V_{B3}	$\Delta V(V_{Bx}) = \text{MAX} (V_{B1} - V_{B2} , V_{B2} - V_{B3} , V_{B1} - V_{B3})$ NER \Rightarrow low					0.75	V	
Supply Voltage Control VCC										
901	V_{CCon}	Threshold Value at VCC for Undervoltage Detection on	NER \Rightarrow low					3.95	V	
902	V_{CCoff}	Threshold Value at VCC for Undervoltage Detection off	NER \Rightarrow high			3			V	
903	V_{CChys}	Hysteresis	$V_{CChys} = V_{CCon} - V_{CCoff}$			250	600		mV	
Temperatur Control										
A01	T_{off}	Thermal Shutdown Threshold				145		175	°C	
A02	T_{on}	Thermal Lock-on Threshold				130		165	°C	
A03	T_{hys}	Thermal Shutdown Hysteresis	$T_{hys} = T_{on} - T_{off}$				12		°C	
Error Output NER										
B01	$V_s()$	Saturation Voltage low at NER	$I(NER) = 5\text{ mA}$, NER = lo					0.4	V	
B02	$I_{sc}()$	Short Circuit Current low at NER	$V(NER) = 2...40V$, NER = lo				12	20	mA	
B03	$I_O()$	Leakage Current at NER	$V(NER) = 0V...V_B$, NER = hi			-10		10	µA	
B04	VCC	Supply Voltage for NER function	$I(NER) = 5\text{ mA}$, NER = lo, $V_s(NER) < 0.4V$			2.6			V	
Time Delays										
I01	$t_{plh}(E-A)$	Propagation Delay $E_x \Rightarrow A_x$	DIFF = lo, $C_I() = 100\text{ pF}$		1		100	400	ns	
I02	$t_{phi}(E-A)$	Propagation Delay $E_x \Rightarrow A_x$	DIFF = lo, $C_I() = 100\text{ pF}$		1		100	200	ns	
I03	$\Delta t_{plh}(A_x)$	Delay Skew $ A1 \Rightarrow A2 , A3 \Rightarrow A4 , A5 \Rightarrow A6 $	DIFF = hi, $C_I() = 100\text{ pF}$		1		30	100	ns	
I04	$\Delta t_{phi}(A_x)$	Delay Skew $ A1 \Rightarrow A2 , A3 \Rightarrow A4 , A5 \Rightarrow A6 $	DIFF = hi, $C_I() = 100\text{ pF}$		1		30	100	ns	
I05	$t_{plh}(ENA)$	Propagation Delay $ENA \Rightarrow A_x$	$E_x = hi$, DIFF = lo, $C_I() = 100\text{ pF}$, $R_I(A_x, GND) = 5\text{ k}\Omega$		1		130	300	ns	
I06	$t_{plh}(ENA)$	Propagation Delay $ENA \Rightarrow A_x$	$E_x = lo$, DIFF = lo, $C_I() = 100\text{ pF}$, $R_I(V_B, A_x) = 100\text{ k}\Omega$		1		100	200	ns	
I07	$t_{phi}(ENA)$	Propagation Delay $ENA \Rightarrow A_x$	$E_x = lo$, DIFF = lo, $R_I(V_B, A_x) = 5\text{ k}\Omega$		1		200	500	ns	
I08	$t_{phi}(ENA)$	Propagation Delay $ENA \Rightarrow A_x$	$E_x = hi$, DIFF = lo, $R_I(A_x, GND) = 5\text{ k}\Omega$		1		250	500	ns	
I09	$t_{phi}(DIFF)$	Propagation Delay DIFF $\Rightarrow A2, A4, A6$	$E1, E3, E5 = hi$, $C_I() = 100\text{ pF}$		1		100	250	ns	
I10	$t_{plh}(DIFF)$	Propagation Delay DIFF $\Rightarrow A2, A4, A6$	$E1, E3, E5 = lo$, $C_I() = 100\text{ pF}$		1		130	400	ns	
I11	$t_{plh}(TNER)$	Propagation Delay $TNER \Rightarrow NER$	$R_I(V_B, NER) = 5\text{ k}\Omega$, $C_I() = 100\text{ pF}$		1		0.5	2	µs	

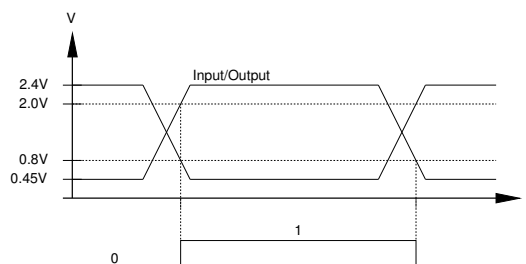


Figure 1: Reference levels for delays

DESCRIPTION

Line drivers for control engineering couple TTL- or CMOS-compatible digital signals with 24 V systems via cables. The maximum permissible signal frequency is dependent on the capacitive load of the outputs (cable length) or, more specifically, the power dissipation in iC-DL resulting from this. To avoid possible short circuiting the drivers are current-limited and shutdown with excessive temperature.

When the output is open the maximum output voltage corresponds to supply voltage V_B (with the exception of any saturation voltages). Figure 2 gives the typical DC output characteristic of a driver as a function of the load. The differential output resistance is typically 75Ω over a wide voltage range.

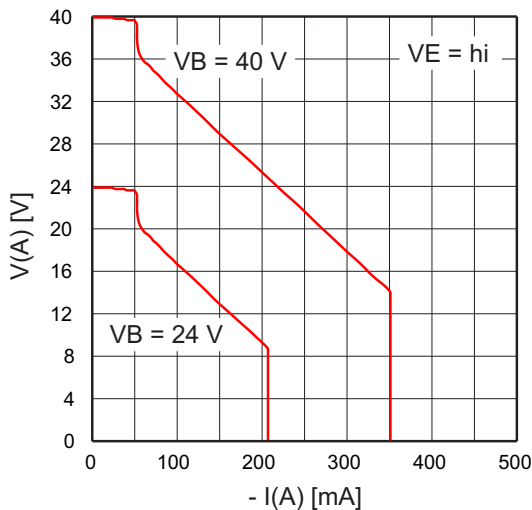


Figure 2: Load dependence of the output voltage (High-side stage)

Each open-circuited input is set to low by an internal pull-down current source; an additional connection to GND increases the device's immunity to interference. The inputs are TTL- and CMOS-compatible. Due to their high input voltage range, the inputs can also be set to high-level by applying VCC or V_B .

LINE EFFECTS

In PLC systems data transmission using 24 V signals usually occurs without a matched line termination. A mismatched line termination generates reflections which travel back and forth if there is also no line adaptation on the driver side of the device. With rapid pulse trains transmission is disrupted. In iC-DL, however, further reflection of back travelling signals is prevented by an integrated impedance network, as shown

in Figure 3.

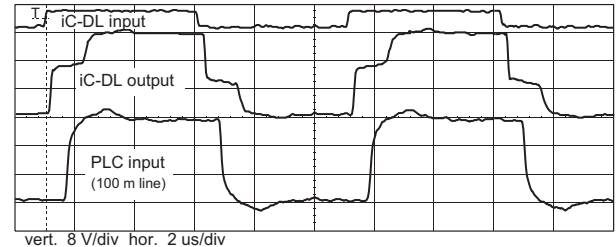


Figure 3: Reflections caused by a mismatched line termination

During a pulse transmission the amplitude at the iC-DL output initially only increases to half the value of supply voltage V_B as the internal driver resistance and characteristic line impedance form a voltage divider. A wave with this amplitude is coupled into the line and experiences after a delay a total reflection at the high-impedance end of the line. At this position, the reflected wave superimposes with the transmitted wave and generates a signal with the double wave amplitude at the receiving device.

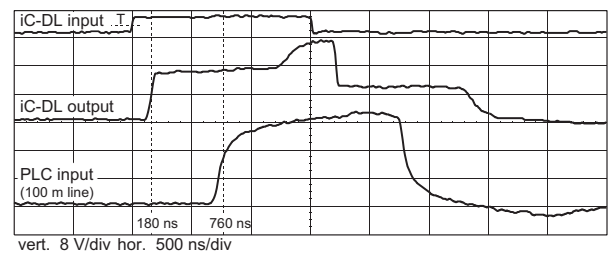


Figure 4: Pulse transmission and transit times

After a further delay, the reflected wave also increases the driver output to the full voltage swing. iC-DL's integrated impedance adapter prevents any further reflection and the achieved voltage is maintained along and at the termination of the line.

A mismatch between iC-DL and the transmission line influences the level of the signal wave first coupled into the line, resulting in reflections at the beginning of the line. The output signal may then have a number of graduations. Voltage peaks beyond V_B or below GND are capped by integrated diodes. By this way, transmission lines with a characteristic impedance between 30 and 140Ω permit proper operation.

iC-DL

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PRINTED CIRCUIT BOARD LAYOUT

The *thermal pad* at the bottom of the package improves thermal dissipation. The board layout has to be designed so that an appropriate number of copper vias below the thermal pad area form a good conductive path to the reverse of the board where a blank copper surface of sufficient size (approx. 2 cm²) carries off

heat. The *thermal pad* is to be soldered to the board and must be connected to GND.

To smooth the local IC supply VCC and VBx, blocking capacitors must be connected directly to these pins and to GND.

DEMO BOARD

iC-DL is in a QFN28 package and comes with a demo board for test purposes. Figures 5 and 6 show both

the wiring and the top of the demo board.

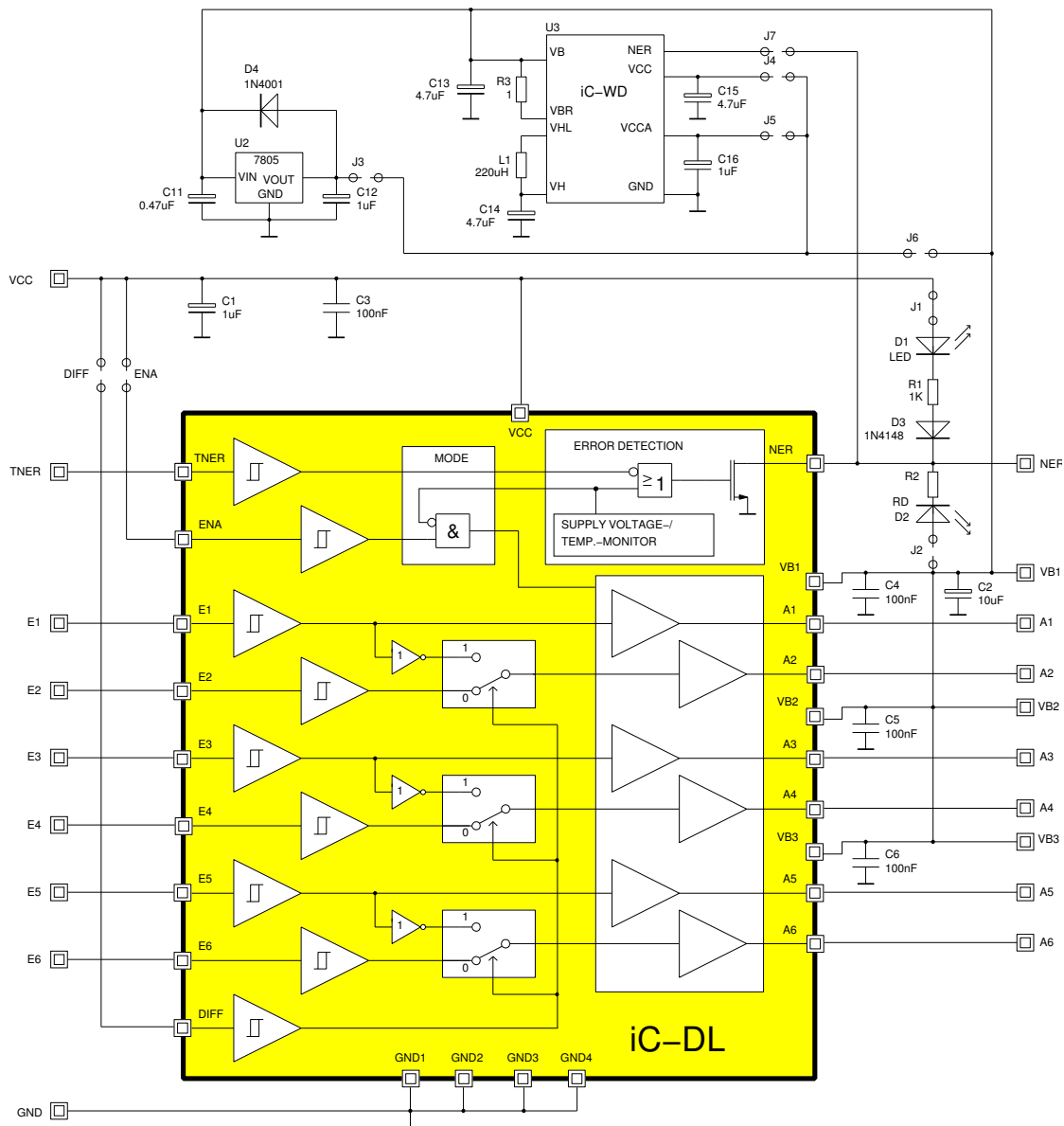


Figure 5: Circuit diagram of the demo board

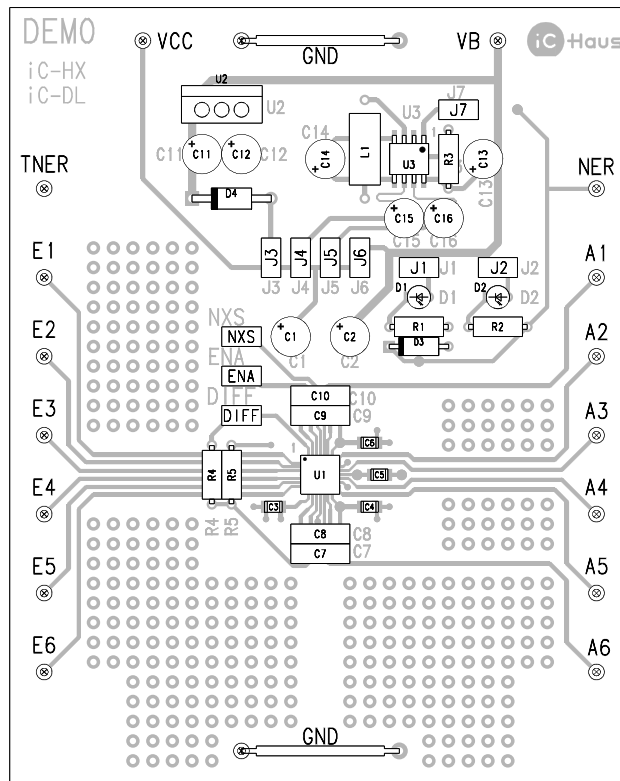


Figure 6: Demo board (component side)

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ORDERING INFORMATION

Type	Package	Order Designation
iC-DL	QFN28 5 x 5 mm ²	iC-DL QFN28
DL-Demo-Board		DL1D DEMO

For information about prices, terms of delivery, other packaging options etc. please contact:

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