Technical Specification
ATA Flash Memory Card
Full Size PCMCIA Card

Version 7.06

memorix elektronik

Introduction :

The FCA Series ATA Flash Card is a flash technology based, ATA interface, Type II PC Card using most advanced Flash ATA controller chips interfacing with Samsung or Hitachi NAND-based flash memory devices. The PC card operates from a single 3.5/5-Volt power supply and comes in capacity form 32MB up to 2048 MB unformatted. Emulating IDE hard disk drives and being fully compatible with PC Card ATA standard, it is a perfect choice of solid-state mass-storage cards for Palmtops, Notebooks, PC, PDA, or Digital Cameras equipped with PC Card sockets supporting ATA interface.

The Flash ATA PC Card is a low-power design with Flash technology's ruggedness, reliability, performance, and convenience. It uses surface-mount components. Non-recoverable error rate is less than 1 error per 10^{14} bit-reads. The Flash ATA card has no seek errors. Mean time between failure (MTBF) is an astonishing 4,000,000 hours. Its solid state construction requires no preventative maintenance.

Features:

- **PC Card compliant**
  - ◊ Fully compatible with PC Card standard and PC Card ATA
  - ◊ Backward compatible with PCMCIA 2.1
  - ◊ Support for CIS implemented with 256 bytes of attribute memory
  - ◊ Compatible with all PC Card Services and Socket Services

- **ATA/IDE interface**
  - ◊ ATA command set compatible
  - ◊ Support for 8- or 16-bit host transfers
  - ◊ Programmable and auto-wait-state generation for compatibility with any host speed using IORDY
  - ◊ Compatible with host ATA disk I/O BIOS, DOS/Windows file system, utilities, and application software

- **Extremely Rugged and reliable**
  - ◊ Solid-state reliability; Endurance: 2,000,000 Write/Erase cycles
  - ◊ 1000-G operating and non-operating shock. 15-G vibration
  - ◊ 4,000,000 power-on hours MTBF
  - ◊ Built-in 32-bit "on-the-fly" ECC

- **High performance**
  - ◊ Fast ATA host-to-buffer burst transfer rates up to 20 Mbytes/second
  - ◊ Supports PIO mode 4 and DMA mode 3, both at 16.6 Mbytes/second
  - ◊ Buffer transfer rates to and from flash memory up to 8 Mbytes/second

- **Support background erase operation**

- **Card capacity of 32, 48, 64, 96, 128, 256, 512, 1024, 2048 MByte available**

- **Single +3,5/+5 Volt power supply. Very low power consumption with automatic power management.**

- **Zero-power data retention, no batteries required**

Product Specifications :

Dimensions:
Type II card : 85.6mm(L) x 54mm(W) x 5mm(H)
Weight : 50 g or 1.8 oz

Storage Capacities: 32, 48, 64, 128, 256, 512, 1024, 2048 Mbytes (unformatted)

System Compatibility:
- Hewlett Packard 95/100/200LX
- Hewlett Packard OmniGo 100
- IBM compatible Notebook PCs, Laptops, Palmtops, or Hand-held devices, etc.

Performance:
Data Transfer Rates:

to/from Flash memory	up to 8 Mbytes/sec
to/from host	up to 20 Mbytes/sec
Command to DREQ	< 200 usec
Idle to Read	< 1 usec
Idle to Write	< 1 usec
Dual-port data buffer	2 Kbytes SRAM

Reliability:

MTBF	4,000,000 power-on hours
Error Rate	less than 1 bit error in 10^{14} bits read (min)
ECC	32-bit polynomial ECC supporting one random word of a sector "on-the-fly" ECC corrections

Ruggedness:
Shock, operating or non-operating 1000-G, any axis or direction Vibration, operating or non-operating 15-G peak to peak, 0.5 sine wave, 10 - 500 Hz, any axis or direction

Operating Voltage: 3.5 or 5V +/- 10%

Power consumption:

Read mode	65 mA (Max.)
Write mode	65 mA (Max.)
Idle mode	0,7 mA

Environment conditions:

Operating temperature	0°C to 55°C	-40°C to 85°C (Industrial Temp)
Storage temperature	-20°C to 65°C	
Relative humidit	95%(Max)	
Altitude	50,000 ft	

Agency Approvals:
CE, UL, VDE

Order Information

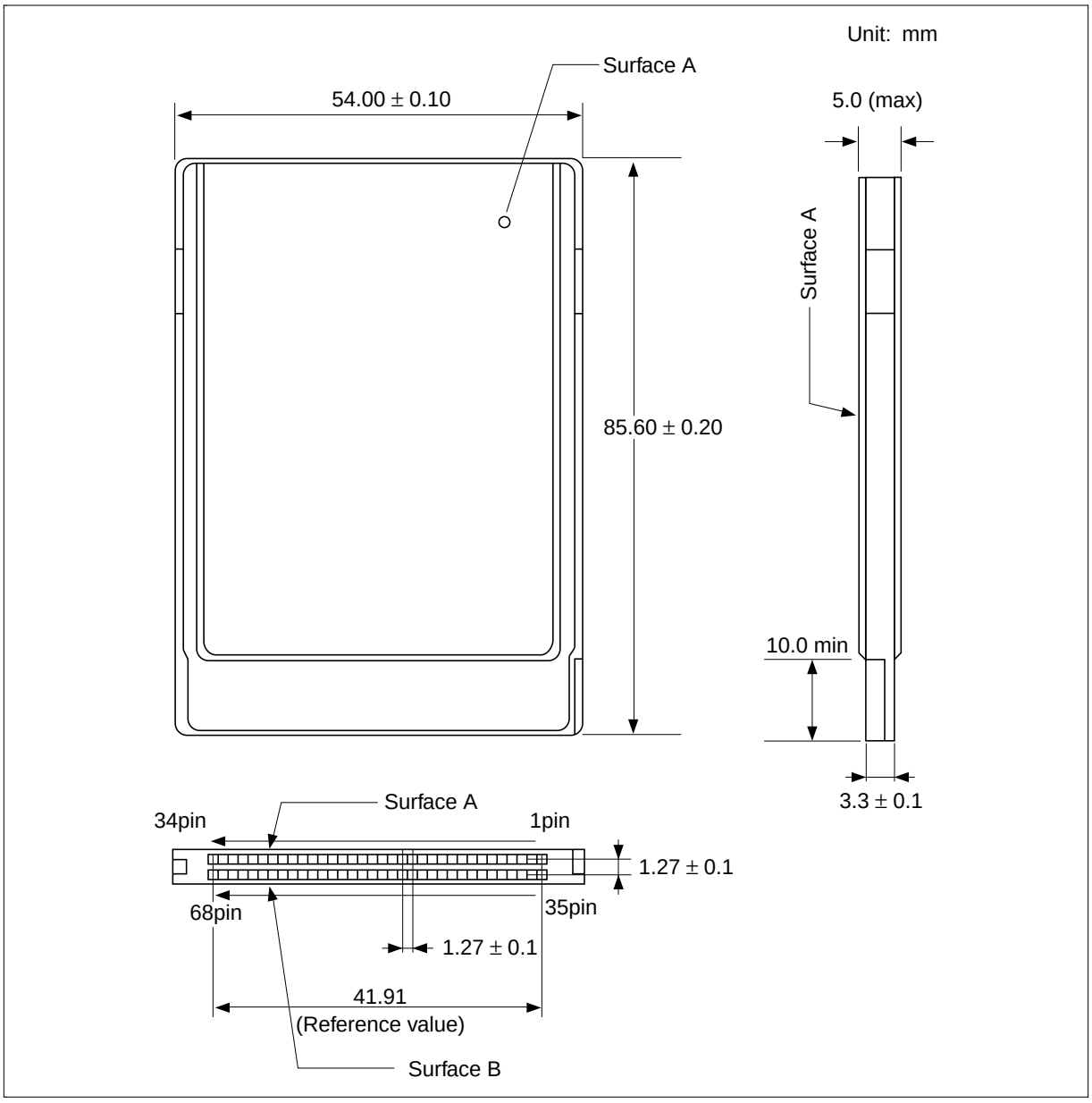
FCAxxxM-13Y-02

xxxx = Capacity
Y = C Standard Temp.
Y = I Industrial Temp.
Y = R Ruggedized Housing (full metal Housing, Industrial Temp)

Capacity	Order Code (Standard)	Order Code (Industrial)
32MB	FCA032M-13C-02	FCA032M-13I-02
64MB	FCA064M-13C-02	FCA064M-13I-02
96MB	FCA096M-13C-02	FCA096M-13I-02
128MB	FCA128M-13C-02	FCA128M-13I-02
256MB	FCA256M-13C-02	FCA256M-13I-02
512MB	FCA512M-13C-02	FCA512M-13I-02
1024MB	FCA001G-13C-02	FCA001G-13I-02
2048MB	FCA002G-13C-02	FCA002G-13I-02

Capacity	Order Code (Ruggedized)
32MB	FCA032M-13R-02
64MB	FCA064M-13R-02
96MB	FCA096M-13R-02
128MB	FCA128M-13R-02
256MB	FCA256M-13R-02
512MB	FCA512M-13R-02
1024MB	FCA001G-13R-02
2048MB	FCA002G-13R-02

Physical Outline



PCMCIA Interface :

The PCMCIA standard, originally created to standardize memory-card to personal-computer interface, now includes I/O devices. It defines signals, voltage levels, and socket- and card-cervices that control hardware. The PC Card-ATA Mass Storage Standard combines PC card interface requirements with the industry-standard ATA specification.

In addition to primary and secondary ATA addressing modes, PCMCIA specifies linear, independent I/O and linear memory-mapped modes. The PCMCIA-ATA specification goes beyond the ATA specification’s 16-bit-only data register and 8-bit-only task file register addressing protocol. It allows all ATA register accesses to be either 8- or 16-bits which allows a wide variety of system architectures to access PCMCIA-ATA drives.

Pin Assignments

PCMCIA-ATA memory and I/O mode pin descriptions

Pin	PCMCIA-ATA Memory Signal	PCMCIA-ATA I/O Signal	Notes
1	GND	GND	
2	D3	D3	
3	D4	D4	
4	D5	D5	
5	D6	D6	
6	D7	D7	
7	CE1#	CE1#	
8	A10	N.U.	2
9	OE#	N.U.	2
10	N.C.	N.C.	1
11	A9	A9	2
12	A8	A8	2
13	N.C.	N.C.	1
14	N.C.	N.C.	1
15	WE#	N.U.	2
16	RDY/BSY#	IREQ#	
17	VCC	VCC	
18	N.C.	N.C.	1
19	N.C.	N.C.	1
20	N.C.	N.C.	1
21	N.C.	N.C.	1
22	A7	A7	
23	A6	A6	
24	A5	A5	
25	A4	A4	
26	A3	A3	
27	A2	A2	
28	A1	A1	
29	A0	A0	
30	D0	D0	
31	D1	D1	
32	D2	D2	
33	WP	IOIS16#	2
34	GND	GND	

1 N.C. = Not connected internally

2 N.U. = Connected internally, but not used in mode

Pin	PCMCIA-ATA Memory Signal	PCMCIA-ATA I/O Signal	Notes
35	GND	GND	
36	CD1#	CD1#	
37	D11	D11	
38	D12	D12	
39	D13	D13	
40	D14	D14	
41	D15	D15	
42	CE2#	CE2#	
43	N.C.	N.C.	1
44	N.U.	IORD#	2
45	N.U.	IOWR#	2
46	N.C.	N.C.	1
47	N.C.	N.C.	1
48	N.C.	N.C.	1
49	N.C.	N.C.	1
50	N.C.	N.C.	1
51	VCC	VCC	
52	N.C.	N.C.	1
53	N.C.	N.C.	1
54	N.C.	N.C.	1
55	N.C.	N.C.	1
56	N.U.	N.U.	2
57	N.C.	N.C.	1
58	RESET	RESET	
59	WAIT#	WAIT#	
60	INPACK#	INPACK#	
61	REG#	REG#	
62	Pullup	Pullup	
63	Pullup	STSCHG#	
64	D8	D8	
65	D9	D9	
66	D10	D10	
67	CD2#	CD2#	
68	GND	GND	

1 N.C. = Not connected internally

2 N.U. = Connected internally, but not used in mode

Pin Descriptions

Symbol	Pin	Direction	Description

GND	1,34,35,68		Ground between the host and drive.
D0-15	2-6,30-32, 37-41,64-66	I/O	Bi-directional data bus between the host and drive.
CE1#	7	I	Card Enable 1 enables even data bytes on D0-7.
A0-25	8,10-14, 19-29, 46-50,53-56	I	Addresses A0-10 access data and registers depending on the memory or I/O mode chosen by the host. Addresses A11-24 are not used.
OE#	9	I	Output Enable reads attribute- and memory-mode data on D0-15.
WE#	15	I	Write Enable reads attribute- and memory-mode data on D0-15.
RDY/BSY#/	16	O	Indicates internally timed activities status. Drive can accept host accesses when high. In memory mode, RDY/BSY# does not reflect the ATA status register's BSY bit.
VCC	17,51	I	+5 Volt DC supply to the drive.
VPP1,VPP2	18,52	N.C.	+12 Volt DC programming supply is not required.
IOIS16#/WP	33	O	Held low after reset initialization (Write Protect is not supported).
CD1#,CD2#	36,67	O	Card Detect pins, internally pulled low, allow the host to determine that the drive is fully inserted in the socket.
CE2#	42	I	Card Enable 2 enables odd data bytes on D8-15.
RFSH#	43	N.C.	Not used.
IORD#	44	I	I/O Read gates data D0-15 during I/O-mode access.
IOWR#	45	I	I/O Write gates data D0-15 during I/O-mode access.
Reserved	57	N.C.	Reserved.
RESET	58	I	Active-high power-on or hardware reset signal resets drive registers.
WAIT#	59	O	Signals that an in-progress host memory or I/O cycle is not complete.
INPACK#	60	O	When selected, the drive asserts Input Acknowledge while responding to an I/O read cycle.
REG#	61	I	Common memory is accessed when high. Attribute memory and ATA registers are accessed when low.
BVD2	62	O	10K Pull-up to VCC.
BVD1/ STSCHG#	63	I/O	Notifies the host of RDY/BSY# and Write Protect state changes.

* Note All pin directions are referenced to drive

Card Configuration Registers

The table summarizes the drive's four PCMCIA configuration registers. These read/write one-byte

registers are located on even-byte attribute-plane addresses to ensure access in 8- and 16-bit system. Available card status information allows arbitration between resources that share interrupts and status of memory-only-card pins 16, 33, 62, and 63.

Register	Add. Offset[1]	R/W	REG#	CE2#	CE1#	OE#	WE#	D15-8	D7-0
Configuration Option	200h	Read	L	H	L	L	H	Invalid	Option
		Write	L	H	L	H	L	Invalid	Option
Card Configuration and Status	202h[2]	Read	L	H	L	L	H	Invalid	Status
		Write	L	H	L	H	L	Invalid	Config
Pin Replacement	202h[2]	Read	L	H	L	L	H	Invalid	Pin Status
		Write	L	H	L	H	L	Invalid	Pin Status
Socket and Copy	202h[2]	Read	L	H	L	L	H	Invalid	Socket ID
		Write	L	H	L	H	L	Invalid	Socket ID

Notes

1 The host obtains attribute-memory address offset from the Configuration Tuple's tpcc_radr field when it reads the drive's CIS.

2 Some engineering samples (marked ES) and early production units do not support these registers.

Configuration Option Register

The host uses the read/write Configuration Option register to configure the drive for drive for one of its four PCMCIA-ATA addressing modes, establish the interrupt signal mode, and issue a soft reset.

7	6	5	4	3	2	1	0
SRST	IRQLvl	Configuration Index					

SRST Resets the card when 1. When 0 (default) after a hardware or software reset or power-on, the card is unconfigured. A configuration occurs when a valid configuration index is written to bits 0-5.

IRQLvl Selects level mode interrupts when 1, pulse mode interrupts when 0 (default).

Conf IDX The host chooses an option from the card's configuration table entry tuples and writes that option's Configuration Index number into this field. When zero (default), the memory-only interface is chosen, I/O accesses are disabled.

Configuration & Status Register

The Configuration and Status register contains card condition information.

7	6	5	4	3	2	1	0
Chng	SigChg	Iois8	0	Audio	PwrDn	Intr	0

Chng The Change bit indicates that a Pin Replacement register bit was changed.

SigChg The host sets/resets the Signal Changed bit to enable/disable a state-change signal from the status register. When set and the drive is configured for I/O, Chng controls pin 63 and is called the Changed Status signal. This bit should be 0 (BVD1/STSCHG# held high when configured for I/O) if no state change signal is desired.

IOis8 Must be set if the host can only perform 8-bit I/O accesses.

Audio Audio is not supported.

PwrDn Setting PwrDn places the drive in sleep mode. Host-initiated ATA task-file-register commands can also invoke low-power modes.

Intr This bit represents the interrupt request's internal state. Its value is available whether or not interrupts are configured. It remains true until the initiating-interrupt request is serviced.

Pin Replacement Register

The Pin Replacement register provides card status information that is otherwise provided on memory-only interface pins 16, 33, 62, and 63. When written, bits 0-3 are masks for setting corresponding bits 4-7.

7	6	5	4	3	2	1	0
CBvd	CBvd	Crdy/ bsy#	CWP	RBvd	RBvd	Rrdy/ bsy#	RWP

CBvd1,2 Set when written, otherwise zero.

Crdy/bsy# Set when Rrdy/bsy# changes state or when written by the host.

CWP Zero unless set by the host.

RBvd1,2 Set unless cleared by the host.

Rrdy/bsy# Internal ready/busy# state when I/O mode uses RDY/BSY# pin for interrupt.

RWP Zero, since the flash drive has no write protect switch, unless set by the host.

Socket and Copy Register

The Socket and Copy register allows the drive to distinguish between similar drives at the same address. The flash drive does not support this feature.

7	6	5	4	3	2	1	0
0	Copy Number			Socket Number			

Copy # The twin-card option is not supported.

Socket # The socket number is ignored.

Memory and I/O Modes Decoding

Memory Mode Decoding

Memory mode allows hosts to access ATA registers within a 2-Kbyte contiguous memory space. The first 16 bytes contain ATA task-file registers. Offsets 400h-7FFh provide alternate ATA data register addresses. The host must decode memory addresses A_{11} and above to provide card-enables CE1# and CE2#. The drive decodes addresses $A_{0\text{-}10}$. The flash drive is in memory mode at power-on or card insertion or when the host writes configuration index value 00h to the card's Configuration Option register. Table 8 summarizes the memory-mode ATA task file registers.

Register	Offset
Data	000h
Error (read), Set Feature (write)	001h
Sector Count	002h
Sector Number	003h
Cylinder Low	004h
Cylinder High	005h
Drive/Head	006h
Status (read), Command (write)	007h

Register	Offset
Data Low (duplicate)	008h
Data High (duplicate)	009h
Not Used	00Ah-00Ch
Error (duplicate)	00Dh
Alternate Status (read)	00Eh
Drive Control (write)	
Drive Address	00Fh
Data (duplicate)	400h-7FFh

Table 8. Memory-mode Task-file Registers

8-bit-only hosts have trouble independently accessing the 16-bit data register's low and high bytes. Normally, an 8-bit host would access offset 000h for the low byte and 001h for the high byte. However, in ATA implementations, offset 001h is the error register. PCMCIA's PC Card ATA specification provides an alternate addressing scheme that solves this problem. The data register can be accessed at either offset 000h, 008h, 009h, or between offsets 400h-7FFh. The error register can be accesses at either offset 001h or 00Dh.

Offset 000h and 008h operate identically. In 8-bit mode (CE1# asserted, CE2# de-asserted, $A_0 = 0$), each 000h- or 008h- offset access presents sequential data bytes over $D_{0\text{-}7}$. The first access presents a data-word's low byte, the next access presents the word's high byte. Offset 000h accesses with CE1# de-asserted and CE2# asserted present Error register contents over $D_{8\text{-}15}$. In 16-bit mode (CE1# and CE2# asserted, A_0 = don't care), each offset 000h or 008h access presents sequential data words on $D_{0\text{-}15}$.

Offset 009h allows an 8-bit host to access the data register's high-byte over D0-7. The drive presents low-then-high bytes if a host repeatedly accesses offset 008h followed by 009h. The drive presents high-then-low bytes if a host repeatedly accesses offset 009h followed by 008h. Sequential high-byte access at 009h are not supported.

Even-memory byte accesses (CE1# asserted, CE2# de-asserted, $A_0 = 0$), at offsets between 400h and 4FFh are equivalent to offset 008h accesses. Odd-memory word accesses (CE1# asserted, CE2# de-asserted, $A_0 = 1$), at these offsets are equivalent to offset 009h accesses. Even-memory word accesses (CE1# and CE2# asserted, A_0 = don't care), at these offsets are equivalent to offset 000h or 008h word accesses.

Offsets 400h-7FFh do not correspond to actual card data-buffer addresses. Each access within this offset-range presents a new data byte or word from the data buffer's FIFO. This data-register aliasing allows host CPUs to perform memory string-move operations. In a read-from-drive example, the host can set a source pointer that corresponds to drive-offset 400h and a destination pointer that corresponds to internal RAM memory. A move-string instruction then transfers data from the source (flash drive) to RAM as it automatically increments source and destination pointers. Although the source pointer increments from 400h to 7FFh offsets, the drive internally accesses only the data register.

PCMCIA's PC Card standard describes other task file register accesses in the common memory plane. Truth table 9 shows the PCMCIA-ATA independent memory address mode.

Table 9. PCMCIA-ATA MODE Independent Memory address = 000-00F, 400-7FF[2]

Function	ADDR	R/W	REG#	CE2#	CE1#	OE#	WE#	IORD#	IOWR#	D_{15-8}	D_{7-0}
No Operation	X[1]		X	H	H	X	X	X	X	High-Z	High-Z
Data (see note 3)	000	Read	H	L	L	L	H	H	H	Data High	Data Low
			H	H	L	L	H	H	H	Invalid	Data
		Write	H	L	L	H	L	H	H	Data High	Data Low
			H	H	L	H	L	H	H	Invalid	Data
Error	001	Read	H	H	L	L	H	H	H	Invalid	Error
			H	L	H	L	H	H	H	Error	Invalid
Set Feature		Write	H	H	L	H	L	H	H	Invalid	Feature
			H	L	H	H	L	H	H	Feature	Invalid
Sector Count	002	Read	H	X	L	L	H	H	H	Invalid	Sect. Cnt.
		Write	H	X	L	H	L	H	H	Invalid	Sect. Cnt.
Sector Number	003	Read	H	H	L	L	H	H	H	Invalid	Sect. No.
			H	L	H	L	H	H	H	Sect. No.	Invalid
		Write	H	H	L	H	L	H	H	Invalid	Sect. No.
			H	L	H	H	L	H	H	Sect. No.	Invalid
Cylinder Low	004	Read	H	X	L	L	H	H	H	Invalid	Cyl. Low
		Write	H	X	L	H	L	H	H	Invalid	Cyl. Low
Cylinder High	005	Read	H	H	L	L	H	H	H	Invalid	Cyl. High
			H	L	H	L	H	H	H	Cyl. High	Invalid
		Write	H	H	L	H	L	H	H	Invalid	Cyl. High
			H	L	H	H	L	H	H	Cyl. High	Invalid

Drive/Head	006	Read	H	X	L	L	H	H	H	Invalid	Drv/Hd
		Write	H	X	L	H	L	H	H	Invalid	Drv/Hd
Status	007	Read	H	L	L	L	H	H	H	Invalid	Status
			H	H	H	L	H	H	H	Status	Invalid
Command		Write	H	L	L	H	L	H	H	Invalid	Command
			H	H	H	H	L	H	H	Command	Invalid
Data (duplicate) (see note 3)	008	Read	H	L	L	L	H	H	H	Data High	Data Low
			H	H	L	L	H	H	H	Invalid	Data
		Write	H	L	L	H	L	H	H	Data High	Data Low
			H	H	L	H	L	H	H	Invalid	Data
	009	Read	H	H	L	L	H	H	H	Invalid	Data High
			H	L	H	L	H	H	H	Data High	Invalid
		Write	H	H	L	H	L	H	H	Invalid	Data High
			H	L	H	H	L	H	H	Data High	Invalid
Invalid	00A-00C		H	X	X	X	H	X	X	Invalid	Invalid
Error (duplicate)	00D	Read	H	H	L	L	H	H	H	Invalid	Error
			H	L	H	L	H	H	H	Error	Invalid
		Write	H	H	L	H	L	H	H	Invalid	Feature
			H	L	H	H	L	H	H	Feature	Invalid
Alternate Status	00E	Read	H	X	L	L	H	H	H	Invalid	Alt. Status
Drive Control		Write	H	X	L	H	L	H	H	Invalid	Control
Drive Address	00F	Read	H	H	L	L	H	H	H	Invalid	Drv. Add.
			H	L	H	L	H	H	H	Drv. Add	Invalid
		Write	H	H	L	H	L	H	H	Invalid	Not Used
			H	L	H	H	L	H	H	Not Used	Invalid
Data (duplicate) (see note 3)	400-7FF	Read	H	L	L	L	H	H	H	Data High	Data Low
		Write	H	L	L	H	L	H	H	Data High	Data Low

1 X = don't care

2 The host must must decode addresses All and above to provide card enables CE1# and CE2# that place the drive on a 2-K byte Boundary The drive decodes A0-10

3 In independent memory mode, each byte access to 000, 008, or even addresses 400-7FE presents a new data-buffer byte on Do-7 starting with the first buffer word's low byte Each word access presents sequential data buffer words on D0-15 Byte access to 009 or odd addresses401-7FF present high byte buffer data on D0-7 or D8-15 depending on CDE1# and CE2#

ATA Compliant Commands

Check Power Mode

Although this command is supported for backward compatibility, it has no actual function. The card will always return the Not In Standby mode code "00h" in the Sector Count register, in response to this command. Command completion status will always indicate command completed with no error.

Check Power Mode Command Issued by Host								
Task File Register	7	6	5	4	3	2	1	0
COMMAND	98h/E5h							
DRIVE/HEAD	nu	nu	nu	D	nu			
CYLINDER HI	nu							
CYLINDER LOW	nu							
SECTOR START	nu							
SECTOR COUNT	nu							
FEATURES	nu							

Command Block specified	upon completion/termination of Check Power Mode command (98h/E5h)							
Task File Register	7	6	5	4	3	2	1	0
	BSY	DRDY	DWF	DSC	DRQ	CORR	IDX	ERR
STATUS	0	1	0	1	V	V	0	0
DRIVE/HEAD	na	na	na	na	na			
CYLINDER HI	na							
CYLINDER LOW	na							
SECTOR	na							
SECTOR COUNT	Power Mode Code. Will always be 00							
	BBK	UNC	MC	IDNF	MCR	ABRT	TK0NF	AMNF
ERROR	0	0	0	0	0	0	0	0

Execute Drive Diagnostic

This command performs self-diagnostics on various internal components of the card. Results of the test are reported in the Error Register. Note that the bit definitions for the Error Register do not apply in this command; rather, the value in the Error Register is a diagnostic code, defined in Table 1 below.

Execute Drive Diagnostics Command Issued by Host								
Task File Register	7	6	5	4	3	2	1	0
COMMAND	90h							
DRIVE/HEAD	nu	nu	nu	D	nu			
CYLINDER HI	nu							
CYLINDER LOW	nu							
SECTOR START	nu							
SECTOR COUNT	nu							
FEATURES	nu							

Command Block specified upon completion/termination of Execute Drive Diagnostics command (90h)								
Task File Register	7	6	5	4	3	2	1	0
	BSY	DRDY	DWF	DSC	DRQ	CORR	IDX	ERR
STATUS	0	1	0	1	V	V	0	V
DRIVE/HEAD	na	na	na	na	na			
CYLINDER HI	na							
CYLINDER LOW	na							
SECTOR	na							
SECTOR COUNT	na							
ERROR	Diagnostic Code. See Table 1 below							

Table 1. Execute Drive Diagnostic Return Codes

Code	Description
01h	No error detected
02h	Formatter device error
03h	Sector buffer error
04h	ECC logic error
05h	Controller microprocessor error

Format Track

This command erases 32 sectors starting at the sector specified by the Cylinder, Head, and Sector Number parameters in the task file. If the sector is not valid, an IDNF (ID Not Found)) bit is set in the Error Register and the command terminates.
In CHS mode, the number of sectors to format per track will be set to the number of Current Sectors per Track in the Identify Drive data, by default 20h. Otherwise, it will be set to the number of sectors per track as set by an Initialize Drive Parameters command. must be the same as the actual number of sectors per track reported .
In LBA mode, the number of sectors to format per track is specified by the Host in the Sector Count register. The sector count must be set to 20h, otherwise the command will be aborted.
For backward compatibility, the card accepts one sector of data from the host . This data is not used. The "Erase" function is then called to erase the sectors indicated by this command (and any other sectors also marked "Old" by any previous operation).

Format Track Command Issued by Host								
Task File Register	7	6	5	4	3	2	1	0
COMMAND	50h							
DRIVE/HEAD	nu	L	nu	D	H[3:0] or LBA[27:24] of the starting sector/LBA			
CYLINDER HI	Cylinder[15:8] or LBA[23:16] of the first sector/LBA to transfer							
CYLINDER LOW	Cylinder[7:0] or LBA[15:8] of the first sector/LBA to transfer							
SECTOR START	[LBA mode only] LBA[7:0] of the first sector/LBA to transfer							
SECTOR COUNT	[LBA mode only] The number of sectors to be formatted on the track. Must be set to 20h							
FEATURES	nu							

Command Block specified upon completion/termination of Format Track command (50h)								
Task File Register	7	6	5	4	3	2	1	0
	BSY	DRDY	DWF	DSC	DRQ	CORR	IDX	ERR
STATUS	0	1	0	1	V	V	0	V
DRIVE/HEAD	na	na	na	na	na			
CYLINDER HI	na							
CYLINDER LOW	na							
SECTOR	na							
SECTOR COUNT	na							
	BBK	UNC	MC	IDNF	MCR	ABRT	TK0NF	AMNF
ERROR	0	0	0	0	0	V	0	0

Identify Drive

This command passes to the host one sector of data describing the card's parameters. See Table 2 on page 9 for a detailed description of the Identify Drive data.

Identify Drive Command Issued by Host								
Task File Register	7	6	5	4	3	2	1	0
COMMAND	ECh							
DRIVE/HEAD	nu	nu	nu	D	nu			
CYLINDER HI	nu							
CYLINDER LOW	nu							
SECTOR START	nu							
SECTOR COUNT	nu							
FEATURES	nu							

Command Block specified upon completion/termination of Identify Drive command (ECh)								
Task File Register	7	6	5	4	3	2	1	0
	BSY	DRDY	DWF	DSC	DRQ	CORR	IDX	ERR
STATUS	0	1	0	1	V	V	0	0
DRIVE/HEAD	na	na	na	na	na			
CYLINDER HI	na							
CYLINDER LOW	na							
SECTOR	na							
SECTOR COUNT	na							
	BBK	UNC	MC	IDNF	MCR	ABRT	TK0NF	AMNF
ERROR	0	0	0	0	0	0	0	0

Table 2. Identify Drive Information

Word	Data	Description		
0	848Ah	General configuration bit-significant information:		
		bit	Data	Description
		15	1	Non-rotating disk drive
		14	0	Format speed tolerance gap not required
		13	0	Track offset option not available
		12	0	Data strobe offset option not available
		11	0	Rotational speed tolerance is < 0.5%
		10	1	Disk transfer rate > 10Mbs
		9	0	10 Mbs <= Disk transfer rate > 5Mbs
		8	0	Disk transfer rate !<= 5Mbs
		7	1	Removable cartridge drive
		6	0	Not a fixed drive
		5	0	Spindle motor control option not implemented
		4	0	Head switch time !> 15µsec
		3	1	Not MFM encoded
		2	0	Not soft sectored
		1	1	Hard sectored
		0	0	reserved
1	Note 1	Number of Cylinders		
2	0000h	reserved		
3	0008h	Number of Heads		
4	4000h	Number of unformatted bytes per track		
5	0200h	Number of unformatted bytes per sector		
6	0020h	Number of sectors per track		
7-9	0000h 0000h 0000h	vendor unique		
10-19	2020h ...2020h	20 ASCII char serial number. Words 10-19 are filled with 20 ASCII ‘ **s** pace’ chars, 20h		
20	0003h	Buffer type: Dual ported, multi-sector, w/read cache		
21	0002h	Bufer size, in 512 byte increments		
22	0004h	ECC length		
23-26	‘00001.02’	Firmware revision, 8 ASCII chars		
27-46	‘ ðððð ’ ð ð’ ‘ððð ð’	Model number, 40 ASCII chars. Note: ‘ð ’ denotes the ASCII ‘ **s** pace’ character, 20h		
47	0001h	Maximum Block Count=1 for Read/write Multiple commands		
48	0000h	Cannot perform doubleword I/O		
49	0200h	Capabilities: LBA supported, DMA not supported		
50	0000h	reserved		
51	0200h	PIO timing mode 2,		
52	0000h	DMA transfer not supported		
53	0001h	Words 54 - 58 are valid		
54	Note 1	Number of Current Cylinders		
55	Note 1	Number of Current Heads		
56	Note 1	Number of Current Sectors Per Track		
57	Note 1	LSW of the Current Capacity in Sectors		
58	0000h	MSW of the Current Capacity in Sectors		
59	0001h	Current Setting for Block Count=1 for R/W Multiple commands		
60	Note 1	LSW of the total number of user addressable LBA’ **s**		
61	0000h	MSW of the total number of user addressable LBA’ **s**		
62	0000h	DMA transfer not supported		
63	0000h	DMA transfer not supported		
64-127	2020h ...	reserved. Words 64 through 255 are filled with the ASCII ‘ **s** pace’ character, 20h		
128-159	... 2020h ...	vendor unique		
160-255	... 2020h	reserved		

Note 1: These values are dependent upon the total capacity of the specific card.

Idle

Although this command is supported for backward compatibility, it has no actual function. The card will always return good status at the completion of this command.

Idle Command Issued by Host								
Task File Register	7	6	5	4	3	2	1	0
COMMAND	97h/E3h							
DRIVE/HEAD	nu	nu	nu	D	nu			
CYLINDER HI	nu							
CYLINDER LOW	nu							
SECTOR START	nu							
SECTOR COUNT	Timeout Parameter. This parameter is ignored by the card.							
FEATURES	nu							

Command Block specified upon completion/termination of Idle command (97h/E3h)								
Task File Register	7	6	5	4	3	2	1	0
	BSY	DRDY	DWF	DSC	DRQ	CORR	IDX	ERR
STATUS	0	1	0	1	V	V	0	0
DRIVE/HEAD	na	na	na	na	na			
CYLINDER HI	na							
CYLINDER LOW	na							
SECTOR	na							
SECTOR COUNT	na							
	BBK	UNC	MC	IDNF	MCR	ABRT	TK0NF	AMNF
ERROR	0	0	0	0	0	0	0	0

Idle Immediate

Although this command is supported for backward compatibility, it has no actual function. The card will always return good status at the completion of this command.

Idle Immediate Command Issued by Host								
Task File Register	7	6	5	4	3	2	1	0
COMMAND	95h/E1h							
DRIVE/HEAD	nu	nu	nu	D	nu			
CYLINDER HI	nu							
CYLINDER LOW	nu							
SECTOR START	nu							
SECTOR COUNT	nu							
FEATURES	nu							

Command Block specified upon completion/termination of Idle Immediate command (95h/E1h)								
Task File Register	7	6	5	4	3	2	1	0
	BSY	DRDY	DWF	DSC	DRQ	CORR	IDX	ERR
STATUS	0	1	0	1	V	V	0	0
DRIVE/HEAD	na	na	na	na	na			
CYLINDER HI	na							
CYLINDER LOW	na							
SECTOR	na							
SECTOR COUNT	na							
	BBK	UNC	MC	IDNF	MCR	ABRT	TK0NF	AMNF
ERROR	0	0	0	0	0	0	0	0

Initialize Drive Parameters

This command allows the host to alter the number of sectors per track and the number of heads per cylinder. This enables Translation Mode which maps the flash storage using the altered parameters. On Host Reset, the default is 32 Sectors per Track and 4 Heads per Cylinder. The current values used for mapping are returned in the Identify Drive command as Number of Current Sectors per Track, and Number of Current Heads.

Initialize Drive Parameters Command Issued by Host								
Task File Register	7	6	5	4	3	2	1	0
COMMAND	91h							
DRIVE/HEAD	nu	nu	nu	D	Number of Heads per Cyl minus 1			
CYLINDER HI	nu							
CYLINDER LOW	nu							
SECTOR START	nu							
SECTOR COUNT	The Number of Sectors per Track							
FEATURES	nu							

Command Block specified upon completion/termination of Initialize Drive Parameters command (91h)								
Task File Register	7	6	5	4	3	2	1	0
	BSY	DRDY	DWF	DSC	DRQ	CORR	IDX	ERR
STATUS	0	1	0	1	V	V	0	0
DRIVE/HEAD	na	na	na	na	na			
CYLINDER HI	na							
CYLINDER LOW	na							
SECTOR	na							
SECTOR COUNT	na							
	BBK	UNC	MC	IDNF	MCR	ABRT	TK0NF	AMNF
ERROR	0	0	0	0	0	0	0	0

Read Buffer

This command transfers the current contents of the first page of the data buffer (512 bytes) to the host.

Read Buffer Command Issued by Host								
Task File Register	7	6	5	4	3	2	1	0
COMMAND	E4h							
DRIVE/HEAD	nu	nu	nu	D	nu			
CYLINDER HI	nu							
CYLINDER LOW	nu							
SECTOR START	nu							
SECTOR COUNT	nu							
FEATURES	nu							

Command Block specified upon completion/termination of Read Buffer command (E4h)								
Task File Register	7	6	5	4	3	2	1	0
	BSY	DRDY	DWF	DSC	DRQ	CORR	IDX	ERR
STATUS	0	1	0	1	V	V	0	0
DRIVE/HEAD	na	na	na	na	na			
CYLINDER HI	na							
CYLINDER LOW	na							
SECTOR	na							
SECTOR COUNT	na							
	BBK	UNC	MC	IDNF	MCR	ABRT	TK0NF	AMNF
ERROR	0	0	0	0	0	0	0	0

Read Long (w/ and wo/ retry)

This command is similar to the Read Sectors command except the contents of the Sector Count register are ignored and only one sector is read. The 512 data bytes and 4 ECC bytes are read into the buffer (with no ECC correction) and then transferred to the host.

Command Issued by Host								
Task File Register	7	6	5	4	3	2	1	0
COMMAND	22h (retries enabled) -or- 23h (retries disabled)							
DRIVE/HEAD	nu	L	nu	D	H[3:0] or LBA[27:24] of the sector/LBA to transfer			
CYLINDER HI	Cylinder[15:8] or LBA[23:16] of the sector/LBA to transfer							
CYLINDER LOW	Cylinder[7:0] or LBA[15:8] of the sector/LBA to transfer							
SECTOR START	Sector[7:0] or LBA[7:0] of the sector/LBA to transfer							
SECTOR COUNT	The number of sectors/logical blocks to transfer. This should be set to 01 for compatibility							
FEATURES	nu							

Command Block specified upon completion/termination of Read Long command (22h/23h)								
Task File Register	7	6	5	4	3	2	1	0
	BSY	DRDY	DWF	DSC	DRQ	CORR	IDX	ERR
STATUS	0	1	0	1	V	V	0	V
DRIVE/HEAD	na	na	na	na	H[3:0] or LBA[27:24] of the sector requested			
CYLINDER HI	Cylinder[15:8] or LBA[23:16] of the sector requested							
CYLINDER LOW	Cylinder[7:0] or LBA[15:8] of the sector requested							
SECTOR	Sector[7:0] or LBA[7:0] of the sector requested							
SECTOR COUNT	00 if the command proceeded without error. 01 if an error occurred							
	BBK	UNC	MC	IDNF	MCR	ABRT	TK0NF	AMNF
ERROR	0	0	0	V	0	0	0	0

Read Multiple

This command is supported for backward compatibility. If R/W Multiple commands have been enabled by a previous valid Set Multiple command, the Read Multiple command is identical to Read Sectors operation except that several sectors are transferred as a block to the Host without intervening Host handshaking. The number of sectors to transfer as a block is referred to as the block count. The block count is established using the Set Multiple command. Although the Set Multiple, and R/W Multiple commands are supported, the only valid block count is one.
If Read Multiple has not been enabled, the ABRT (Aborted Command) bit is set in the Error register and the command terminates.

Read Multiple Command Issued by Host								
Task File Register	7	6	5	4	3	2	1	0
COMMAND	C4h							
DRIVE/HEAD	nu	L	nu	D	H[3:0] or LBA[27:24] of the starting sector/LBA			
CYLINDER HI	Cylinder[15:8] or LBA[23:16] of the first sector/LBA to transfer							
CYLINDER LOW	Cylinder[7:0] or LBA[15:8] of the first sector/LBA to transfer							
SECTOR START	Sector[7:0] or LBA[7:0] of the first sector/LBA to transfer							
SECTOR COUNT	The number of sectors/logical blocks to transfer							
FEATURES	nu							

Command Block specified upon completion/termination of Read Multiple command (C4h)								
Task File Register	7	6	5	4	3	2	1	0
	BSY	DRDY	DWF	DSC	DRQ	CORR	IDX	ERR
STATUS	0	1	0	1	V	V	0	V
DRIVE/HEAD	na	na	na	na	H[3:0] or LBA[27:24] last good sector transferred			
CYLINDER HI	Cylinder[15:8] or LBA[23:16] of the last good sector transferred							
CYLINDER LOW	Cylinder[7:0] or LBA[15:8] of the last good sector transferred							
SECTOR	Sector[7:0] or LBA[7:0] of the last good sector transferred							
SECTOR COUNT	The number of sectors that were not transferred if an unrecoverable error occurred. Zero otherwise.							
	BBK	UNC	MC	IDNF	MCR	ABRT	TK0NF	AMNF
ERROR	0	V	0	V	0	0	0	0

Read Sectors

This command transfers data from the FCA card to the Host. Data transfer starts at the sector specified by the Cylinder, Head, and Sector Number registers in the Task File, and proceeds for the number of sectors specified in the Sector Count Register.

Read Sectors Command Issued by Host								
Task File Register	7	6	5	4	3	2	1	0
COMMAND	20h (retries enabled) -or- 21h (retries disabled)							
DRIVE/HEAD	nu	L	nu	D	H[3:0] or LBA[27:24] of the starting sector/LBA			
CYLINDER HI	Cylinder[15:8] or LBA[23:16] of the first sector/LBA to transfer							
CYLINDER LOW	Cylinder[7:0] or LBA[15:8] of the first sector/LBA to transfer							
SECTOR START	Sector[7:0] or LBA[7:0] of the first sector/LBA to transfer							
SECTOR COUNT	The number of sectors/logical blocks to transfer							
FEATURES	nu							

Command Block specified upon completion/termination of Read Sectors command (20h/21h)								
Task File Register	7	6	5	4	3	2	1	0
	BSY	DRDY	DWF	DSC	DRQ	CORR	IDX	ERR
STATUS	0	1	0	1	V	V	0	V
DRIVE/HEAD	na	na	na	na	H[3:0] or LBA[27:24] last good sector transferred			
CYLINDER HI	Cylinder[15:8] or LBA[23:16] of the last good sector transferred							
CYLINDER LOW	Cylinder[7:0] or LBA[15:8] of the last good sector transferred							
SECTOR	Sector[7:0] or LBA[7:0] of the last good sector transferred							
SECTOR COUNT	The number of sectors that were not transferred if an unrecoverable error occurred							
	BBK	UNC	MC	IDNF	MCR	ABRT	TK0NF	AMNF
ERROR	0	V	0	V	0	0	0	0

Read Verify Sectors

The Read Verify Sectors command verifies one or more sectors on the card by transferring data from the Flash media to the data buffer in the card and verifying that the ECC is correct. It is performed identically to the Read Sectors command, except that DRQ is not asserted, and no data is transferred to the host. If an uncorrectable error occurs, the read verify will be terminated at the failing sector. The Command Block Registers contain the CHS, or LBA of the sector in which the error occurred.

Read Verify Sectors Command Issued by Host								
Task File Register	7	6	5	4	3	2	1	0
COMMAND	40h (retries enabled) -or- 41h (retries disabled)							
DRIVE/HEAD	nu	L	nu	D	H[3:0] or LBA[27:24] of the starting sector/LBA			
CYLINDER HI	Cylinder[15:8] or LBA[23:16] of the first sector/LBA to verify							
CYLINDER LOW	Cylinder[7:0] or LBA[15:8] of the first sector/LBA to verify							
SECTOR START	Sector[7:0] or LBA[7:0] of the first sector/LBA to verify							
SECTOR COUNT	The number of sectors/logical blocks to verify							
FEATURES	nu							

Command Block specified upon completion/termination of Read Verify Sectors command (40h/41h)								
Task File Register	7	6	5	4	3	2	1	0
	BSY	DRDY	DWF	DSC	DRQ	CORR	IDX	ERR
STATUS	0	1	0	1	V	V	0	V
DRIVE/HEAD	na	na	na	na	H[3:0] or LBA[27:24] last sector verified, or sector where an unrecoverable error occurred			
CYLINDER HI	Cylinder[15:8] or LBA[23:16] of the sector verified, or sector where an unrecoverable error occurred							
CYLINDER LOW	Cylinder[7:0] or LBA[15:8] of the sector verified, or sector where an unrecoverable error occurred							
SECTOR	Sector or LBA[7:0] of the sector verified, or sector where an unrecoverable error occurred							
SECTOR COUNT	The number of sectors that not yet verified if an unrecoverable error occurred							
	BBK	UNC	MC	IDNF	MCR	ABRT	TK0NF	AMNF
ERROR	0	V	0	V	0	0	0	0

Recalibrate

Although this command is supported for backward compatibility, it has no actual function. The card will always return good status at the completion of this command.

Recalibrate Command Issued by Host								
Task File Register	7	6	5	4	3	2	1	0
COMMAND	1xh							
DRIVE/HEAD	nu	nu	nu	D	nu			
CYLINDER HI	nu							
CYLINDER LOW	nu							
SECTOR START	nu							
SECTOR COUNT	nu							
FEATURES	nu							

Command Block specified upon completion/termination of Recalibrate command (1xh)								
Task File Register	7	6	5	4	3	2	1	0
	BSY	DRDY	DWF	DSC	DRQ	CORR	IDX	ERR
STATUS	0	1	0	1	V	V	0	0
DRIVE/HEAD	na	na	na	na	na			
CYLINDER HI	na							
CYLINDER LOW	na							
SECTOR	na							
SECTOR COUNT	na							
	BBK	UNC	MC	IDNF	MCR	ABRT	TK0NF	AMNF
ERROR	0	0	0	0	0	0	0	0

Seek

This command is supported for backward compatibility. Although this command has no actual function, it does perform a range check of valid track, and posts an IDNF error if the Head or Cylinder specified are out of bounds.

Seek Command Issued by Host								
Task File Register	7	6	5	4	3	2	1	0
COMMAND	7xh							
DRIVE/HEAD	nu	L	nu	D	H[3:0] or LBA[27:24] of the track			
CYLINDER HI	Cylinder[15:8] or LBA[23:16] of the track							
CYLINDER LOW	Cylinder[7:0] or LBA[15:8] of the track							
SECTOR START	(Valid in LBA mode only) LBA[7:0] of the track							
SECTOR COUNT	nu							
FEATURES	nu							

Command Block specified upon completion/termination of Seek command (7xh)								
Task File Register	7	6	5	4	3	2	1	0
	BSY	DRDY	DWF	DSC	DRQ	CORR	IDX	ERR
STATUS	0	1	0	1	0	0	0	0
DRIVE/HEAD	na	na	na	na	na			
CYLINDER HI	na							
CYLINDER LOW	na							
SECTOR	na							
SECTOR COUNT	na							
	BBK	UNC	MC	IDNF	MCR	ABRT	TK0NF	AMNF
ERROR	0	0	0	V	0	0	0	0

Set Features

This command allows the host to alter the card's internal clock, choosing from three speeds to optimize performance and power. Table 3 on page 21shows the valid data which may be set in the Feature Register by the Host. All other values are invalid and will cause the ABRT (Command Aborted) bit to be set in the Error Register and the command to terminate. A feature number of 97h specifies that the FCA card' **s** internal clock is to be set according to the code in the Sector Count register. The remaining valid values are essentially NOPs, simply returning command completed status.

Set Features Command Issued by Host								
Task File Register	7	6	5	4	3	2	1	0
COMMAND	EFh							
DRIVE/HEAD	nu	nu	nu	D	nu			
CYLINDER HI	nu							
CYLINDER LOW	nu							
SECTOR START	nu							
SECTOR COUNT	If Feature Number = 97h, then specifies the card' **s** internal clock according to Table 4 below							
FEATURES	Feature Number. Refer to Table 3.							

Command Block specified upon completion/termination of Set Features command (EFh)								
Task File Register	7	6	5	4	3	2	1	0
	BSY	DRDY	DWF	DSC	DRQ	CORR	IDX	ERR
STATUS	0	1	0	1	V	V	0	V
DRIVE/HEAD	na	na	na	na	na			
CYLINDER HI	na							
CYLINDER LOW	na							
SECTOR	na							
SECTOR COUNT	na							
	BBK	UNC	MC	IDNF	MCR	ABRT	TK0NF	AMNF
ERROR	0	0	0	0	0	V	0	0

Table 3. Description of Valid Feature Numbers

Code	Description
97h	set clock speed per contents of Sector Count Register
44h	valid; no operation (for backward compatibility)
55h	valid; no operation (for backward compatibility)
69h	valid; no operation (for backward compatibility)
96h	valid; no operation (for backward compatibility)
AAh	valid; no operation (for backward compatibility)
BBh	valid; no operation (for backward compatibility)

Table 4. Sector Count Code specifies internal clock rate

Code	Description
00h	Divide by 4
0Ah	Divide by 2
0Bh	Divide by 2
0Eh	Divide by 1
0Fh	Divide by 1

Set Multiple

This command is supported for backward compatibility. This command is used either to set the block count (number of sectors per block), simultaneously enabling R/W Multiple command support, or to disable support of R/W Multiple commands. Although setting, reading, and writing blocks are supported, the only valid block count is one. If the block count specified by the Host is greater than one, the command will be aborted; the ERR bit in the Status Register will be set, and the ABRT bit in the Error Register will be set.
If the contents of the Sector Count Register is 1, Read Multiple and Write Multiple commands are enabled until the next Host RESET.
Invoking this command with Sector Count = 0 will disable R/W Multiple commands. In this case, all subsequent R/W Multiple commands issued by the Host will be aborted by the FCA card.

Set Multiple Command Issued by Host								
Task File Register	7	6	5	4	3	2	1	0
COMMAND	C6h							
DRIVE/HEAD	nu	nu	nu	D	nu			
CYLINDER HI	nu							
CYLINDER LOW	nu							
SECTOR START	nu							
SECTOR COUNT	01: R/W Multiple command transfer enabled, 00: R/W Multiple command transfer disabled							
FEATURES	nu							

Command Block specified upon completion/termination of Set Multiple command (C6h)								
Task File Register	7	6	5	4	3	2	1	0
	BSY	DRDY	DWF	DSC	DRQ	CORR	IDX	ERR
STATUS	0	1	0	1	V	V	0	V
DRIVE/HEAD	na	na	na	na	na			
CYLINDER HI	na							
CYLINDER LOW	na							
SECTOR	na							
SECTOR COUNT	na							
	BBK	UNC	MC	IDNF	MCR	ABRT	TK0NF	AMNF
ERROR	0	0	0	0	0	V	0	0

Sleep

Although this command is supported for backward compatibility, it has no actual function. The card will always return good status at the completion of this command.

Sleep Command Issued by Host								
Task File Register	7	6	5	4	3	2	1	0
COMMAND	99h/E6h							
DRIVE/HEAD	nu	nu	nu	D	nu			
CYLINDER HI	nu							
CYLINDER LOW	nu							
SECTOR START	nu							
SECTOR COUNT	nu							
FEATURES	nu							

Command Block specified upon completion/termination of Sleep command (99h/E6h)								
Task File Register	7	6	5	4	3	2	1	0
	BSY	DRDY	DWF	DSC	DRQ	CORR	IDX	ERR
STATUS	0	1	0	1	0	0	0	0
DRIVE/HEAD	na	na	na	na	na			
CYLINDER HI	na							
CYLINDER LOW	na							
SECTOR	na							
SECTOR COUNT	na							
	BBK	UNC	MC	IDNF	MCR	ABRT	TK0NF	AMNF
ERROR	0	0	0	0	0	0	0	0

Standby

Although this command is supported for backward compatibility, it has no actual function. The card will always return good status at the completion of this command.

Standby Command Issued by Host								
Task File Register	7	6	5	4	3	2	1	0
COMMAND	96h/E2h							
DRIVE/HEAD	nu	nu	nu	D	nu			
CYLINDER HI	nu							
CYLINDER LOW	nu							
SECTOR START	nu							
SECTOR COUNT	Timeout Parameter. This is ignored by the FCA card							
FEATURES	nu							

Command Block specified upon completion/termination of Standby command (96h/E2h)								
Task File Register	7	6	5	4	3	2	1	0
	BSY	DRDY	DWF	DSC	DRQ	CORR	IDX	ERR
STATUS	0	1	0	1	0	0	0	0
DRIVE/HEAD	na	na	na	na	na			
CYLINDER HI	na							
CYLINDER LOW	na							
SECTOR	na							
SECTOR COUNT	na							
	BBK	UNC	MC	IDNF	MCR	ABRT	TK0NF	AMNF
ERROR	0	0	0	0	0	0	0	0

Standby Immediate

Although this command is supported for backward compatibility, it has no actual function. The card will always return good status at the completion of this command.

Standby Immediate Command Issued by Host								
Task File Register	7	6	5	4	3	2	1	0
COMMAND	94H/E0h							
DRIVE/HEAD	nu	nu	nu	D	nu			
CYLINDER HI	nu							
CYLINDER LOW	nu							
SECTOR START	nu							
SECTOR COUNT	nu							
FEATURES	nu							

Command Block specified upon completion/termination of Standby Immediate command (94H/E0h)								
Task File Register	7	6	5	4	3	2	1	0
	BSY	DRDY	DWF	DSC	DRQ	CORR	IDX	ERR
STATUS	0	1	0	1	V0	V0	0	0
DRIVE/HEAD	na	na	na	na	na			
CYLINDER HI	na							
CYLINDER LOW	na							
SECTOR	na							
SECTOR COUNT	na							
	BBK	UNC	MC	IDNF	MCR	ABRT	TK0NF	AMNF
ERROR	0	0	0	0	0	0	0	0

Write Buffer

This command transfers 512 bytes of data from the host to the first page of the data buffer.

Write Buffer Command Issued by Host								
Task File Register	7	6	5	4	3	2	1	0
COMMAND	E8h							
DRIVE/HEAD	nu	nu	nu	D	nu			
CYLINDER HI	nu							
CYLINDER LOW	nu							
SECTOR START	nu							
SECTOR COUNT	nu							
FEATURES	nu							

Command Block specified upon completion/termination of Write Buffer command (E8h)								
Task File Register	7	6	5	4	3	2	1	0
	BSY	DRDY	DWF	DSC	DRQ	CORR	IDX	ERR
STATUS	0	1	0	1	V	V	0	0
DRIVE/HEAD	na	na	na	na	na			
CYLINDER HI	na							
CYLINDER LOW	na							
SECTOR	na							
SECTOR COUNT	na							
	BBK	UNC	MC	IDNF	MCR	ABRT	TK0NF	AMNF
ERROR	0	0	0	0	0	0	0	0

Write Long (w/ and w/o retry)

This command is similar to the Write Sectors (w/ retry) except the contents of the Sector Count register are ignored and only one sector is written. The 512 data bytes and 4 ECC bytes are transferred from the host and then written from the buffer to the flash..

Write Long Command Issued by Host								
Task File Register	7	6	5	4	3	2	1	0
COMMAND	32h (retries enabled) -or- 33h (retries disabled)							
DRIVE/HEAD	nu	L	nu	D	H[3:0] or LBA[27:24] of the starting sector/LBA			
CYLINDER HI	Cylinder[15:8] or LBA[23:16] of the first sector/LBA to transfer							
CYLINDER LOW	Cylinder[7:0] or LBA[15:8] of the first sector/LBA to transfer							
SECTOR START	Sector[7:0] or LBA[7:0] of the first sector/LBA to transfer							
SECTOR COUNT	The number of sectors/logical blocks to transfer. Should be set to 1 for compatibility.							
FEATURES	nu							

Command Block specified upon completion/termination of Write Long command (32h/33h)								
Task File Register	7	6	5	4	3	2	1	0
	BSY	DRDY	DWF	DSC	DRQ	CORR	IDX	ERR
STATUS	0	1	0	1	V	V	0	V
DRIVE/HEAD	na?	L	na?	na?	H[3:0] or LBA[27:24] last good sector transferred			
CYLINDER HI	Cylinder[15:8] or LBA[23:16] of the last good sector transferred							
CYLINDER LOW	Cylinder[7:0] or LBA[15:8] of the last good sector transferred							
SECTOR	Sector[7:0] or LBA[7:0] of the last good sector transferred							
SECTOR COUNT	1 if an unrecoverable error occurred, 0 if the command proceeded successfully							
	BBK	UNC	MC	IDNF	MCR	ABRT	TK0NF	AMNF
ERROR	V	0	0	V	0	0	0	V0

Write Multiple

This command is supported for backward compatibility. If R/W Multiple commands have been enabled by a previous valid Set Multiple command, the Write Multiple command is identical to Write Sectors (w/retry) operation except that several sectors are transferred as a block from the Host without intervening Host handshaking. The number of sectors to transfer as a block is referred to as the block count. Although the Set Multiple, and R/W Multiple commands are supported, the only valid block size is one.
If Write Multiple has not been enabled, the ABRT (Command Aborted) bit is set in the Error register and the command terminates.

Write Multiple Command Issued by Host								
Task File Register	7	6	5	4	3	2	1	0
COMMAND	C5h							
DRIVE/HEAD	nu	L	nu	D	H[3:0] or LBA[27:24] of the starting sector/LBA			
CYLINDER HI	Cylinder[15:8] or LBA[23:16] of the first sector/LBA to transfer							
CYLINDER LOW	Cylinder[7:0] or LBA[15:8] of the first sector/LBA to transfer							
SECTOR START	Sector[7:0] or LBA[7:0] of the first sector/LBA to transfer							
SECTOR COUNT	The number of sectors/logical blocks to transfer							
FEATURES	nu							

Command Block specified upon completion/termination of Write Multiple command (C5h)								
Task File Register	7	6	5	4	3	2	1	0
	BSY	DRDY	DWF	DSC	DRQ	CORR	IDX	ERR
STATUS	0	1	0	1	V	V	0	V
DRIVE/HEAD	na?	L	na?	na?	H[3:0] or LBA[27:24] last good sector transferred			
CYLINDER HI	Cylinder[15:8] or LBA[23:16] of the last good sector transferred							
CYLINDER LOW	Cylinder[7:0] or LBA[15:8] of the last good sector transferred							
SECTOR	Sector[7:0] or LBA[7:0] of the last good sector transferred							
SECTOR COUNT	The number of sectors that were not transferred if an unrecoverable error occurred							
	BBK	UNC	MC	IDNF	MCR	ABRT	TK0NF	AMNF
ERROR	V	0	0	V	0	0	0	0

Write Sectors

This command transfers data from the Host to the FCA card. Data transfer starts at the sector specified by the Cylinder, Head, and Sector Number registers in the Task File, and proceeds for the number of sectors specified in the Sector Count Register.
If the address of the starting sector is not within the range of addresses supported by this card, the IDNF (ID Not Found)) bit is set in the Error Register and the command terminates.

Write Sectors Command Issued by Host								
Task File Register	7	6	5	4	3	2	1	0
COMMAND	30h (retries enabled) -or- 31h (retries disabled)							
DRIVE/HEAD	nu	L	nu	D	H[3:0] or LBA[27:24] of the starting sector/LBA			
CYLINDER HI	Cylinder[15:8] or LBA[23:16] of the first sector/LBA to transfer							
CYLINDER LOW	Cylinder[7:0] or LBA[15:8] of the first sector/LBA to transfer							
SECTOR START	Sector[7:0] or LBA[7:0] of the first sector/LBA to transfer							
SECTOR COUNT	The number of sectors/logical blocks to transfer							
FEATURES	nu							

Command Block specified upon completion/termination of Write Sectors command (30h/31h)								
Task File Register	7	6	5	4	3	2	1	0
	BSY	DRDY	DWF	DSC	DRQ	CORR	IDX	ERR
STATUS	0	1	0	1	V	V	0	V
DRIVE/HEAD	na?	L	na?	na?	H[3:0] or LBA[27:24] last good sector transferred			
CYLINDER HI	Cylinder[15:8] or LBA[23:16] of the last good sector transferred							
CYLINDER LOW	Cylinder[7:0] or LBA[15:8] of the last good sector transferred							
SECTOR	Sector[7:0] or LBA[7:0] of the last good sector transferred							
SECTOR COUNT	The number of sectors that were not transferred if an unrecoverable error occurred							
	BBK	UNC	MC	IDNF	MCR	ABRT	TK0NF	AMNF
ERROR	V	0	0	V	0	0	0	0

Vendor Unique Commands

Erase Sectors

This command is supported for backward compatibility. It has no actual function, and will always return good status.

Erase Sectors Command Issued by Host								
Task File Register	7	6	5	4	3	2	1	0
COMMAND	C0h							
DRIVE/HEAD	nu	nu	nu	D	nu			
CYLINDER HI	nu							
CYLINDER LOW	nu							
SECTOR START	nu							
SECTOR COUNT	nu							
FEATURES	nu							

Command Block specified upon completion/termination of Erase Sectors command (C0h)								
Task File Register	7	6	5	4	3	2	1	0
	BSY	DRDY	DWF	DSC	DRQ	CORR	IDX	ERR
STATUS	0	1	0	1	0	0	0	0
DRIVE/HEAD	na	na	na	na	na			
CYLINDER HI	na							
CYLINDER LOW	na							
SECTOR	na							
SECTOR COUNT	na							
	BBK	UNC	MC	IDNF	MCR	ABRT	TK0NF	AMNF
ERROR	0	0	0	0	0	0	0	0

Wear Leveling

Although this command is supported for backward compatibility, it has no actual function. The card will always return good status at the completion of this command.

Wear Leveling Command Issued by Host								
Task File Register	7	6	5	4	3	2	1	0
COMMAND	F5h							
DRIVE/HEAD	nu	nu	nu	D	nu			
CYLINDER HI	nu							
CYLINDER LOW	nu							
SECTOR START	nu							
SECTOR COUNT	nu							
FEATURES	nu							

Command Block specified upon completion/termination of Wear Leveling command (F5h)								
Task File Register	7	6	5	4	3	2	1	0
	BSY	DRDY	DWF	DSC	DRQ	CORR	IDX	ERR
STATUS	0	1	0	1	V	V	0	0
DRIVE/HEAD	na	na	na	na	na			
CYLINDER HI	na							
CYLINDER LOW	na							
SECTOR	na							
SECTOR COUNT	na							
	BBK	UNC	MC	IDNF	MCR	ABRT	TK0NF	AMNF
ERROR	0	0	0	0	0	0	0	0

Reserved Command Codes F1h, FCh, Fdh, and FEh