Data Sheets

Codicount
7-Segment-LED-Displays

Series 800

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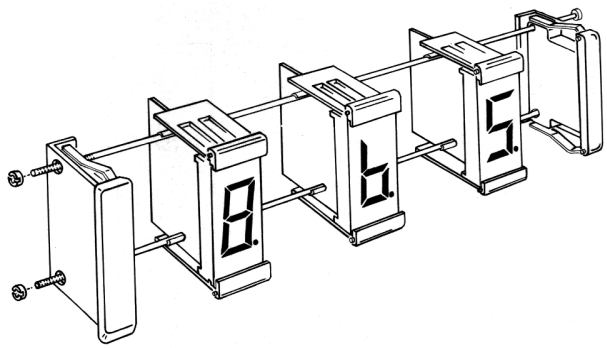
Mounting instructions

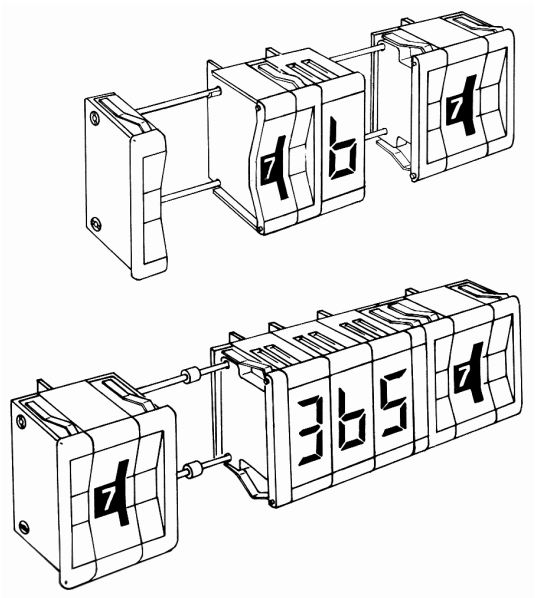
Assembly

The individual display modules are lined up in blocks. Each block is completed with end brackets. The block is secured with threaded rods.
The assembly procedure is completed after the block is inserted through the cut-out in the front panel.
The snap springs provide reliable fastening power. In series 100 and 300, the individual modules are assembled into blocks simply by pressing them together (push-fit principle). Threaded rods can be used in both these series to fulfil extreme requirements.



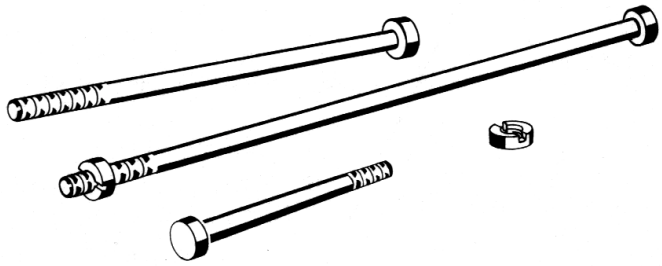
Additional assembly of division plates or dummy housings

A display block can be subdivided into groups with dummy housings. If selector switches are to be integrated in a display block, the division plates will provide a neat transition between display and switch modules. Switches can be mounted on either side of the display modules. In series 100 and 300, the division plates are one-piece elements. In the other series, they are composed of a division plate of the display series and of a division plate of the corresponding ***Multiswitch*** series. Centering sleeves simplify assembly procedures.



Mounting material

In series 500 and 800, modules are assembled with two M2 threaded rods and two M2 slotted nuts. For increased strength, series 100 / 300 can also be assembled with threaded rods and slotted nuts of size M2.



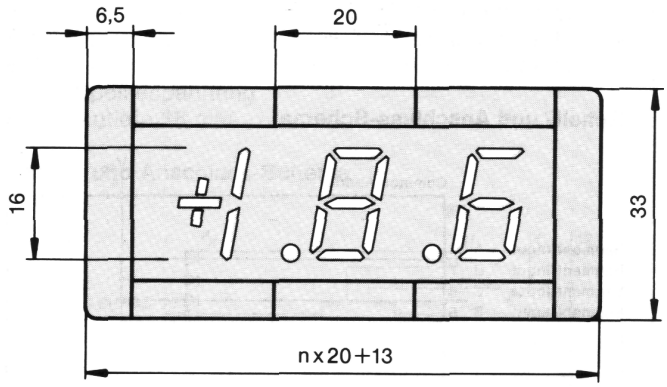
Connections

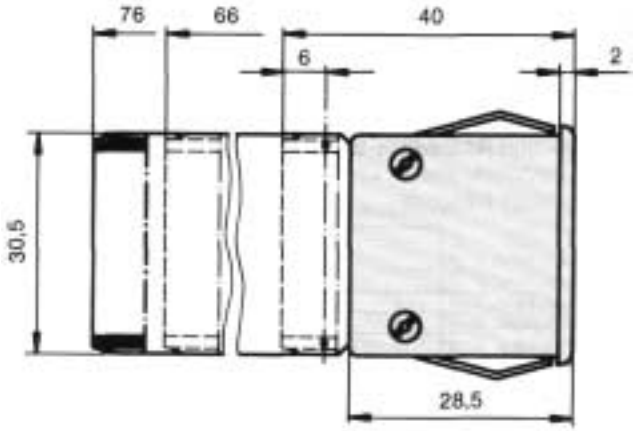
All plug connectors are hard gold-plated. A matching connector program is available.

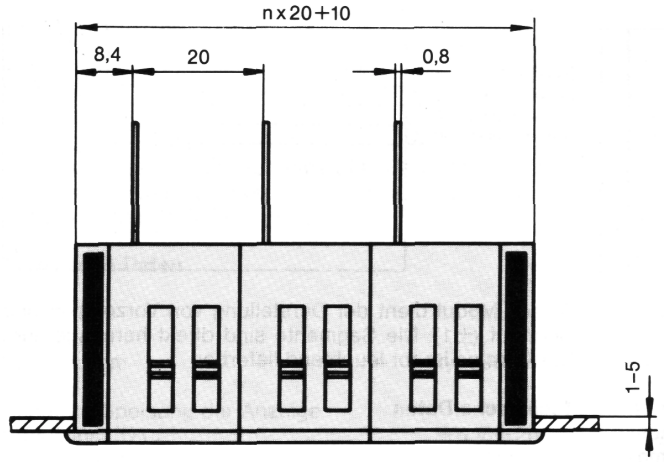
Data Sheet

Displays *Codicount*
Series 800

- Display red
- Module width 20 mm
- Contrast filters for up to 6 modules
- Block length unlimited
- Combinable with ***Multiswitches*** M, H, und S

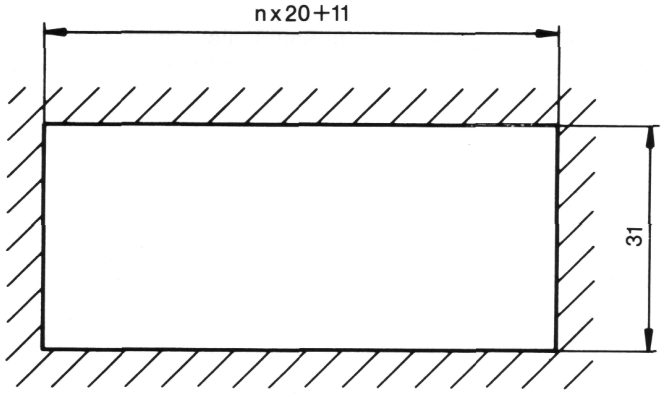




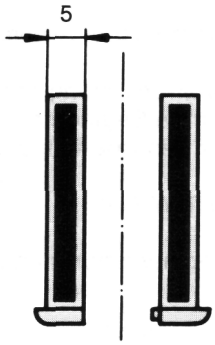


n = number of modules

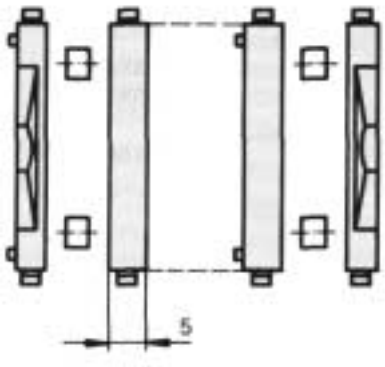
Front panel cut-out



End bracket pair



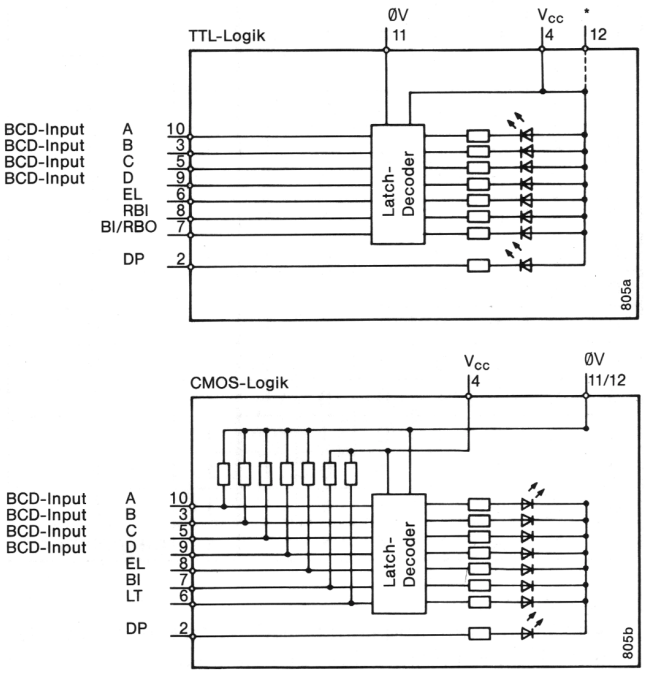
Division plates pair



Type 805

- 7-segment display
- Height of character 16 mm
- Memory
- BCD-Input
- TTL or CMOS logic
- 5 or 12 V supply voltage
- Depth when mounted 38 mm

Circuit diagram



In this module, the display is operated by the BCD code in positive logic. A control signal (Input EL) makes it possible to freeze the display without inhibiting the BCD input signals. TTL and CMOS logic models are available. The inputs of the CMOS models are terminated with resistors.

Caution:

The terminals of the TTL and CMOS models are not identical. Terminal 12* can be used to separately power the LED display in the TTL model. However, it must be specified in the order (see ordering data).

Technical data

Character height	16 mm
Supply current I_{CC}	
with TTL logic	typ. 140 mA
with CMOS logic	typ. 90 mA
Separate display power terminal in TTL-model	
(Terminal 12)	+5 V ±20 %
Depth behind panel	38 mm

Input data

Input voltage (all inputs)

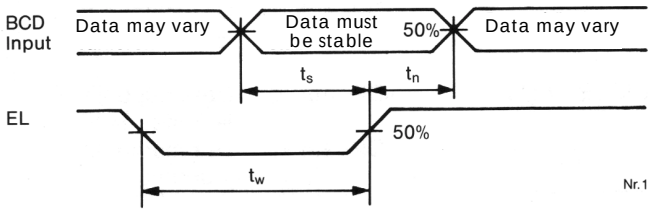
		TTL	CMOS
U_{in} «0» with V_{cc}	= 5 V	max. 0.8 V	1 1.5 V
	= 12 V	max.	3.6 V
U_{in} «1» with V_{cc}	= 5 V	min. 2 V	3.5 V
	= 12 V		8.4 V

Input currents

TTL logic

BCD input currents with EL = «0»

I_{in} «0» with U_{in} = 0.4 V	max. -1.6 mA
I_{in} «1» with U_{in} = 2.4 V	max. 80 µA
with EL = «1»	
I_{in} «0» and «1»	max. -0.1 mA
Inputs EL and RBI	
I_{in} «0» with U_{in} = 0.4 V	max. -1.6 mA
Input BI	
I_{in} «0» with U_{in} = 0.4 V	max. -3.2 mA
I_{in} «1» with U_{in} = 2.4 V	max. 80 µA

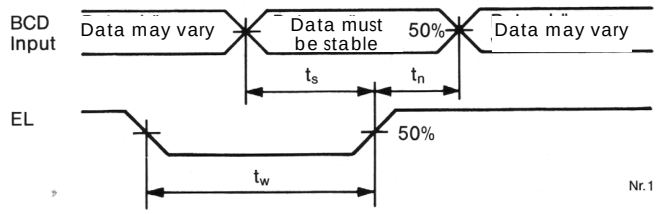


Length of storage instruction	t_w	min.	45 ns
Length of setting time	t_s	min.	30 ns
Length of holding time	t_n	min.	0 ns

CMOS logic:

All inputs Pull-up / Pull-down Resistance 100 KΩ

I_{in} «0» with U_{in}	= 1.5 V	max.	15.5 µA
	= 3 V	max.	31 µA
	= 3.6 V	max.	37 µA
	= 4.5 V	max.	46 µA
I_{in} «1» with U_{in}	= 3.5 V	max.	36 µA
	= 7 V	max.	71.5 µA
	= 8.4 V	max.	86 µA
	= 10.5 V	max.	107 µA



		V_{CC}		
Length of storage instruction	t_w	5	min.	400 ns
		10	min.	160 ns
		15	min.	100 ns
Length of setting time	t_s	5	min.	150 ns
		10	min.	70 ns
		15	min.	40 ns
Length of holding time	t_n	5	min.	75 ns
		10	min.	35 ns
		15	min.	20 ns

Output data (RBO only)

Output data		
U_{out} «0» with I_{out} = 3.2 mA	max.	0.4 V
U_{out} «1» with I_{out} = -80 µA	min.	2.4 V
Output current		
I_{out} «0»	max.	3.2 mA
I_{out} «1»	max.	-80 µA

Description for Enable Latch (EL) and Decimal Point (DP):

This instruction will freeze the display and suppress further response to changes of the BCD input

«EL» on «0» The display responds to the BCD input value.

«EL» on «1» The display freezes

DP (Decimal point): The decimal point must be controlled externally. The module features an integral current limiting resistor.

TTL logic: «DP» on «0» Decimal point on

«DP» on «1» Decimal point off

CMOS logic: «DP» on «0» Decimal point off

«DP» on «1» Decimal point on

Truth table

CMOS logic

Inputs							Outputs
EL	LT	D 2^3	C 2^2	B 2^1	A 2^0	BI	Display
x	0	x	x	x	x	x	8 (Test)
x	1	x	x	x	x	0	none
0	1	0	0	0	0	1	0
0	1	0	0	0	1	1	1
0	1	0	0	1	0	1	2
0	1	0	0	1	1	1	3
0	1	0	1	0	0	1	4
0	1	0	1	0	1	1	5
0	1	0	1	1	0	1	6
0	1	0	1	1	1	1	7
0	1	1	0	0	0	1	8
0	1	1	0	0	1	1	9
1	1	x	x	x	x	1	stored*

x = «0» or «1»

* Controlled by applied BCD code during the leading edge of the «EL» instruction signal.

TTL logic

Inputs							Outputs	
EL	RBI	D 2^3	C 2^2	B 2^1	A 2^0	BI**	RBO	Display
x	x	x	x	x	x	0	0	none
0	0	0	0	0	0	x	0	none
0	1	0	0	0	0	1	1	0
0	x	0	0	0	1	1	1	1
0	x	0	0	1	0	1	1	2
0	x	0	0	1	1	1	1	3
0	x	0	1	0	0	1	1	4
0	x	0	1	0	1	1	1	5
0	x	0	1	1	0	1	1	6
0	x	0	1	1	1	1	1	7
0	x	1	0	0	0	1	1	8
0	x	1	0	0	1	1	1	9
0	x	1	0	1	0	1	1	A
0	x	1	0	1	1	1	1	b
0	x	1	1	0	0	1	1	C
0	x	1	1	0	1	1	1	d
0	x	1	1	1	0	1	1	E
0	x	1	1	1	1	1	1	F
1	x	x	x	x	x	1	1	stored*

x = «0» or «1»

* Controlled by the applied BCD code during the leading edge of the «EL» instruction signal.

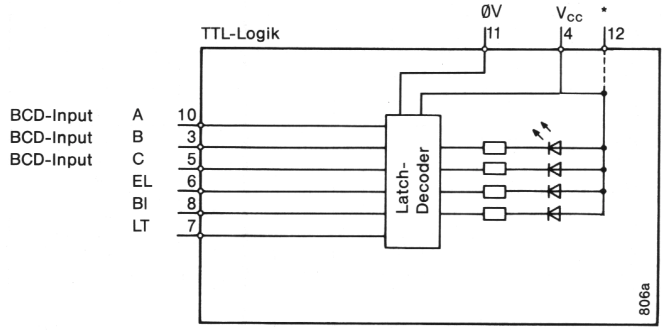
** Input BI should only be shifted to «0» to obtain blanking of the display irrespective to the BCD input. Further information on this input is provided in the general data section.

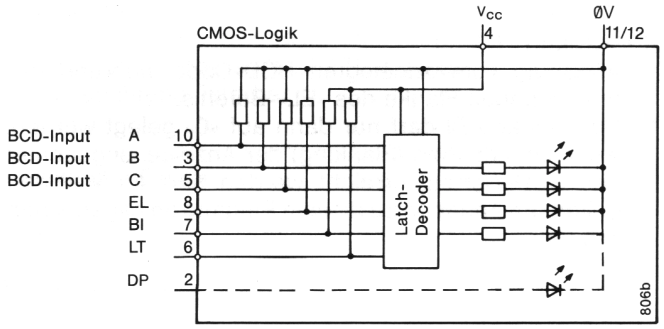
Type	VDC	Ordering code
805,	5 V, TTL	805-010-21
805,	5 V, CMOS	805-020-21
805,	12 V, CMOS	805-025-21

Type 806

- Sign and overflow display
- Height of character 16 mm
- Memory
- BCD-Input
- TTL or CMOS logic
- 5 or 12 V supply voltage
- Depth when mounted 38 mm

Circuit diagram





This module is used to display sign and overflow (±1). The display is operated by the BCD code in positive logic. A control signal (input EL) makes it possible to freeze the display without inhibiting the BCD input signals. TTL and CMOS logic models are available. The inputs of CMOS model are terminated with resistors.

Caution

The terminals of the TTL and CMOS models are not identical. Terminal 12* can be used to separately power the LED display in the TTL model. However, it must be specified in the order (see ordering data).
Observe the General handling directions for CMOS logic elements (s. page 2).

Technical data

Character height	16 mm
Supply current I_{CC}	
with TTL logic	typ. 105 mA
with CMOS logic	typ. 50 mA
Separate display power terminal in TTL model	
(Terminal 12) +5 V ±20 %	
Depth behind panel	38 mm

Input data

Input voltage

(all inputs)		TTL	CMOS
U_{in} «0» with V_{CC}	= 5 V	max. 0.8 V	1.5 V
	= 12 V	max.	3.6 V
U_{in} «1» with V_{CC}	= 5 V	min. 2 V	3.5 V
	= 12 V	min.	8.4 V

Input currents

TTL logic:

BCD input currents with EL = «0»

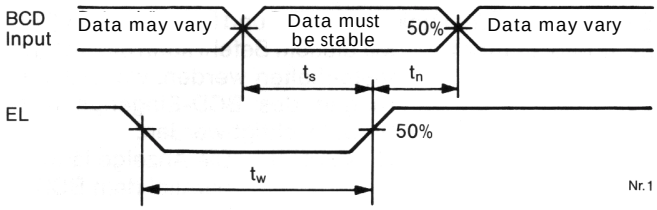
I_{in} «0» with U_{in} = 0.4 V	max.	-1.6 mA
I_{in} «1» with U_{in} = 2.4 V	max.	80 µA
with EL = 0 »		
I_{in} «0» and «1»	max.	-0.1 mA

Inputs EL and RBI

I_{in} «0» with U_{in} = 0.4 V	max.	-1.6 mA
I_{in} «1» with U_{in} = 2.4 V	max.	40 µA

Input BI

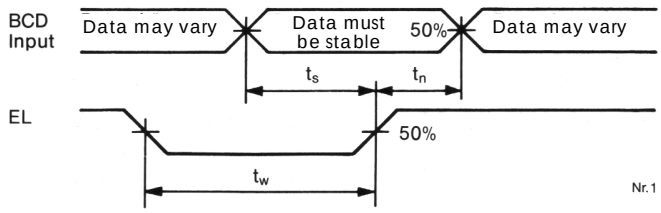
I_{in} «0» with U_{in} = 0.4 V	max.	-3.2 mA



Length of storage instruction	t_w	min. 45 ns
Length of setting time	t_s	min. 30 ns
Length of holding time	t_n	min. 0 ns

CMOS logic:

All inputs Pull-up / Pull-down Resistance			100 KΩ
I_{in} «0» with U_{in}	= 1.5 V	max.	15.5 µA
	= 3 V	max.	31 µA
	= 3.6 V	max.	37 µA
	= 4.5 V	max.	46 µA
I_{in} «1» with U_{in}	= 3.5 V	max.	36 µA
	= 7 V	max.	71.5 µA
	= 8.4 V	max.	86 µA
	= 10.5 V	max.	107 µA



		V_{CC}	
Length of storage instruction	tw	5	min. 400 ns
		10	min. 160 ns
		15	min. 100 ns
Length of setting time	ts	5	min. 150 ns
		10	min. 70 ns
		15	min. 40 ns
Length of holding time	tn	5	min. 75 ns
		10	min. 35 ns
		15	*min. 20 ns

Output data (RBO only)

Output data

U_{out} «0» with I_{out} = 3.2 mA	max. 0.4 V
U_{out} «1» with I_{out} = -80 µA	min. 2.4 V

Output current

I_{out} «0»	max. 3.2 mA
I_{out} «1»	max. -80 µA

Description of Enable Latch (EL) and Decimal Point (DP):

EL (Enable Latch):	This instruction will freeze the display and suppress further response to changes of the BCD input.	
	«EL» on «0»	The display responds to the BCD input value
	«EL» on «1»	The display freezes
TTL logic:	«DP» on «0»	Decimal point on
	«DP» on «1»	Decimal point off
CMOS logic:	«DP» on «0»	Decimal point off
	«DP» on «1»	Decimal point on

Truth table

Inputs							Outputs	
EL	RBI (TTL only)	C 2^2	B 2^1	A 2^0	LT (CMOS only)	BI**	RBO (TTL only)	Display
x	x	x	x	x	0	1	1	+1 (Test)
x	x	x	x	x	1	0	0	none
0	0	0	0	0	1	0	0	none
0	1	0	0	0	1	1	1	+1
0	x	0	0	1	1	1	1	-
0	x	0	1	0	1	1	1	1
0	x	0	1	1	1	1	1	-1
0	x	1	0	0	1	1	1	+
0	x	1	0	1	1	1	1	+1
0	x	1	1	0	1	1	1	+1
0	x	1	1	1	1	1	1	-
1	x	x	x	x	1	1	1	stored*

x = «0» or «1»

* Controlled by applied BCD code during the leading edge of the «EL» instruction signal.

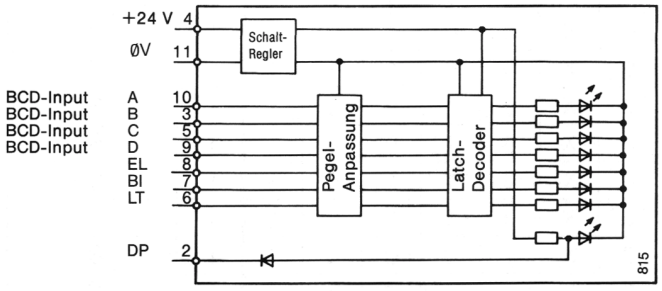
** Input BI should only be shifted to «0» to obtain blanking of the display irrespective of the BCD input. Further information on this input is provided in the general data section.

Type	VDC		Ordering code
806,	5 V,	TTL	806-010-21
806,	5 V,	CMOS	806-020-21
806,	12 V,	CMOS	806-025-21

Type 815

- 7-segment display
- Height of character 16 mm
- Memory
- BCD-Input
- Signal level adaptation
- 24 V supply voltage
- Depth when mounted 64 mm
- CE-konform

Circuit diagram



In this module, the display is controlled with the BCD code in positive logic. The signal

Technical data

Character height		16 mm
Supply voltage V_{CC}		12-30 V
Supply current I_{CC} with V_{CC}	= 12 V	typ. 61 mA
	= 24 V	typ. 36 mA
	= 30 V	typ. 30 mA
Signal voltage		10-30 V
Limit frequency with V_{CC}	= 12 V	≤ 20 kHz
	= 24 V	≤ 50 kHz
	= 30 V	≤ 50 kHz
Depth behind panel		64 mm

Input data

All inputs are connected to ground Ø V.

Input voltage all inputs

U_{in} «0»		min.	-3.5 V
or open to		max.	+2 V
U_{in} «I»		min.	+10 V
		max.	+30 V

Input currents all inputs

I_{in} «0» with	U_{in} = -3.5 V	max.	-0.3 mA
	U_{in} = +2 V	max.	+0.2 mA
I_{in} «1» with	U_{in} = +10 V	max.	1.5 mA
	U_{in} = +30 V	max.	3 mA

DP (Decimal point): The decimal point must be controlled externally. The module features an integral current limiting resistor and a protective diode.
«DP» on «0» Decimal point off
«DP» on «1» Decimal point on (+24 V) or open

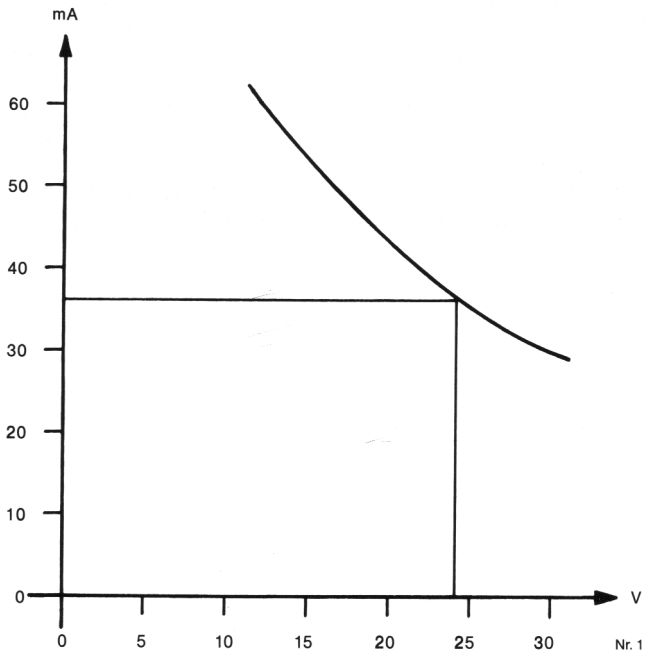
Truth table

Inputs							Outputs
LT	BI	EL	D 2^3	C 2^2	B 2^1	A 2^0	Display
1	1	0	0	0	0	0	0
1	1	0	0	0	0	1	1
1	1	0	0	0	1	0	2
1	1	0	0	0	1	1	3
1	1	0	0	1	0	0	4
1	1	0	0	1	0	1	5
1	1	0	0	1	1	0	6
1	1	0	0	1	1	1	7
1	1	0	1	0	0	0	8
1	1	0	1	0	0	1	9
0	1	x	x	x	x	x	8 (Test)
1	0	x	x	x	x	x	none
1	1	1	x	x	x	x	stored*

x = «0» or «1»

* Controlled by applied BCD code during the leading edge of the «EL» instruction signal.

Supply current in relation to supply voltage

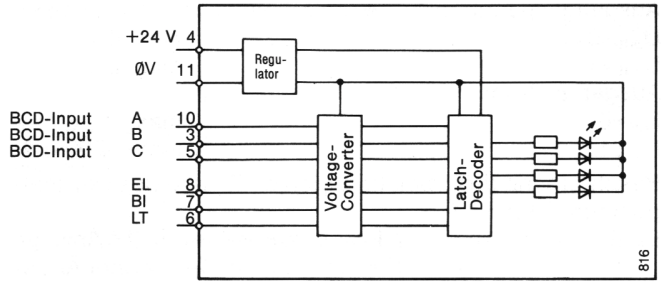


Type	VDC	Ordering code
815,	24 V	815-057-21

Type 816

- Sign and overflow display
- Height of character 16 mm
- Memory
- BCD-Input
- 24 V supply voltage
- Depth when mounted 64 mm

Circuit diagram



This module is used to display sign and overflow (±1). It is controlled with the BCD code in positive logic. The signal and supply voltage is +24 V. A control signal (input EL) makes it possible to freeze the display without affecting incoming BCD signals.

Technical data

Character height		16 mm
Supply voltage VCC		12...30 V
Supply current I_{CC} with VCC	= 12 V	typ. 30 mA
	= 24 V	typ. 18 mA
	= 30 V	typ. 16 mA
Signal voltage		10...30 V
Limit frequency with VCC	= 12 V	≤ 20 kHz
	= 24 V	≤ 950 kHz
	= 30 V	≤ 550 kHz
Depth behind panel		64 mm

Input data

All inputs are connected to ground ØV.

U_{in} «0»		min.	-3.5 V
or open to		max.	+2 V
U_{in} «1»		min.	+10 V
		max.	+30 V
Input currents (all inputs)			
I_{in} «0» with	U_{in} = -3.5 V	max.	-0.3 mA
	U_{in} = +2 V	max.	+0.2 mA
I_{in} «1» with	U_{in} = +10 V	max.	1.5 mA
	U_{in} = +30 V	max.	3 mA

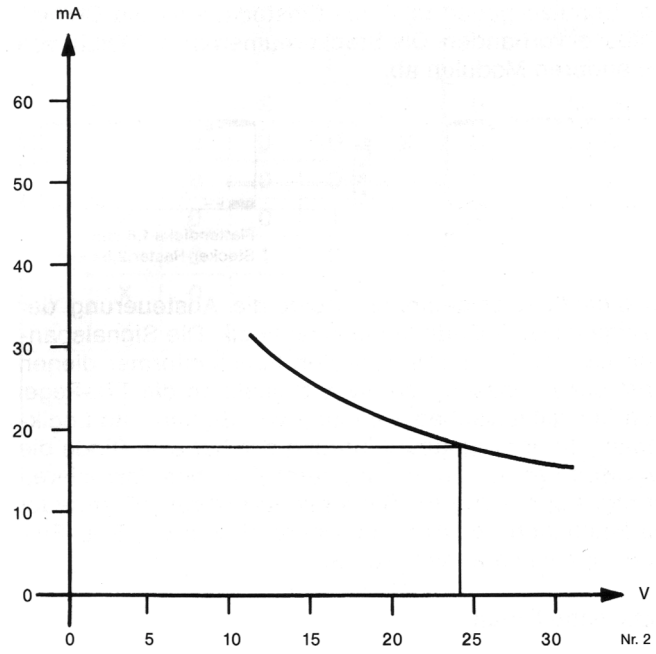
Truth table

Inputs						Outputs
LT	BI	C 2^2	B 2^1	A 2^0	EL	Display
1	1	0	0	0	0	+1
1	1	0	0	1	0	-
1	1	0	1	0	0	1
1	1	0	1	1	0	-1
1	1	1	0	0	0	+
1	1	1	0	1	0	+1
1	1	1	1	0	0	+1
1	1	1	1	1	0	-
0	1	x	x	x	x	+ 1 (Test)
1	0	x	x	x	x	none
1	1	x	x	x	1	stored*

x = «0» or «1»

* Controlled by applied BCD code during the leading edge of the «EL» instruction signal.

Supply current in relation to supply voltage

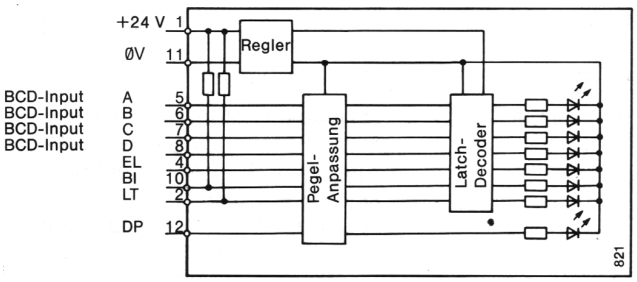


Type	VDC	Ordering code
816,	24 V	816-057-21

Type 821

- 7-segment display
- Height of character 16 mm
- Memory
- BCD-Input
- Signal level adaptation
- 24 V Signal- and supply voltage
- Depth when mounted 74 mm
- CE-konform

Circuit diagram



In this module, the display is controlled by the BCD code in positive logic. The signal and supply voltage is +24 V. A control signal (input EL) makes it possible to freeze the display without affecting incoming BCD signals. Inputs «BI» and «LT» are already connected to the 24 V power supply via internal resistors. If these inputs are not used, the module will function properly due to these resistors. Both of these inputs must be controlled in open collector circuits.

Technical data

Character height		16 mm
Supply voltage V_{CC}		12...30 V
Supply current I_{CC} with V_{CC}	= 12 V	typ. 52 mA
	= 24 V	typ. 32 mA
	= 30 V	typ. 28 mA
Signal voltage		10 V...30 V
Limit frequency with V_{CC}	= 12 V	≤ 10 kHz
	= 24 V	≤ 515 kHz
	= 30 V	≤ 20 kHz
Depth behind panel		74 mm

Input data:

Input voltage all inputs (except DP)

U_{in} «0»	min.	-3.5 V
	or open	
	max.	+2 V
U_{in} «1»	min.	+10 V
	max.	+30 V

Input voltage Input DP

U_{in} «0»	min.	-3.5 V
	max.	+0.7 V
U_{in} «1»	min.	+1.1 V
	max.	+30 V
	or open	

Input currents all inputs (except BI, LT and DP)

All inputs are connected to ØV.

I_{in} «0» with U_{in}	= -3.5 V	max. -150 µA
	= +2 V max.	140 µA
I_{in} «1» with U_{in}	= +10 V	max. 700 µA
I_{in} «0» with U_{in}	= +30 V	max. 2.6 µA

Input currents inputs LT, BI

Pull-up resistances		3.3 KΩ
I_{in} «0» with U_{in}	= -3.5 V	max. -11 mA
	= +2 V max. -9.2 mA	
I_{in} «1» with U_{in}	= +10 V	max. -7.2 mA
	= +30 V	max. 3 mA

Input voltage Input DP

I_{in} «0» with U_{in}	= -3.5 V	max. -1 mA
	= +0.7 V	max. -400 µA
I_{in} «1» with U_{in}	= +1.1 V	max. -10 µA
	= +30 V	max. 1 µA

DP (Decimal point): «DP» on «0» Decimal point on
«DP» on «1» Decimal point off
(+24 V or open)

Truth table

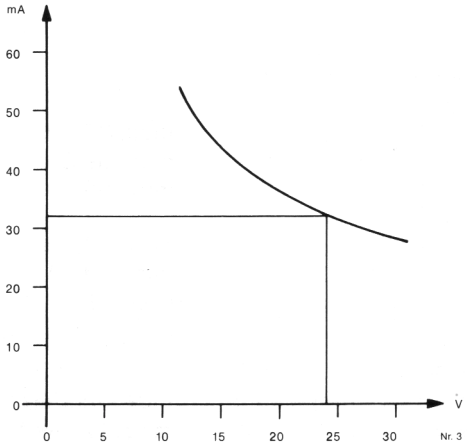
Inputs							Outputs
LT*	BI*	EL	D 2^3	C 2^2	B 2^1	A 2^0	Display
1	1	0	0	0	0	0	0
1	1	0	0	0	0	1	1
1	1	0	0	0	1	0	2
1	1	0	0	0	1	1	3
1	1	0	0	1	0	0	4
1	1	0	0	1	0	1	5
1	1	0	0	1	1	0	6
1	1	0	0	1	1	1	7
1	1	0	1	0	0	0	8
1	1	0	1	0	0	1	9
0	1	x	x	x	x	x	8 (Test)
1	0	x	x	x	x	x	none
1	1	1	x	x	x	x	stored**

x = «0» or «1»

* Inputs BI and LT are internally wired to 1. An open collector control circuit is needed.

** Controlled by the applied BCD code during the leading edge of the «EL» instruction signal (aus dt. Vorlage).

Supply current in relation to supply voltage

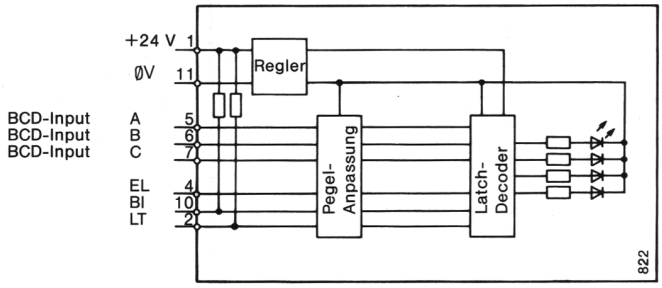


Type	VDC	Ordering code
821,	24 V	821-057-21

Type 822

- Sign and overflow display
- Height of character 16 mm
- Memory
- BCD-Input
- Signal level adaptation
- 24 V Signal- and supply voltage
- Depth when mounted 74 mm

Circuit diagram



This module is used to display sign and overflow (±1). It is controlled by the BCD code in positive logic. The signal and supply voltage is +24 V. A control signal (input EL) makes it possible to freeze the display without affecting the incoming BCD signals. Inputs «BI» and «LT» are already connected to the 24 V power supply via internal resistors. If these inputs are not used, the module will function properly due to these resistors. Both of these inputs must be controlled in open collector circuits.

Technical data

Character height		16 mm
Supply voltage VCC		12 V...30 V
Supply current I_{CC} with VCC	= 12 V	typ. 26 mA
	= 24 V	typ. 19 mA
	= 30 V	typ. 18 mA
Signal voltage		10 V...30 V
Limit frequency with VCC	= 12 V	≤ 10 kHz
	= 24 V	≤ 15 kHz
	= 30 V	≤ 20 kHz
Depth behind panel		74 mm

Input data

Input voltage all inputs

U_{in} «0»	min.	- 3.5 V
	or open	
	max.	+2 V
U_{in} «1»	min.	+10 V
	max.	+30 V

Input currents all inputs (except BI and DP)

I_{in} «0» with U_{in} = -3.5 V	max.	-150 µA
U_{in} = +2 V	max.	140 µA
I_{in} «1» with U_{in} = +10 V	max.	700 µA
I_{in} «0» with U_{in} = +30 V	max.	2.6 mA

All inputs are connected to ØV.

Input currents Inputs LT, BI

Pull-up resistances		3.3 KΩ
I_{in} «0» with U_{in} = -3.5 V	max.	-11 mA
U_{in} = +2 V	max.	-9.2 mA
I_{in} «1» with U_{in} = +10 V	max.	-7.2 mA
U_{in} = +30 V	max.	3 mA

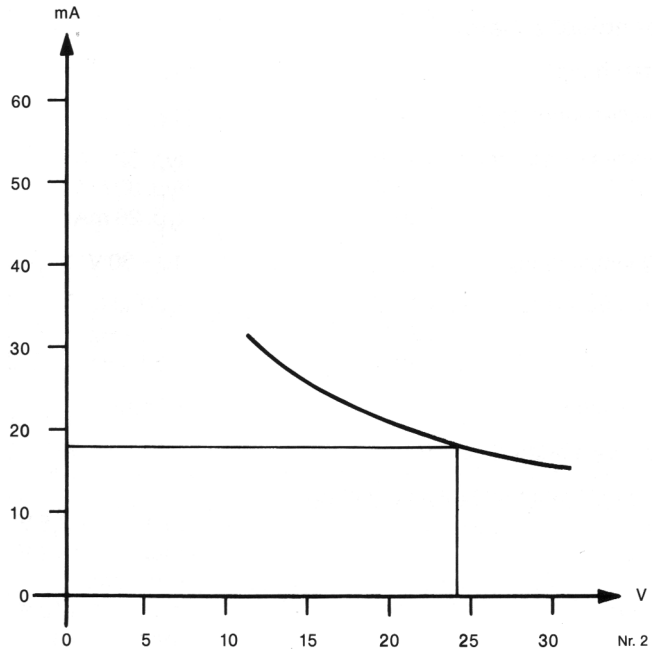
Truth table

Inputs						Outputs
LT*	BI*	EL	C 2^2	B 2^1	A 2^0	Display
1	1	0	0	0	0	+1
1	1	0	0	0	1	-
1	1	0	0	1	0	1
1	1	0	0	1	1	-1
1	1	0	1	0	0	+
1	1	0	1	0	1	+1
1	1	0	1	1	0	+1
1	1	0	1	1	1	-
1	1	0	0	0	0	+1
1	1	0	0	0	1	-
0	1	x	x	x	x	+1 (Test)
1	0	x	x	x	x	none
1	1	1	x	x	x	stored*

x = «0» or «1»

* Inputs BI and LT are internally wired to 1. An open collector control circuit is needed.

Supply current in relation to supply voltage

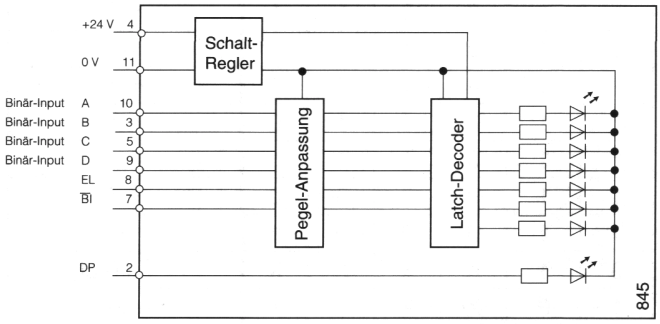


Type	VDC	Ordering code
822,	24 V	822-057-21

Type 845

- 7-segment display
- Height of character 16 mm
- Memory
- Binary input
- Signal level adaptation
- 24 V Signal- and supply voltage
- Depth when mounted 64 mm
- CE-konform

Circuit diagram



In this module, the display is controlled by the Binary code in positive logic. The signal and supply voltage is +24 V. A control signal (input EL) makes it possible to freeze the display without affecting the incoming BCD code signals.

Technical data

Character height		16 mm
Supply voltage VCC		12...30 V
Supply current I_{CC} with V_{CC}	= 12 V	typ. 52 mA
	= 24 V	typ. 32 mA
	= 30 V	typ. 28 mA
Signal voltage		10...30 V
Limit frequency with V_{CC}	= 12 V	≤ 20 kHz
	= 24 V	≤ 50 kHz
	= 30 V	≤ 50 kHz
Depth behind panel		64 mm

Input data without DP

Input voltage (all inputs)

U_{in} «0»	min.	-3.5 V
	max.	+2 V
	or open	
U_{in} «1 »	min.	+10 V
	max.	+30 V

Input currents all inputs

I_{in} «0» with	U_{in} = -3.5 V	max.	-0.3 mA
	U_{in} = +2 V	max.	+1 mA
I_{in} «1» with	U_{in} = +10 V	max.	6.5 mA
	U_{in} = +30 V	max.	14 mA

Decimal point (DP): The decimal point must be controlled externally. The module features an integral current limiting resistor and a protective diode.
«DP» on «0» Decimal point off
«DP» on «1» Decimal point on

Truth table

Inputs						Outputs
$\overline{BI}$	EL	D 2^3	C 2^2	B 2^1	A 2^0	Display
	0	0	0	0	0	0
1	0	0	0	0	1	1
1	0	0	0	1	0	2
1	0	0	0	1	1	3
1	0	0	1	0	0	4
1	0	0	1	0	1	5
1	0	0	1	1	0	6
1	0	0	1	1	1	7
1	0	1	0	0	0	8
1	0	1	0	0	1	9
1	0	1	0	1	0	A
1	0	1	0	1	1	b
1	0	1	1	0	0	C
1	0	1	1	0	1	d
1	0	1	1	1	0	E
1	0	1	1	1	1	F
0	x	x	x	x	x	none
1	1	x	x	x	x	stored*

x = «0» or «1»

* Controlled and applied Binary Code during the leading edge of the «EL» instruction signal.

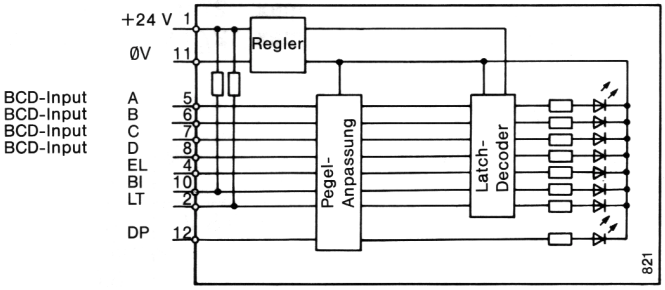
Supply current in relation to supply voltage

Type	VDC	Ordering code
845,	24 V	845-057-21

Type 846

- 7-segment display
- Height of character 16 mm
- Memory
- BCD-Input
- Signal level adaptation
- 24 V Signal- and supply voltage
- Depth when mounted 74 mm

Circuit diagram



In this module, the display is controlled by the Binary Code in positive logic. The signal and supply voltage is +24 V. A control signal (input EL) makes it possible to freeze the display without affecting the incoming Binary Code signals. Inputs «BI» and «LT» are already connected to the 24 V power supply via internal resistors. If these inputs are not used, the module will function properly due to these resistors. Both of these inputs must be controlled in open collector circuits.

Technical data

Character height		16 mm
Supply voltage V_{CC}		12 V...30 V
Supply current I_{CC} with V_{CC}	= 12 V	typ. 52 mA
	= 24 V	typ. 32 mA
	= 30 V	typ. 28 mA
Signal voltage		10 V...30 V
Limit frequency with V_{CC}	= 12 V	≤ 10 kHz
	= 24 V	≤ 15 kHz
	= 30 V	≤ 20 kHz
Depth behind panel		74 mm

Input data

Input voltage all inputs (except DP)

U_{in} «0»	min.	- 3.5 V
		or open
	max.	+2 V
U_{in} «1»	min.	+10 V
	max.	+30 V

Input voltage Input DP

U_{in} «0»	min.	-3.5 V
	max.	+0.7 V
U_{in} «1 »	min.	+1.1 V
	max.	+30 V
		or open

Input currents all inputs (except BL, LT and DP)

I_{in} «0» with	U_{in} = -3.5 V	max.	-150 mA
	U_{in} = +2 V	max.	140 µA
I_{in} «1» with	U_{in} = +10 V	max.	700 µA
	U_{in} = +30 V	max.	2.6 mA

Input currents Inputs LT, BI

I_{in} «0» with U_{in}	= -3.5 V	max. -11 mA
	= +2 V	max. -9.2 mA
I_{in} «1» with U_{in}	= +10 V	max. -7.2 mA
	= +30 V	max. 3 mA

Input currents Input DP

I_{in} «0» with U_{in}	= -3.5 V	max. -1 mA
	= +0.7 V	max. -400 µA
I_{in} «1» with U_{in}	= +1.1 V	max. -10 µA
	= +30 V	max. 1.6 µA

DP (Decimal point): «DP» on «0» Decimal point on
«DP» on «1» Decimal point off
(+24 V or open)

Truth table

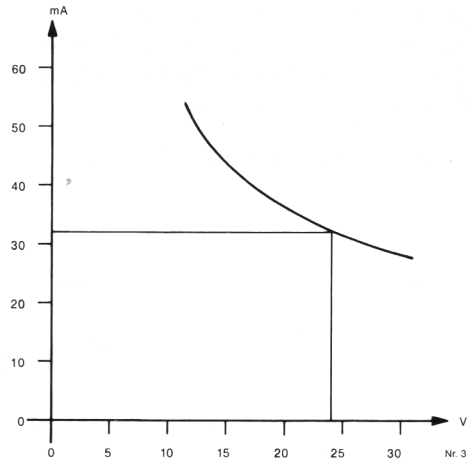
Inputs							Outputs
LT*	BI*	EL	D 2^3	C 2^2	B 2^1	A 2^0	Display
1	1	0	0	0	0	0	0
1	1	0	0	0	0	1	1
1	1	0	0	0	1	0	2
1	1	0	0	0	1	1	3
1	1	0	0	1	0	0	4
1	1	0	0	1	0	1	5
1	1	0	0	1	1	0	6
1	1	0	0	1	1	1	7
1	1	0	1	0	0	0	8
1	1	0	1	0	0	1	9
1	1	0	1	0	1	0	A
1	1	0	1	0	1	1	b
1	1	0	1	1	0	0	C
1	1	0	1	1	0	1	d
1	1	0	1	1	1	0	E
1	1	0	1	1	1	1	F
0	*x*	*x*	*x*	*x*	*x*	*x*	8 (Test)
1	0	*x*	*x*	*x*	*x*	*x*	none
1	1	1	*x*	*x*	*x*	*x*	stored**

x = «0» or «1»

* Inputs BI and LT are internally wired to H. An open collector control circuit is needed.

** Depends on the BCD value during the leading edge of the «EL».

Supply current in relation to supply voltage



Type	VDC	Ordering code
846,	24 V	846-057-21

Accessories

Series 800	Ordering code
Dummy housing, black	800-01-102
End bracket pair, black (up to 3 mm panel thickness)	800-03-302
End bracket pair, black (up to 5 mm panel thickness)	800-03-802
Pair of division plates, black (up to 3 mm panel thickness)	800-04-302
Pair of division plates, black (up to 5 mm panel thickness)	800-04-802
Contrast filter, length 20 mm	800-06-020
Contrast filter, length 40 mm	800-06-040
Contrast filter, length 60 mm	800-06-060
Contrast filter, length 80 mm	800-06-080
Contrast filter, length 100 mm	800-06-100
Contrast filter, length 120 mm	800-06-120
Mutter M2 A100	M2A100
Threaded rod M2 up to 300 mm	G2x...mm
Block assembly	BLOCK800

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Codicount series	800
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Serie 800 with H, M or S switches

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